

# RJK5013DPP-A0

500V - 14A - MOS FET High Speed Power Switching R07DS1428EJ0100 Rev.1.00 Mar.10.2021

#### **Features**

• Low on-resistance

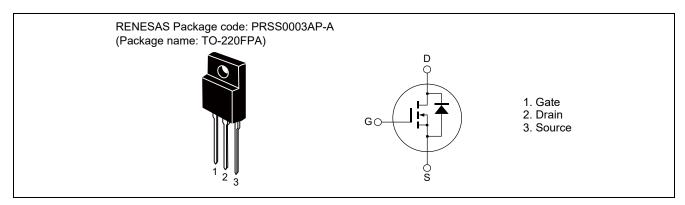
 $R_{DS(on)} = 0.385 \Omega \text{ typ.}$  (at  $I_D = 7 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$ ,  $Ta = 25 ^{\circ}\text{C}$ )

Low leakage current

· High speed switching

· Quality grade: Standard

#### **Outline**



## **Absolute Maximum Ratings**

(Ta = 25 °C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	500	V
Gate to source voltage	V <sub>GSS</sub>	±30	V
Drain current	I <sub>D</sub> Notes4	14	Α
Drain peak current	I <sub>D</sub> (pulse) <sup>Notes1</sup>	42	Α
Body-drain diode reverse drain current	I <sub>DR</sub>	14	Α
Body-drain diode reverse drain peak current	I <sub>DR (pulse)</sub> Notes1	42	Α
Avalanche current	I <sub>AP</sub> Notes3	4	Α
Avalanche energy	E <sub>AR</sub> Notes3	0.88	mJ
Channel dissipation	Pch Notes2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

Notes: 1. PW  $\leq$  10  $\mu$ s, duty cycle  $\leq$  1 %

- 2. Value at Tc = 25 °C
- 3. STch = 25 °C, Tch  $\leq$  150 °C
- 4. Limited by maximum safe operation area

# **Thermal Resistance Characteristics**

(Ta = 25 °C)

Item	Symbol	Max. Value Notes5	Unit
Channel to case thermal impedance	θch-c	4.17	°C/W

Notes: 5. Designed target value on Renesas measurement condition. (Not tested)

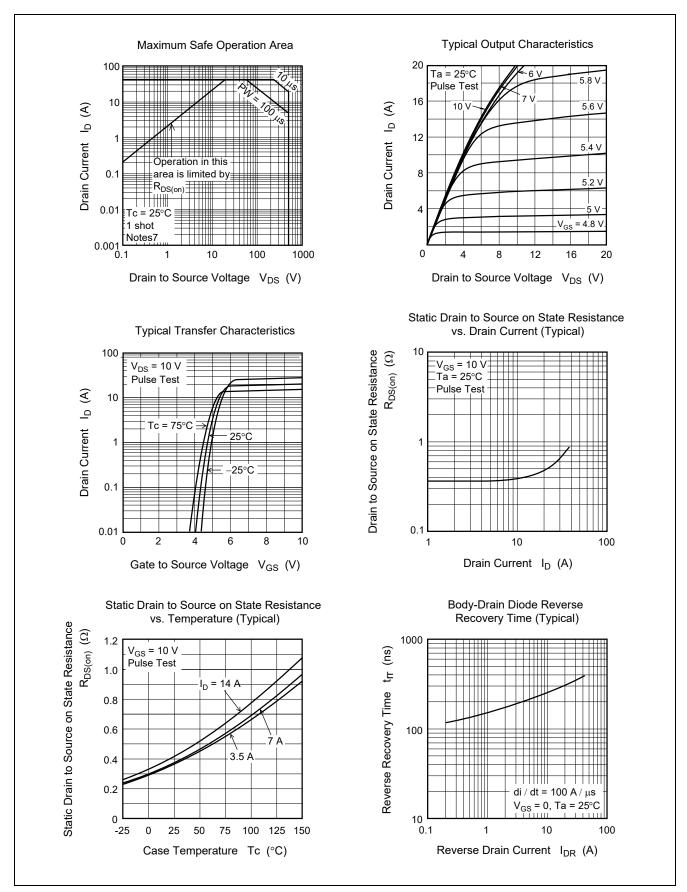
## **Electrical Characteristics**

(Ta = 25 °C)

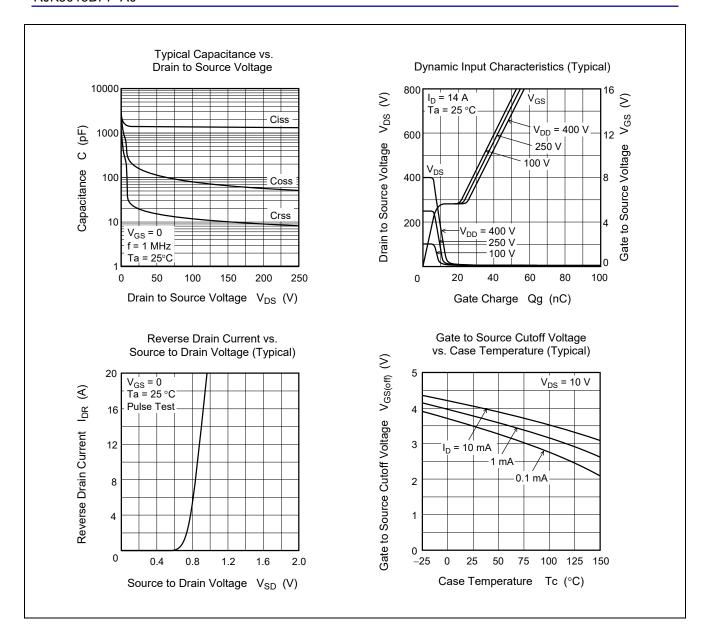
Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	500	_	_	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Zero gate voltage drain current	IDSS	_	_	1	μΑ	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0
Gate to source leak current	Igss	_	_	±0.1	μΑ	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	V <sub>GS(off)</sub>	3.0	_	4.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Static drain to source on state	R <sub>DS(on)</sub>	_	0.385	0.465	Ω	I <sub>D</sub> = 7 A, V <sub>GS</sub> = 10 V Notes6
resistance						
Input capacitance	Ciss	_	1450	_	pF	V <sub>DS</sub> = 25 V
Output capacitance	Coss	_	155	_	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	Crss	_	19	_	pF	f = 1 MHz
Turn-on delay time	t <sub>d(on)</sub>	_	34	_	ns	I <sub>D</sub> = 7 A
Rise time	tr	_	24	_	ns	$V_{GS}$ = 10 V $R_L$ = 35.7 $\Omega$ $Rg$ = 10 $\Omega$
Turn-off delay time	t <sub>d(off)</sub>	_	86	_	ns	
Fall time	t <sub>f</sub>	_	16	_	ns	
Total gate charge	Qg	_	38	_	nC	V <sub>DD</sub> = 400 V
Gate to source charge	Qgs	_	8	_	nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 14 A
Gate to drain charge	Qgd	_	17	_	nC	
Body-drain diode forward voltage	$V_{DF}$	_	0.9	1.5	V	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 Notes6
Body-drain diode reverse recovery time	t <sub>rr</sub>	_	310	_	ns	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 di <sub>F</sub> /dt = 100 A/μs

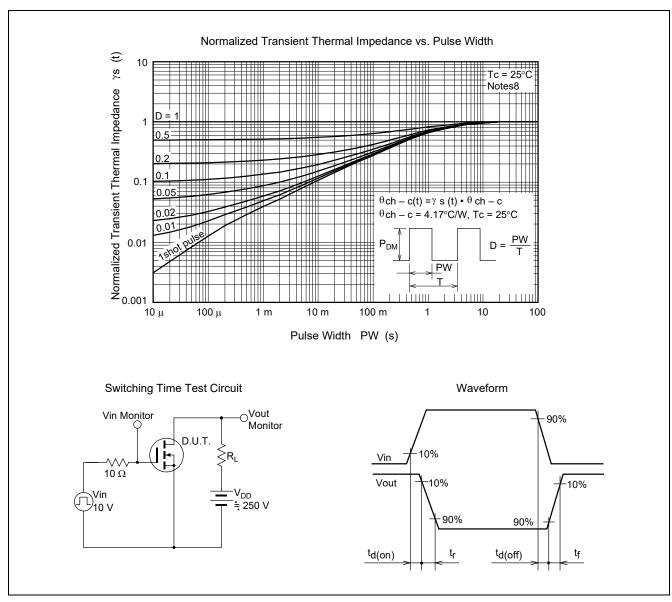
Notes: 6. Pulse test

### **Main Characteristics**



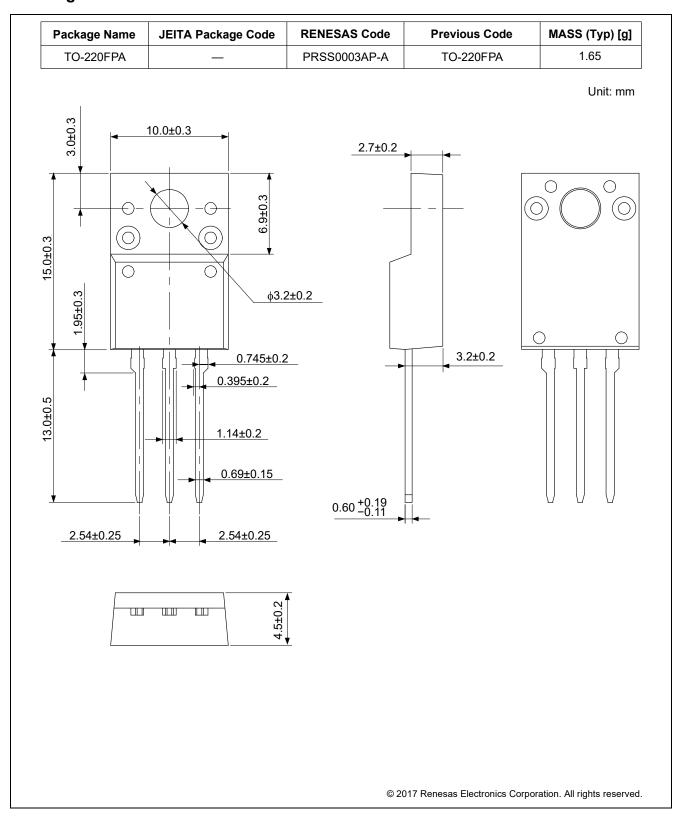
Notes: 7. Designed target value on Renesas measurement condition. (Not tested)
Renesas recommends that operating conditions are designed according to a document "Power MOS FET •
IGBT Attention of Handling Semiconductor Devices".





Notes: 8. Designed target value on Renesas measurement condition. (Not tested)

## **Package Dimensions**



# **Ordering Information**

Orderable Part No.	Quantity	Shipping Container
RJK5013DPP-A0#T2	2500 pcs	Box (Tube)

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(Rev.5.0-1 October 2020)

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