# RJF0610DSP

## 60V , 1.5A Silicon N channel Thermal FET
## Power Switching

R07DS0560EJ0301
Rev.3.01
Sep 06, 2016

## Description

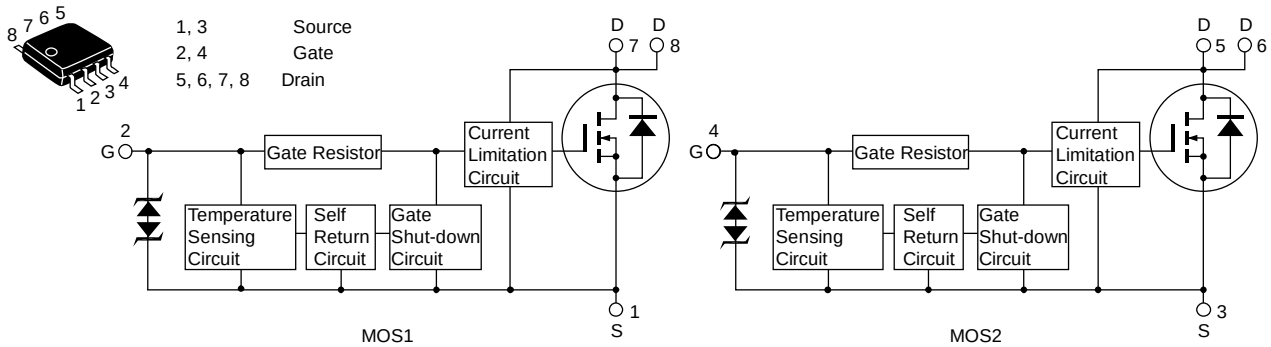
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

## Features

- Logic level operation (5 to 6 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Temperature hysteresis type.
- High density mounting
- Power supply voltage applies 12 V and 24 V.

## Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV> )




## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 60 | V |
| Gate to source voltage | $V_{GSS}$ | 16 | V |
| Gate to source voltage | $V_{GSS}$ | –2.5 | V |
| Drain current | $I_D$ Note4 | 1.5 | A |
| Body-drain diode reverse drain current | $I_{DR}$ | 1.5 | A |
| Avalanche current | $I_{AP}$ Note 3 | 0.95 | A |
| Avalanche energy | $E_{AR}$ Note 3 | 77.4 | mJ |
| Channel dissipation | Pch Note 1 | 2 | W |
| Channel dissipation | Pch Note 2 | 3 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

Notes: 1. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
2. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
3. Tch = 25°C, Rg ≥ 50 Ω, L = 100 mH
4. It provides by the current limitation lower bound value.

## Typical Operation Characteristics

(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 3.5 | — | — | V | |
| | $V_{IL}$ | — | — | 1.2 | V | |
| Input current (Gate non shut down) | $I_{IH1}$ | — | — | 100 | μA | Vi = 5 V, $V_{DS}$ = 0 |
| | $I_{IH2}$ | — | — | 50 | μA | Vi = 3.5 V, $V_{DS}$ = 0 |
| | $I_{IL}$ | — | — | 1 | μA | Vi = 1.2 V, $V_{DS}$ = 0 |
| Input current (Gate shut down) | $I_{IH(sd)1}$ | — | 0.4 | — | mA | Vi = 8 V, $V_{DS}$ = 0 |
| | $I_{IH(sd)2}$ | — | 0.24 | — | mA | Vi = 5 V, $V_{DS}$ = 0 |
| | $I_{IH(sd)3}$ | — | 0.16 | — | mA | Vi = 3.5 V, $V_{DS}$ = 0 |
| Shut down temperature | Tsd | — | 175 | — | °C | Channel temperature |
| Return temperature | Thr | — | 120 | — | °C | Channel temperature |
| Gate operation voltage | Vop | 3.5 | — | 12 | V | |
| Drain current (Current limitation value) | $I_{D\ limit}$ | 1.5 | — | — | A | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V Note 5 |

Notes; 5. Pulse test

## Electrical Characteristics

(Ta = 25°C)

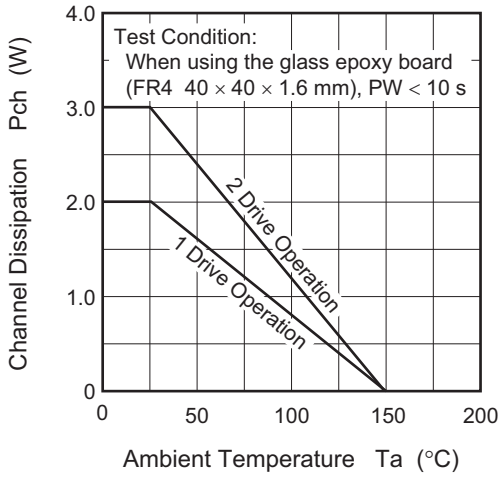
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain current | $I_{D1}$ | — | — | 2.4 | A | $V_{GS}$ = 3.5 V, $V_{DS}$ = 2 V |
| | $I_{D2}$ | — | — | 10 | mA | $V_{GS}$ = 1.2 V, $V_{DS}$ = 2 V |
| | $I_{D3}$ | 1.5 | — | — | A | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V Note 6 |
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 60 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | 16 | — | — | V | $I_G$ = 500 μA, $V_{DS}$ = 0 |
| | $V_{(BR)GSS}$ | –2.5 | — | — | V | $I_G$ = –100 μA, $V_{DS}$ = 0 |
| Gate to source leak current | $I_{GSS1}$ | — | — | 100 | μA | $V_{GS}$ = 5 V, $V_{DS}$ = 0 |
| | $I_{GSS2}$ | — | — | 50 | μA | $V_{GS}$ = 3.5 V, $V_{DS}$ = 0 |
| | $I_{GSS3}$ | — | — | 1 | μA | $V_{GS}$ = 1.2 V, $V_{DS}$ = 0 |
| | $I_{GSS4}$ | — | — | –100 | μA | $V_{GS}$ = –2.4 V, $V_{DS}$ = 0 |
| Input current (shut down) | $I_{GS(OP)1}$ | — | 0.4 | — | mA | $V_{GS}$ = 8 V, $V_{DS}$ = 0 |
| | $I_{GS(OP)2}$ | — | 0.24 | — | mA | $V_{GS}$ = 5 V, $V_{DS}$ = 0 |
| | $I_{GS(OP)3}$ | — | 0.16 | — | mA | $V_{GS}$ = 3.5 V, $V_{DS}$ = 0 |
| Zero gate voltage drain current | $I_{DSS}$ | — | — | 10 | μA | $V_{DS}$ = 60 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.4 | — | 2.5 | V | $I_D$ = 1 mA, $V_{DS}$ = 10 V |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 207 | 285 | mΩ | $I_D$ = 0.7 A, $V_{GS}$ = 5 V Note 6 |
| | $R_{DS(on)}$ | — | 153 | 214 | mΩ | $I_D$ = 0.7 A, $V_{GS}$ = 10 V Note 6 |
| Output capacitance | Coss | — | 267 | — | pF | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 4.3 | — | μs | $I_D$= 0.7 A, $V_{GS}$ = 5 V, $R_L$ = 43 Ω |
| Rise time | $t_r$ | — | 18.3 | — | μs | |
| Turn-off delay time | $t_{d(off)}$ | — | 0.62 | — | μs | |
| Fall time | $t_f$ | — | 0.61 | — | μs | |
| Body-drain diode forward voltage | $V_{DF}$ | — | 0.8 | — | V | $I_F$ = 1.5 A, $V_{GS}$ = 0 |
| Body-drain diode reverse recovery time | $t_{rr}$ | — | 55 | — | ns | $I_F$ = 1.5 A, $V_{GS}$ = 0<br>$di_F/dt$ = 50 A/μs |
| Over load shut down operation time Note 7 | $t_{os1}$ | — | 18 | — | ms | $V_{GS}$ = 5 V, $V_{DD}$ = 16 V |
| | $t_{os2}$ | — | 5.7 | — | ms | $V_{GS}$ = 5 V, $V_{DD}$ = 24 V |

Notes: 6. Pulse test

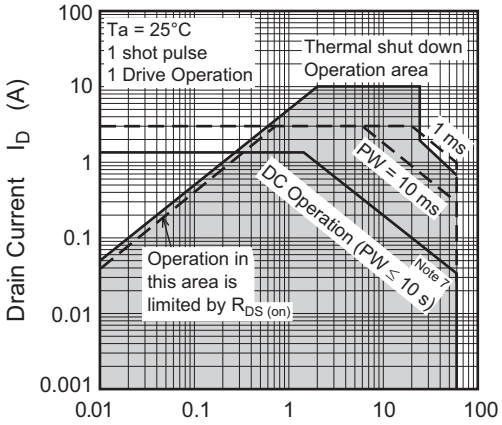
7. Including the junction temperature rise of the over loaded condition.

## Main Characteristics

Power vs. Temperature Derating

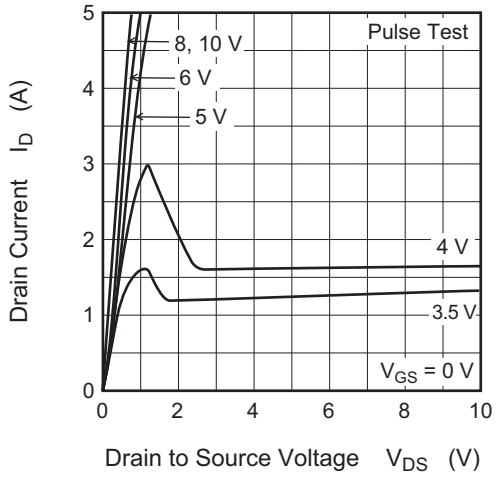



Maximum Safe Operation Area

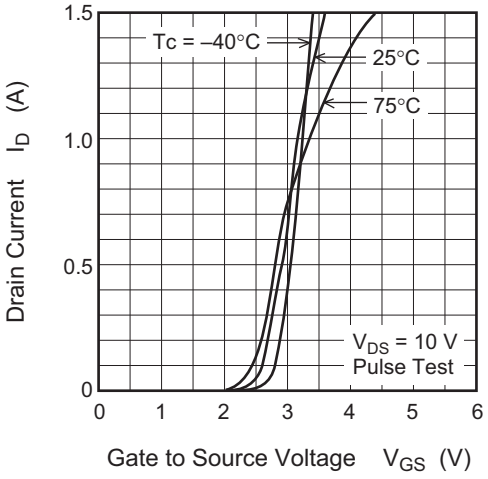



Note 7:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

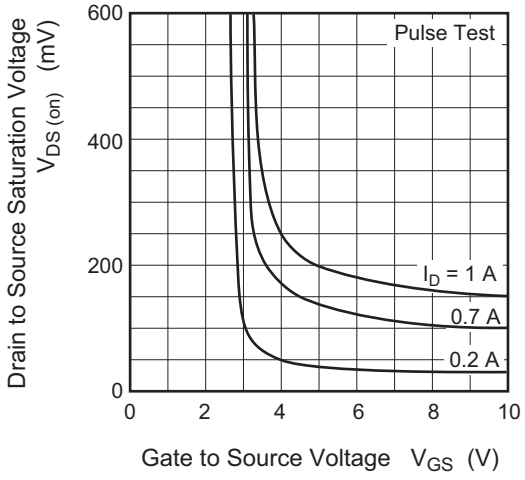
Typical Output Characteristics



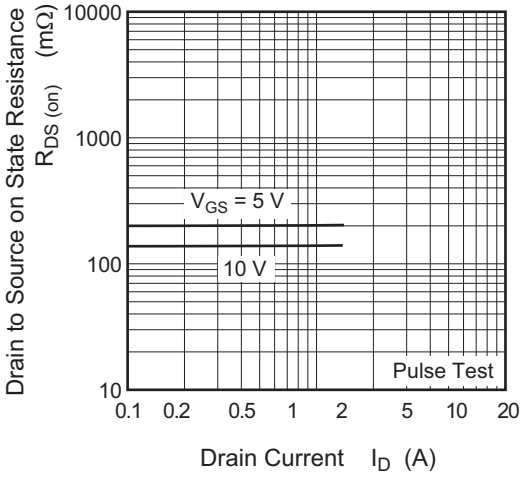

Typical Transfer Characteristics



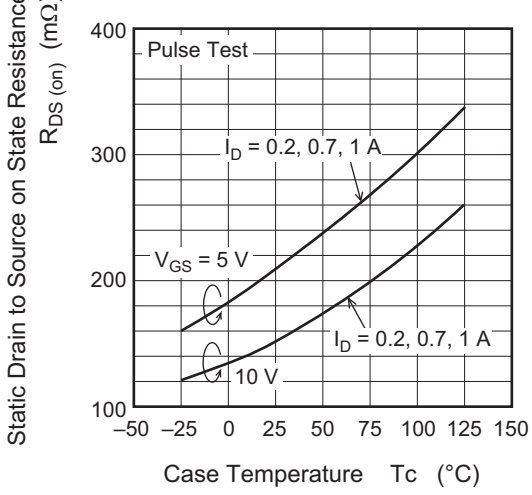

Drain to Source Saturation Voltage vs.
Gate to Source Voltage



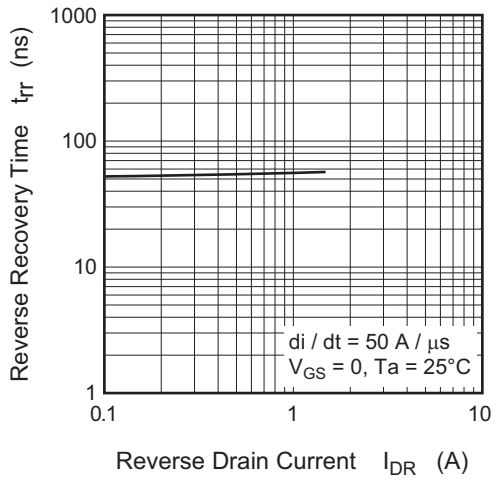

Static Drain to Source on State Resistance
vs. Drain Current



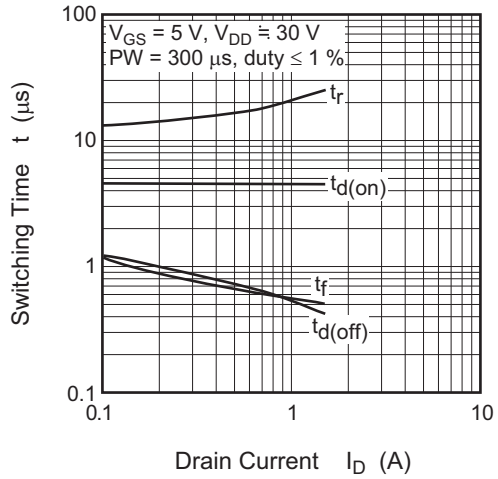
Static Drain to Source on State Resistance vs. Temperature



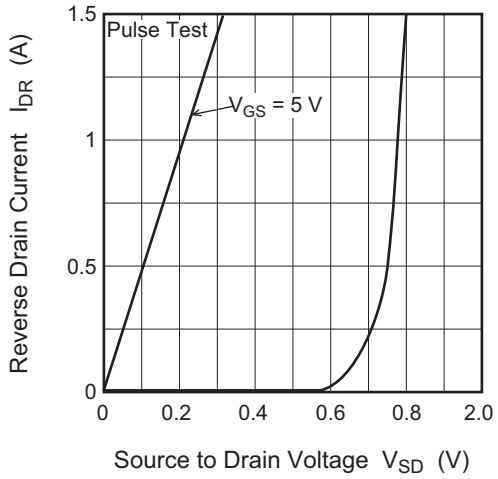

Body-Drain Diode Reverse Recovery Time



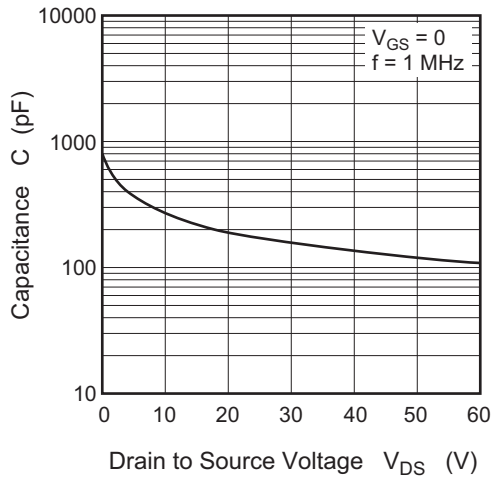

Switching Characteristics



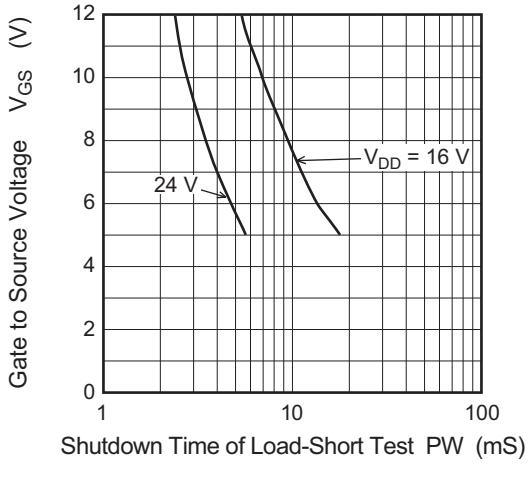

Reverse Drain Current vs. Source to Drain Voltage



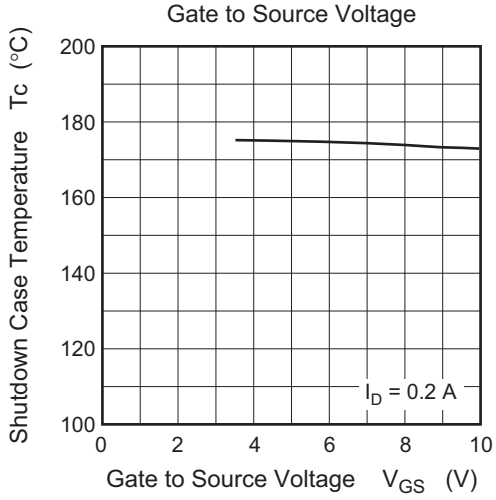

Typical Capacitance vs. Drain to Source Voltage



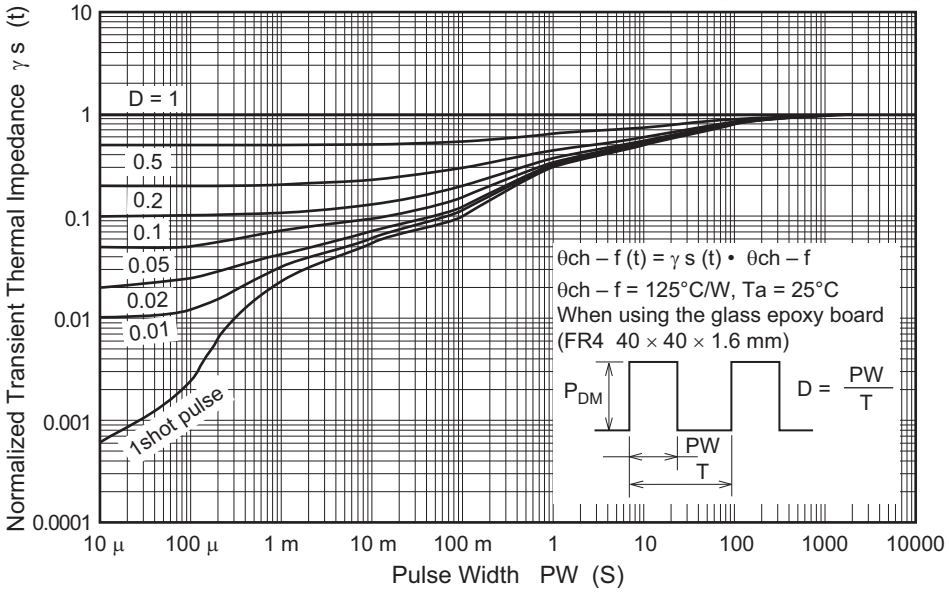

Gate to Source Voltage vs. Shutdown Time of Load-Short Test



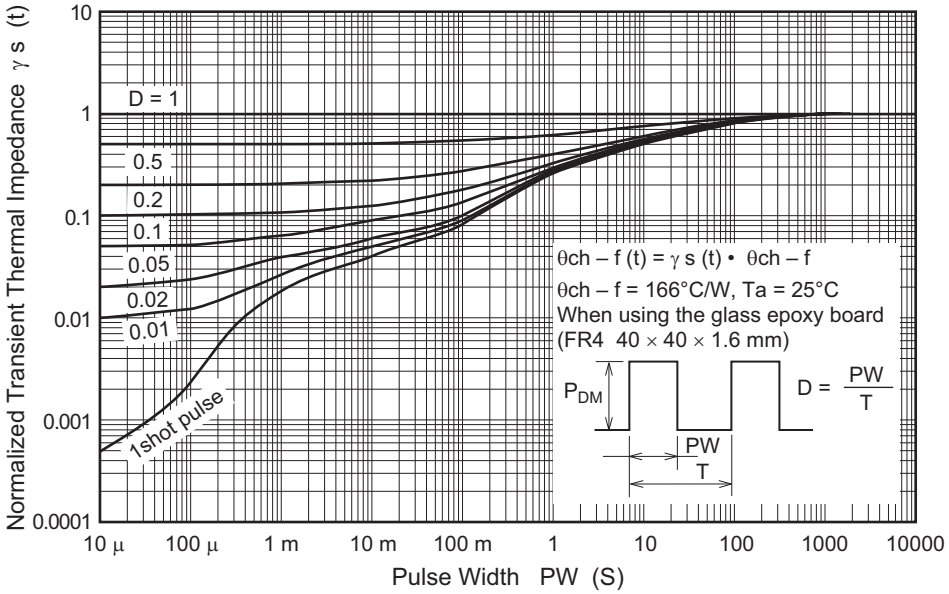
Shutdown Case Temperature vs.
Gate to Source Voltage



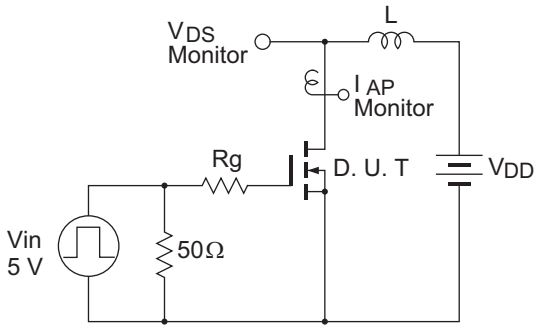

Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)




Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

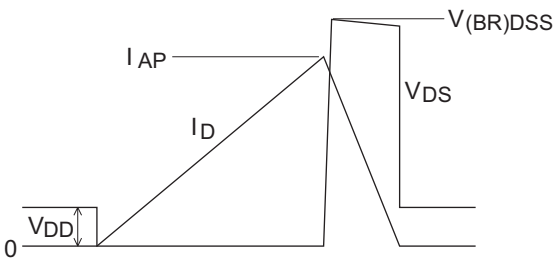


Avalanche Test Circuit

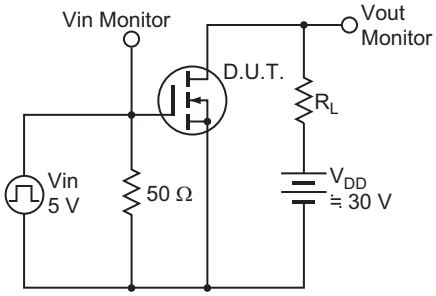



Avalanche Waveform

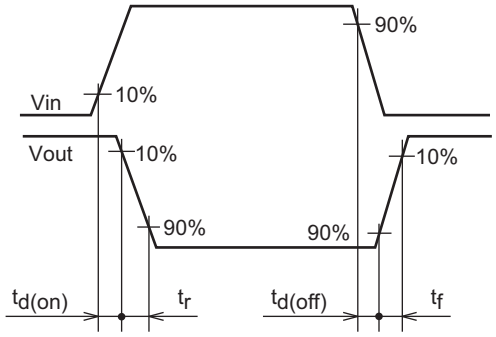
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$




Switching Time Test Circuit

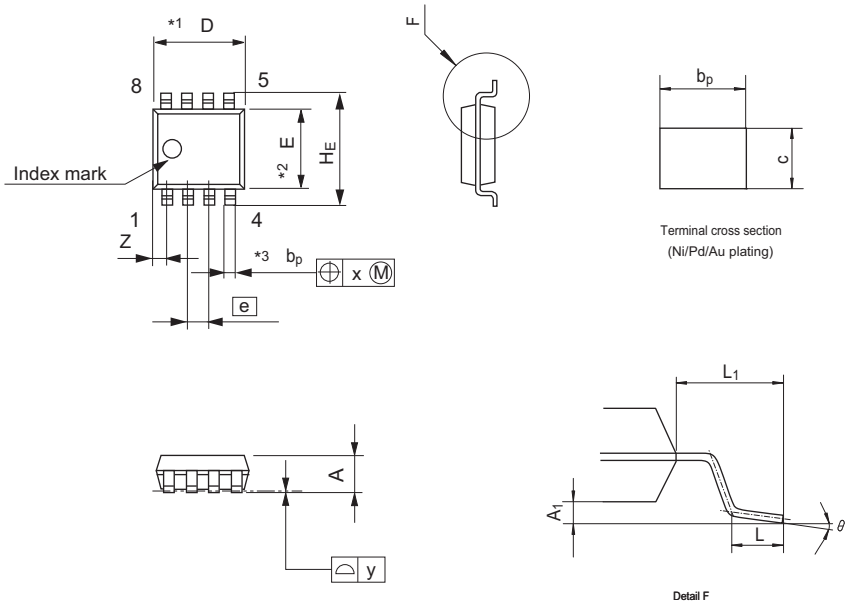



Waveform



## Package Dimensions

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|---|
| SOP-8 | P-SOP8-3.95 × 4.9-1.27 | PRSP0008DD-D | FP-8DAV | 0.085g |




NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 4.90 | 5.3 |
| E | — | 3.95 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.10 | 0.14 | 0.25 |
| A | — | — | 1.75 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 5.80 | 6.10 | 6.20 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.1 |
| Z | — | — | 0.75 |
| L | 0.40 | 0.60 | 1.27 |
| $L_1$ | — | 1.08 | — |

## Ordering Information

| Orderable Part Number | Quantity | Shipping Container |
|---|---|---|
| RJF0610DSP-00#J0 | 2500 pcs | Taping (Reel) |

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