RAA305350MGBM

General purpose 3CH Driver IC

Rev.1.06
2021.2.17

1 Over View

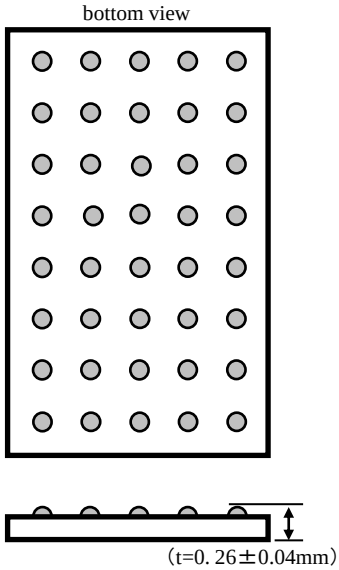
RAA305350MGBM is general-purpose 3CH H-bridge driver IC .This is a small size single chip IC constituted by the control block built in 32 bits RISC microcomputer and DSP, and by the driver block built in hall signal processing circuit.

2 Features

Applications

Smart phone, Tablet, Camera, Sensing and Actuator Control

Pin alignment image
(40pin 2.17mm x 3.60mm
0.4mm pitch square grid array)



WLBGA

Driver Block

[CH1/CH2/CH3]

(1)Built-in 3 channels H-bridge drivers
Composition : CH1, CH2, CH3
(2)Built-in 3 channels Hall signal processing circuits
Composition :
Constant Current Bias --- 3 channels
Gain Amp --- 3 channels (with gain resistor)
(3)Built-in 12bit-ADC with 6 channels input selector
(4)Configurable for VCM/Piezo/SMA/BLDC motor drive
(5)PWM/Linear drive
(6)Other
CH3（AF Control case）; Supports open/closed loop control

Controller

(1)Built-in 32bit RISC CPU
(2)Built-in Code Flash ROM(48KB)
(3)Built-in RAM(8KB) for program
(4)Built-in DSP 2 channels (GREEN_DSP_V2)
(5)Built-in SPI 2 channels
(6)Built-in Timer (16bit) 4 channels
(7)Built-in IIC serial interface 1 channel
(8)Built-in General purpose I/O 8lines (with interruption function)
(9)Clock frequency : Built-in PLL (x4, x6, x8, x12, x16)
For system clock ---------- 32.4MHz(Max)
For PWM clock of motor control ------- 162MHz(Max)
For SPI serial clock ---------- Master 4MHz(Max), Slave 2MHz(Max)
For IIC serial clock ---------- 1MHz(Max, Fast Mode+)

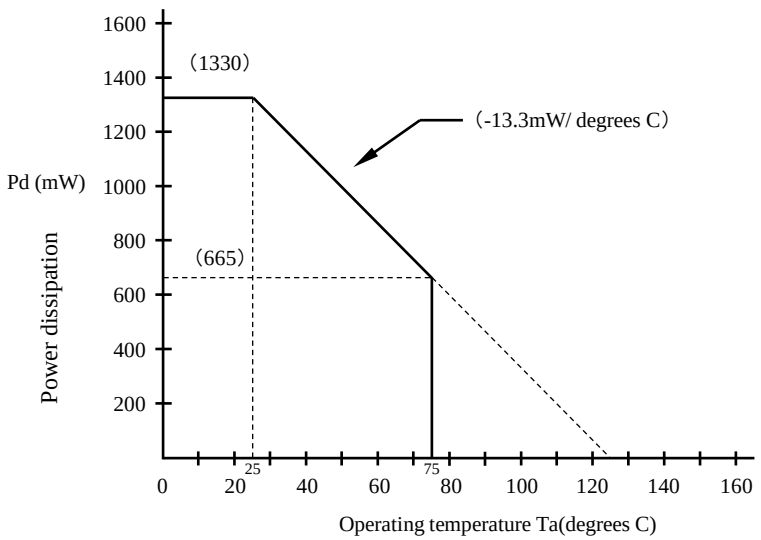
Others

(1)Built in POR(power on reset), TSD(thermal shut down)
(2)Built in Power save mode
(3)Built in IS/AF Driver control synchronized signal from Image Sensor (OIS case)

ABSOLUTE MAXIMUM RATING (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power dissipation	Pd	(1330)	mW	note1 (Ta=25 degrees C)
Thermal derating	Kθ	(-13.3)	mW/degrees C	note1 (Ta=25 degrees C)
Maximum junction temperature	Tj	125	degrees C	
Storage temperature	Tstg	-40 to 125	degrees C	
Power supply 1	VDD	4.6	V	note2
Power supply 2	VCC	4.6	V	note2
Power supply 3	VM	6.5	V	note2
Input voltage of terminals	Vin	-0.3 to VDD + 0.3	V	note3
DC output current	Iout	+/- 600	mA	note4
Peak output current	Iop	+/- 800	mA	note5 pulse width<10ms,Duty<=20%

Notes note1 : Glass epoxy board: 76mm × 114mm × 1.6mm 4layers board(Cu cover rate:1-layer 20%,2-layer 100%,3-layer 100%,4-layer 20%)
note2 : Don't impress a power supply conversely in principle.
note3 : Don't impress more than power supply voltage and below GND voltage in principle.
note4 : Don't exceed +/-200mA per channel.
note5 : Don't exceed the specification of output current, when more than one CH use them, turning on at the same time.



Notes The power consumption of this IC has the dominant electric power which each output transistor consumes.

Output transistor power consumption formula
(Output current)^2 x Ron (ex.) (400mA)^2 x 3.3 ohm=528mW

When ambient air temperature is 25 degrees C or more, please install a heat sink with reference to the above figure if needed.

To continue operating a long-time at high temperature impacts a product life.

RECOMMENDED OPERATING CONDITIONS (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power supply 1	VDD	1.7 to 3.3	V	
Power supply 2	VCC	2.7 to 3.3	V	
Power supply 3	VM	2.7 to 3.3	V	Linear drive mode
Power supply 4	VM	2.7 to 5.5	V	PWM drive mode

RATED POWER SUPPLY VOLTAGE (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power supply 1	VDD	1.8	V	
Power supply 2	VCC	2.8	V	
Power supply 3	VM	2.8	V	Linear / PWM drive mode
Power supply 4	VM	5.0	V	PWM drive mode

OPERATING TEMPERATURE

ITEM	SYMBOL	RATING	UNIT	NOTES
Operating temperature	Topr	-30 to 85	degrees C	note1

note1 : Flash write / erase : -10 to 50 degrees C

PIN LOCATION

Bottom View

	5	4	3	2	1
A	RESET_N	GPIO10	GPIO11	SPI_DAT0	SPI_MISO0
B	EXCLK	IMGHD	REGM	VDD	SPI_SCK0
C	SWDIO	SWCLK	TEST	SPI_CS0	SPI_CS1
D	SCL	SDA	MON (analog monitor)	SPI_SCK1	SPI_DAT1
E	VSS	AD2	HA1_INP	HA1_INN	HD1_OUT
F	VCC	HA3_INP	HA2_INP	HA2_INN	HD2_OUT
G	HA3_INN	OUT3_A	OUT1_B	OUT2_B	HD3_OUT
H	VM	OUT3_B	OUT1_A	OUT2_A	PGND

Power Supply

GND

Driver

Sensing circuit

Controller

RENESAS TEST (Don't Connect)

TopView

	1	2	3	4	5
A	SPI_MISO0	SPI_DAT0	GPIO11	GPIO10	RESET_N
B	SPI_SCK0	VDD	REGM	IMGHD	EXCLK
C	SPI_CS1	SPI_CS0	TEST	SWCLK	SWDIO
D	SPI_DAT1	SPI_SCK1	MON (analog monitor)	SDA	SCL
E	HD1_OUT	HA1_INN	HA1_INP	AD2	VSS
F	HD2_OUT	HA2_INN	HA2_INP	HA3_INP	VCC
G	HD3_OUT	OUT2_B	OUT1_B	OUT3_A	HA3_INN
H	PGND	OUT2_A	OUT1_A	OUT3_B	VM

Pin Functions

No.	Land Address	Pin	Sub Function			I/O Level	IN/OUT	Initial Condition *4	Function	Termination of unused pin
			GPIO	CPU INT	DSP INT		Power/GND			
1	F5	VCC	-	-	-	-	Power supply	-	Power supply for analog block and flash	-
2	B2	VDD							Power supply for I/O and digital block	-
3	H5	VM							Power supply for CH1,CH2,CH3 driver	-
4	H1	PGND	-	-	-	-	GND	-	Power system GND	-
5	E5	VSS							Digital and analog GND	-
6	H3	**OUT1_A**	-	-	-	VM	OUT	Hi-Z	CH1 driver output A	*1
7	G3	**OUT1_B**	-	-	-		OUT	Hi-Z	CH1 driver output B	*1
8	H2	**OUT2_A**	-	-	-		OUT	Hi-Z	CH2 driver output A	*1
9	G2	**OUT2_B**	-	-	-		OUT	Hi-Z	CH2 driver output B	*1
10	G4	**OUT3_A**	-	-	-		OUT	Hi-Z	CH3 driver output A	*1
11	H4	**OUT3_B**	-	-	-		OUT	Hi-Z	CH3 driver output B	*1
12	D3	MON	-	-	-	VCC	OUT	Hi-Z	To Monitor Loop Gain	*1
13	E1	**HD1_OUT**	-	-	-		OUT	Hi-Z	Hall CH1 constant current output	*1
14	E3	**HA1_INP**	-	-	-		IN	Hi-Z	Hall amplifier CH1 non-inverting input	*2
15	E2	**HA1_INN**	-	-	-		IN	Hi-Z	Hall amplifier CH1 inverting input	
16	F1	**HD2_OUT**	-	-	-		OUT	Hi-Z	Hall CH2 constant current output	*1
17	F3	**HA2_INP**	-	-	-		IN	Hi-Z	Hall amplifier CH2 non-inverting input	*2
18	F2	**HA2_INN**	-	-	-		IN	Hi-Z	Hall amplifier CH2 inverting input	
19	G1	**HD3_OUT**	-	-	-		OUT	Hi-Z	Hall CH3 constant current output	*1
20	F4	**HA3_INP**	-	-	-		IN	Hi-Z	Hall amplifier CH3 non-inverting input	*2
21	G5	**HA3_INN**	-	-	-		IN	Hi-Z	Hall amplifier CH3 inverting input	
22	E4	AD2	-	-	-		IN	Hi-Z	ADC input	*2
23	A5	RESET_N	-	-	-	VDD	IN	Hi-Z	Reset	-
24	D5	SCL	GPIO00	INTIN0	INT IN0		IN/OUT	Hi-Z	SCL for I2C Interface / GPIO port GPIO00 / UART RXD00 / CPU INTIN0 / DSP INT IN0	*3
25	D4	SDA	GPIO01	-	-		IN/OUT	Hi-Z	SDA for I2C Interface / GPIO port GPIO01 / UART TXD00	*3
26	B1	SPI_SCK0	GPIO02	-	-		IN/OUT	Hi-Z	CLOCK input or output for SPI (SCK) / GPIO port GPIO02	*3
27	A2	SPI_DAT0	GPIO03	-	-		IN/OUT	Hi-Z	Data input or output for SPI (DAT) / Data output for SPI (MOSI) / GPIO port GPIO03	*3
28	A1	SPI_MISO0	GPIO07	INTIN7	-		IN/OUT	Hi-Z	Data input for SPI (MISO) / GPIO port GPIO07 / CPU INTIN7	*3
29	C2	SPI_CS0	GPIO04	INTIN4	-		IN/OUT	Hi-Z	Chip select input or output for SPI (CS) / GPIO port GPIO04 / TAU TO0, TO1, TO2 / CPU INTIN4	*3
30	B5	EXCLK	-	-	-		IN	Hi-Z	External CLOCK input	-
31	D2	SPI_SCK1	GPIO08	-	-		IN/OUT*6	Hi-Z	CLOCK input for SPI (SCK)	*3
32	D1	SPI_DAT1	GPIO09	-	-		IN/OUT*6	Hi-Z	Data input or output for SPI (DAT)	*3
33	C1	SPI_CS1	GPIO12	-	-		IN/OUT*6	Hi-Z	Chip select input or output for SPI (CS) / GPIO port GPIO12	*3
34	C4	SWCLK	GPIO05	INTIN5	-		IN/OUT*6	Hi-Z (Pull-up)*5	Clock input for Debugger / GPIO port GPIO05 / UART RXD00 / TAU TI2 / CPU INTIN5	*3
35	C5	SWDIO	GPIO06	INTIN6	-		IN/OUT*6	Hi-Z (Pull-up)*5	Data input/output for Debugger / GPIO port GPIO06 / UART TXD00 / TAU TI1 / CPU INTIN6	*3
36	B4	IMGHD	-	INTIN3	INT IN3		IN*6	Hi-Z	CPU INTIN3 / DSP INT IN3 (Image Sencor Sync signal)	*2
37	A4	GPIO10	GPIO10	INTIN1	INT IN1		IN/OUT*6	Hi-Z	GPIO port GPIO10 / TAU TO2 / CPU INTIN1 / DSP INT IN1	*3
38	A3	GPIO11	GPIO11	INTIN2	INT IN2		IN/OUT*6	Hi-Z	GPIO port GPIO11 / TAU TO3 / CPU INTIN2 / DSP INT IN2	*3
39	C3	TEST	-			-	IN	Pull-up	TEST for RENESAS	*1
40	B3	REGM	-			-	OUT	-	TEST for RENESAS	*1

*1 Open

*2 Connect to VSS

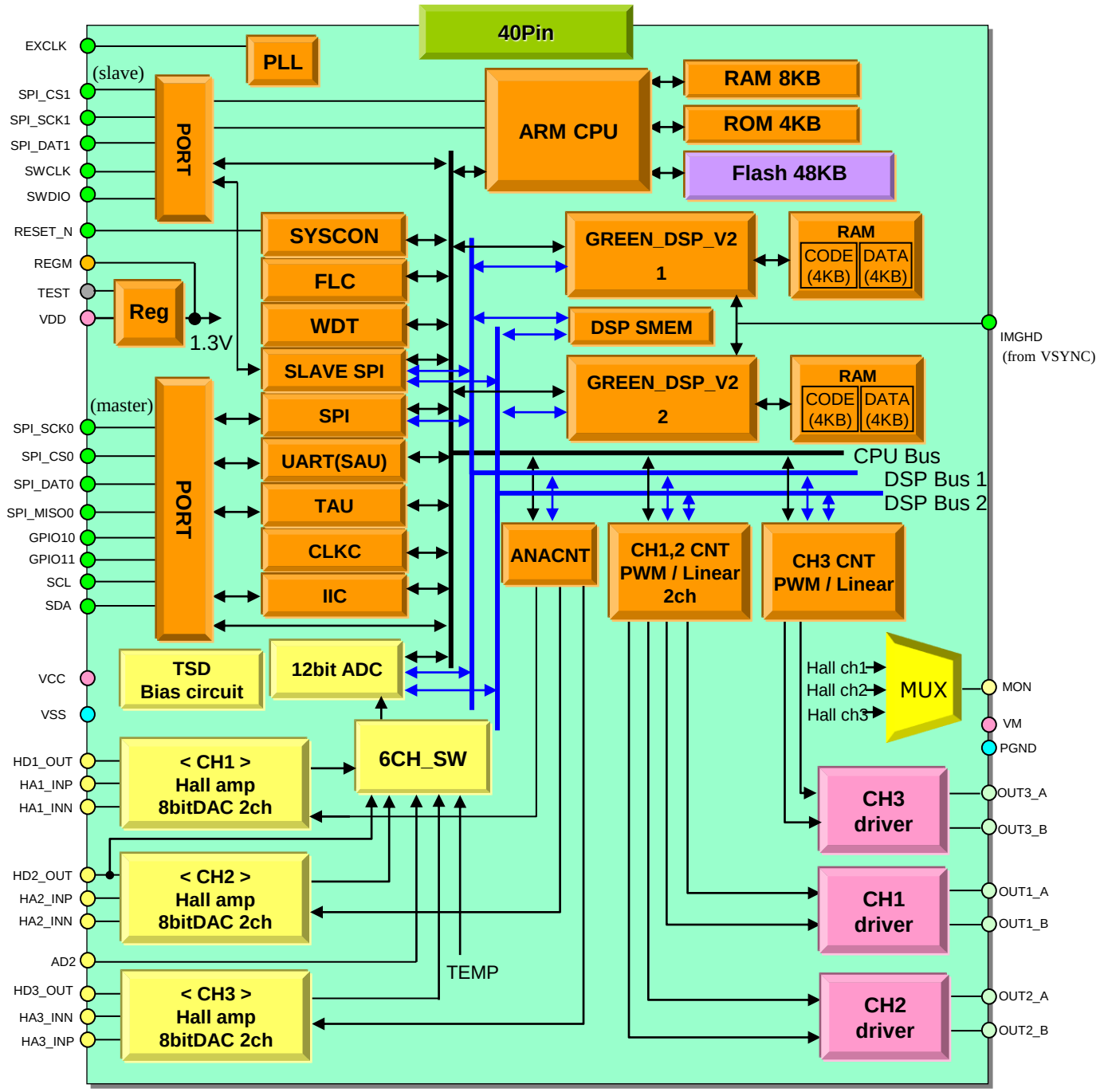
*3 'Connect to VSS' or
'Pin is Open,
,Pin enbled in PORTSEL register
,Switch to GPIO in PNMOD register
,Output Enable in GPIO0OE register
and output data fixed to '0' in GPIO0DT register.'

*4 An initial value is not influenced by the RESET_N terminal.

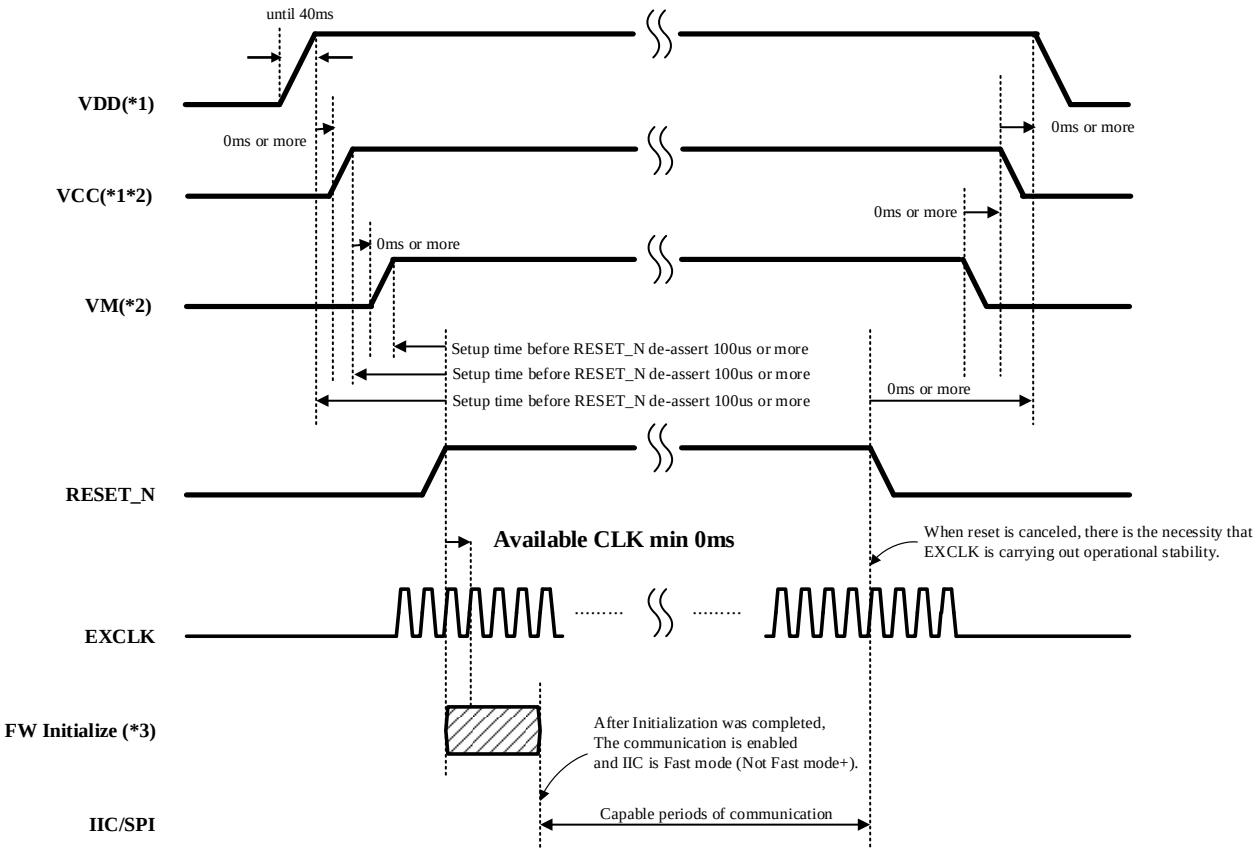
*5 Pull-up can be turned off by register setting.

*6 Pull-up can be turned on/off by register setting.

TOTAL BLOCK


40Pin
EXCLK
PLL
(slave)
SPI_CS1
SPI_SCK1
SPI_DAT1
SWCLK
SWDIO
PORT
ARM CPU
RAM 8KB
ROM 4KB
Flash 48KB
RESET_N
REGM
TEST
VDD
Reg
1.3V
SYSCON
FLC
WDT
SLAVE SPI
SPI
UART(SAU)
TAU
CLKC
IIC
GREEN_DSP_V2 1
RAM
CODE (4KB)
DATA (4KB)
DSP SMEM
GREEN_DSP_V2 2
IMGHD
(from VSYNC)
(master)
SPI_SCK0
SPI_CS0
SPI_DAT0
SPI_MISO0
GPIO10
GPIO11
SCL
SDA
CPU Bus
DSP Bus 1
DSP Bus 2
ANACNT
CH1,2 CNT PWM / Linear 2ch
CH3 CNT PWM / Linear
VCC
VSS
TSD Bias circuit
12bit ADC
Hall ch1
Hall ch2
Hall ch3
MUX
MON
VM
PGND
HD1_OUT
HA1_INP
HA1_INN
< CH1 > Hall amp 8bitDAC 2ch
6CH_SW
CH3 driver
OUT3_A
OUT3_B
HD2_OUT
HA2_INP
HA2_INN
< CH2 > Hall amp 8bitDAC 2ch
CH1 driver
OUT1_A
OUT1_B
AD2
TEMP
HD3_OUT
HA3_INN
HA3_INP
< CH3 > Hall amp 8bitDAC 2ch
CH2 driver
OUT2_A
OUT2_B

POWER SUPPLY SEQUENCE



Notes at the time of power-on

*1 Please apply VDD at the same time or before VCC.

*2 Please apply VCC at the same time or before VM.

(Please apply all powers with a stable voltage.)

Notes at the time of power-down

*1 Please power down VCC and VM at the same time.

*2 Please power down VDD at the same time or after power VCC.

Notes at the time of FW Initialization

*3 The periods of FW Initialization is depend on FW.

CPU initialize the registers of IIC during the periods of FW Initialization.

Consumption current

If not specified, VDD=1.8V,VCC=VM=2.8V Ta=25degreeC

Item	Symbol	Condition	Standard Value			Unit	Remarks
			min	typ	max		
VDD current	IVDln	EXCLK=27MHz PLL=162MHz,System Clock=32.4MHz Linear mode	-	10	-	mA	*1
VCC current	IVCln	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h,BTL_IS*DAC & AF_BTL setting Default.	-	4.7	7.05	mA	
VM current	IVMpw	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h PWM mode	-	1.2	1.8	mA	*2
VM current	IVMln	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h,BTL_IS*DAC & AF_BTL setting Default.	-	7.6	11.4	mA	

Note *1: These are reference data. These are depend on FW processing.

Note *2: These are reference,not guaranteed.

Electrical characteristics (POR threshold)

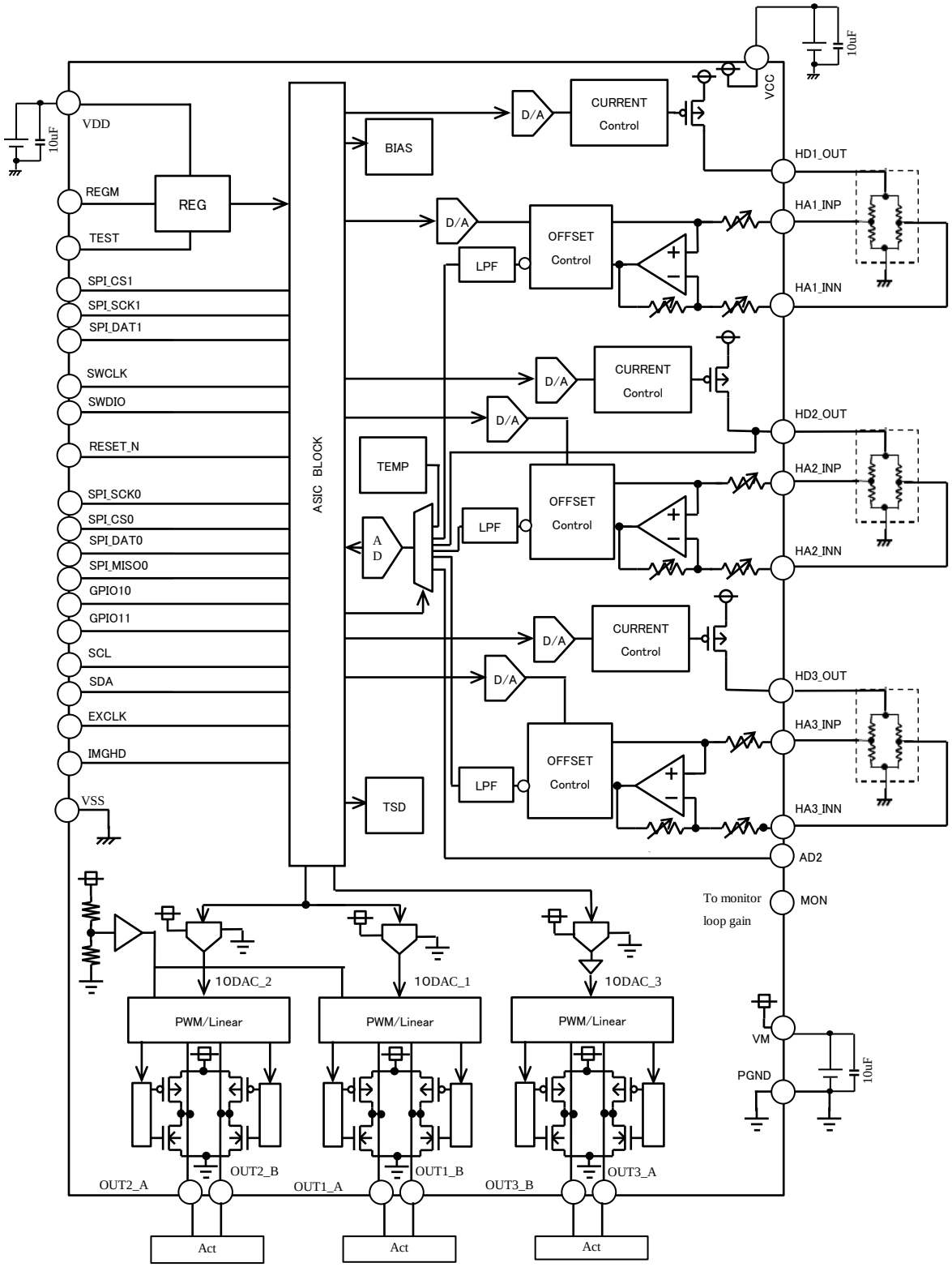
If not specified, Ta=25degreeC

Item	Symbol	Condition	Standard Value			Unit	Remarks
			min	typ	max		
UVP (Under Voltage Protect)							
PVO detect level	PVO	Check on VCC >Vcore	1.30	1.55	1.67	V	
LVI detect level	LVI	Check on VCC level	2.35	-	-	V	*1
POR detect level	POR	Check on VDD	1.30	1.60	1.68	V	

Note *1: These are reference , not guaranteed.

RAA305350MGBM
(Driver Block)

Example for circuit of Driver Block (Analog & Driver)



Electrical specification (Analog block) Ta=25 degrees C

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
12bit ADC	Resolution	RES	684uV/LSB @VCC=2.8V	—	12	—	bit	
	Liniearity minimum code	DRLAD	about 0.1V	—	—	080h	CODE	
	Liniearity maximum code	DRHAD	about VCC-0.1V	F7Fh	—	—	CODE	
	Zero scale input voltage	VINLAD		—	0	—	V	
	Full scale input voltage	VINHAD		—	VCC	—	V	
	Conversion time	TCAD		3.375	—	—	us	
	clock frequency	FCLK		—	—	16	MHz	
Hall Amplifier	Lo output voltage	VOLMN		—	—	0.10	V	
	Hi output voltage	VOHMN		VCC-0.1	—	—	V	
	Differential Gain accuracy	GHS	x20, x30, x40, x80 x120, x160, x100, x150, x7	-12	0	12	%	
	Output LPF cut-off frequency	BWHA	-3dB	—	10	—	kHz	∗1
Hall Amplifier offset adjusting 8bit DAC	Resolution	RES	10.9mV/LSB @VCC=2.8V	—	8	—	bit	
	Differential Nonlinearity	DNLDA8	guaranteed monotonic, IO=0mA DAC setting code DRLDA8～DRHDA8	-1	—	1	LSB	∗1
	Integral Nonlinearity	INLDA8	IO=0mA DAC setting code DRLDA8～DRHDA8	(Reference value) -2	—	(Reference value) 2	LSB	∗1
	Liniearity minimum code	DRLDA8	about 0.25V IO=0mA	—	—	15h	CODE	
	Liniearity maximum code	DRHDA8	about 2.75V IO=0mA	EBh	—	—	CODE	
	Zero scale output voltage	VOZSDA8	DAC setting code 00h, IO=0mA	—	—	0.1	V	
	Full scale output voltage	VOFSDA8	DAC setting code FFh, IO=0mA	VCC-0.1	—	—	V	
	Output response time	TCDA8	DRLDA8～DRHDA8	—	—	(Reference value) 5	us	∗1
Constant Current Amplifier	FET Tr minimum current	IIBMINIC	DAC setting code 00h VIN=0V, ISET[1:0]=01b	—	—	10	uA	
	FET Tr maximum current 1	IIBMAXIC1	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=00b	1.0	—	—	mA	
	FET Tr maximum current 2	IIBMAXIC2	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=01b	2.0	—	—	mA	
	Internal DAC linearity minimum code	DRLIDA8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	—	—	11h	CODE	
	Internal DAC linearity maximum code	DRHIDA8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	D6h	—	—	CODE	

Electrical specification (Driver block) Ta=25 degrees C

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
Linear Driver (CH1,2,3)	IS DAC Resolution	RESIS		-	10	-	bit	
	IS internal DAC linearity minimum code	DRLIDA10IS	RL=28ohm	—	—	C0h	CODE	*1
	IS internal DAC linearity maximum code	DRHIDA10IS	RL=28ohm	340h	—	—	CODE	*1

Note *1: These are reference , not guaranteed.

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
PWM driver (CH1,2,3)	On resistance IS	RONIS	Io=100mA, VM=2.8V Total of top and bottom resistance	-	3.6	5.8	ohm	*1
	Turn on time 1	TON1	Threshold 50%, Io=100mA IS slew rate setting=000b	-	0.3	0.45	µs	
	Turn off time 1	TOFF1	Threshold 50%, Io=100mA IS slew rate setting=000b	-	0.12	0.24	µs	
	Rise up time 1	Tr1	From 10% to 90%, Io=100mA IS slew rate setting=000b	-	0.13	0.52	µs	
	Fall downtime 1	Tf1	From 90% to 10%, Io=100mA IS slew rate setting=000b	-	0.05	0.10	µs	
	Turn on time 2	TON2	Threshold 50%, Io=100mA IS slew rate setting=110b	-	0.26	0.39	µs	*1
	Turn off time 2	TOFF2	Threshold 50%, Io=100mA IS slew rate setting=110b	-	0.12	0.24	µs	*1
	Rise up time 2	Tr2	From 10% to 90%, Io=100mA IS slew rate setting=110b	-	0.11	0.44	µs	*1
	Fall downtime 2	Tf2	From 90% to 10%, Io=100mA IS slew rate setting=110b	-	0.05	0.10	µs	*1
	Turn on time 3	TON3	Threshold 50%, Io=100mA IS slew rate setting=101b	-	0.24	0.36	µs	*1
	Turn off time 3	TOFF3	Threshold 50%, Io=100mA IS slew rate setting=101b	-	0.12	0.24	µs	*1
	Rise up time 3	Tr3	From 10% to 90%, Io=100mA IS slew rate setting=101b	-	0.08	0.32	µs	*1
	Fall downtime 3	Tf3	From 90% to 10%, Io=100mA IS slew rate setting=101b	-	0.05	0.10	µs	*1

Note *1: These are reference , not guaranteed.

RAA305350MGBM
(Controller Block)

Controller Block outline

Block diagram

Block diagram is shown in below.

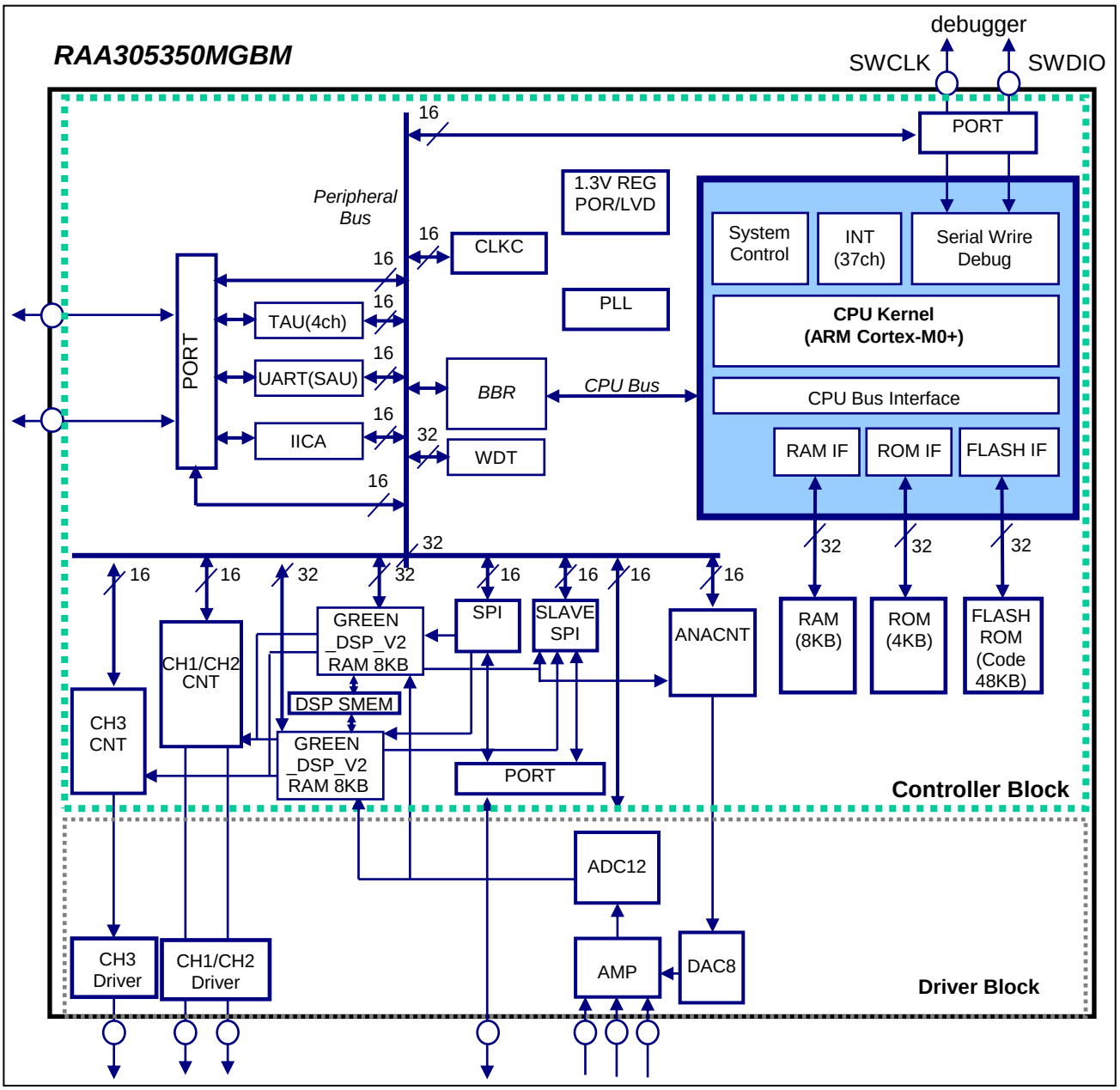
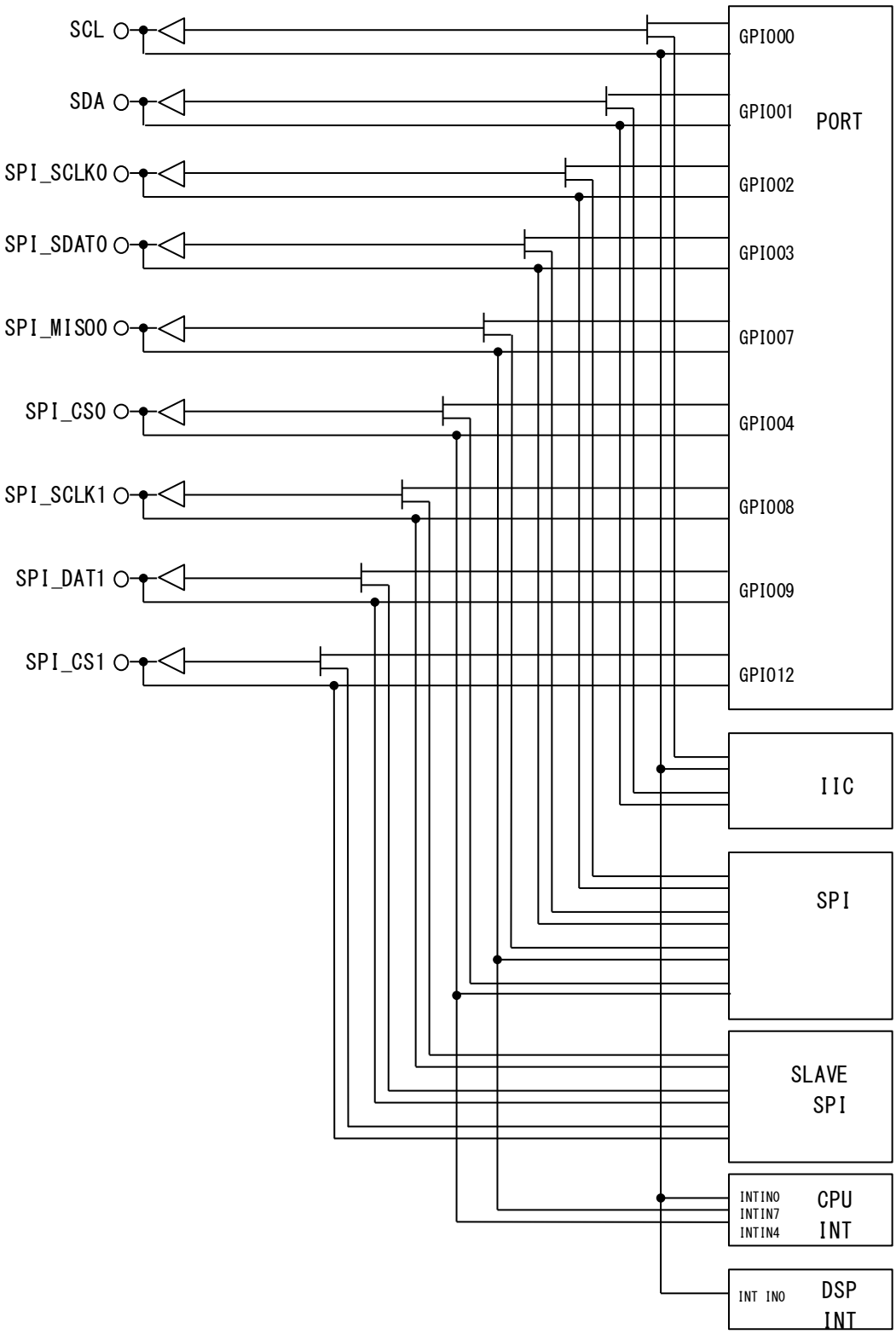


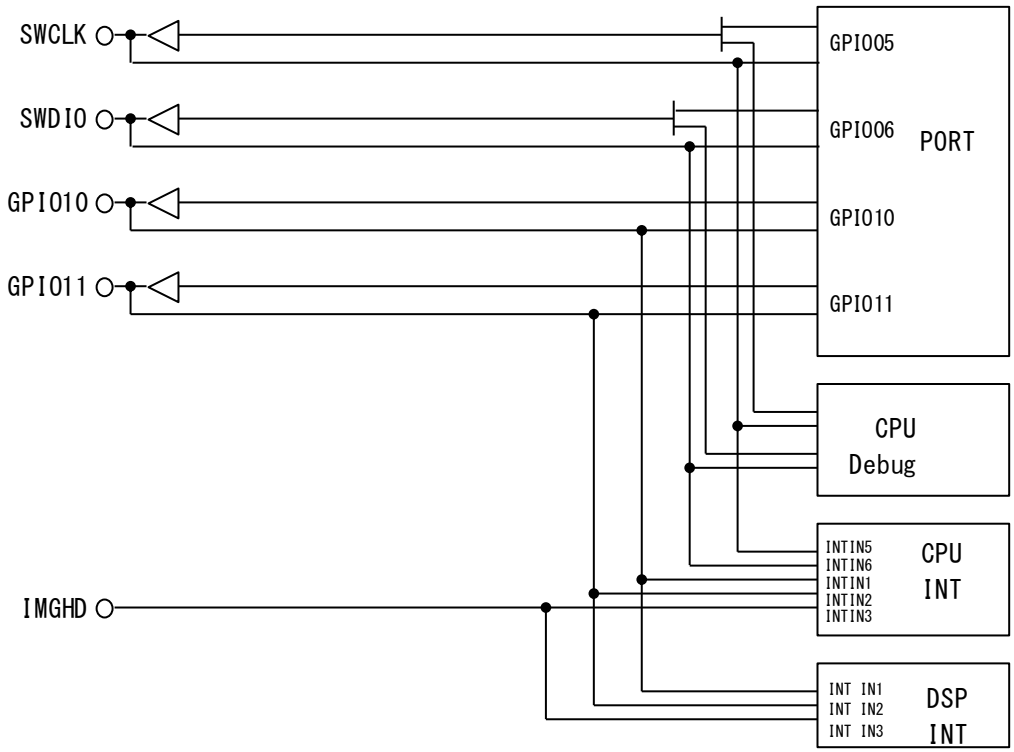
Figure 1.1 RAA305350MGBM Block diagram

BBR:Bus BRidge
TAU:Timer Array Unit

Pin connection (1/2)



Pin connection (2/2)



Controller Features

controller peripheral I/O Features shown in Table (1)

Function block	Features	
Interrupt controller (INT)	· Internal Interrupts	: 37 sources
	· External interrupts	: 8 sources
	· ICUIN input sense	: Edge sense (rise edge, fall edge, both edges)
	· Priority	: Programable
TIMER ARRAY UNIT(TAU)	· Channels	: 4ch
	· Count bit	: 16 bits counter, down counting
	· Timer scale	: $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
General purpose I/O & Pin control (PORT)	· GPIO number of lines	: 12 lines (GPIO)
	· I/O pins	: Can be set to each I/O pin using the corresponds input and output control register bits. : Can be select to each I/O from GPIO and peripheral module Pin mode register 0/1/2/3.
	· I/O pins control	: Each pins can be changed GPIO and other peripheral functions with setting the operation mode register.
	· I/O pins pull-up	: Enables and disables the pull-up resistors.
Serial Peripheral Interface (SPI)	· Number of channels	: 1 channel
	· Character length	: 8 bits
	· Order of transfer	: MSB first or LSB first
	· Shift clock	: Internal or external shift clock
	· Internal shift clock source	: $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
	· Baud rate count	: 2-256
	· Transmit interrupt factor	: Transmit buffer empty or Transmit end
	· Receive error detection	: Overrun
	· Chip Select	: Chip select signal
	· DSP register access	: Registers are accessible from CPU
Slave Serial Peripheral Interface (SLAVE SPI)	· Number of channels	: 1 channel
	· Character length	: 8 bits
	· Order of transfer	: MSB first
	· Shift clock	: external shift clock
	· Transmit interrupt factor	: Transmit end
	· Receive/Send buffer	: 1Byte address buffer(Receive) and 6 Byte data buffer(Send)
	· Chip Select	: Chip select signal
	· DSP register access	: Registers are accessible from CPU

controller peripheral I/O Features shown in Table (2)

Function block	Features	
Universal asynchronous Receiver Transmitter (UART)	·Channels	: 1 channel
	·Character length	: 7/8/9 -bit length can be selected
	·Transfer order	: MSB and LSB first can be selected
	·Stop bit length	: 1 or 2 bit can be selected
	·Parity check	: Can be enabled or disabled
	·Attribute of parity check	: Even or Odd parity can be selected
	·Internal clock source	: Dividable range = : $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
	·Baud rate counter	: Maximum 2-256
	·Transmit interrupt factor	: Transmit buffer empty or Transmit end can be selected. Error interrupt also.
	·Error detection	: Framing error, Parity error, Overrun error.
Clock /PLL/ System control	·Clock source	: External Input (EXCLK)
	·SYSTEM/DSP clocks	: 32.4MHz max
	·PWM clocks	: 162MHz max
	·Standby Function	: SLEEP, DEEP-SLEEP
	·PLL clock(=PWM clocks)	: MAX : 162MHz
	·PLL control	: PLL can be stop.
	·OIS module clock control	: OIS module clock control can be stop
Multi Master & Slave SERIAL INTERFACE IICA (IICA)	·Channels	: 1 channel
	·Clock frequency	: Standard mode (fastest transfer rate: 100 kbps) : Fast mode (fastest transfer rate: 400 kbps) : Fast mode+ (fastest transfer rate: 1 Mbps)
	·Transmit interrupt factor	: Transfer end interrupt
	·Error detection	: Overrun error Parity error (ACK error)
CH1,CH2 Control (OISCNT)	·Image stabilizer drive function	: 2 channel PWM or Linear (H-bridge)
	·DSP register access	: Registers are accessible through CPU Bus.
CH3 Control (AFCNT)	·Auto focus drive function	: 1 channel PWM or Linear (H-bridge)
	·DSP register access	: Registers are accessible through CPU Bus.

controller peripheral I/O Features shown in Table (3)

Function block	Features	
DSP (GREEN_DSP_V2 1, 2)	· Channels	: 2 channels
	· Arithmetic operation	: Multiplication Signed 32 bits * Signed 32 bits = Signed 32 bits Multiplication results (64 bits) can be shifted right any number of bits : Addition/ Substruct Signed 32 bits + Signed 32 bits = Signed 32 bits Signed 32 bits - Signed 32 bits = Signed 32 bits Internally calculated with 33bits precision. : Limit calculation Upper-/lower-limits can be set. : Capable to generate an interrupt to the CPU at program halt.
	· Interrupt requests	: When program halts: Executes the STOP, break, and undefined instructions.
Shared Memory (DSP SMEM)	·Memory Capacity	: 16byte (GREEN_DSP_V2 1->GREEN_DSP_V2 2) 16byte (GREEN_DSP_V2 2->GREEN_DSP_V2 1)
	· Interrupt requests (Software interrupt)	: GREEN_DSP_V2 1->GREEN_DSP_V2 2 GREEN_DSP_V2 2->GREEN_DSP_V2 1
Analog Control (ANACNT)	· AMP,DAC8 control	: Control register
	· DSP register access	: Registers are accessible through CPU Bus.
12bit ADC Control (ADC12)	· Resolution	: 12bits
	· Channels	: 6ch
	· Conversion mode	: Single mode, Scan mode
	· DSP register access	: Registers are accessible through CPU Bus.

Electrical characteristics (Controller block) Ta=25 degrees C

DC characteristics

If not specified VDD=1.8V, VCC=VM=2.8V, Ta=25 degrees C

Item	Symbol	Conditions	Limit			Unit	Remarks
			Min	Typ	Max		
'H' output voltage	VOH	IOH=-2mA	VDD*0.8	-	VDD	V	note1
'L' output voltage	VOL	IOL=2mA	0		VDD*0.2	V	note1
'H' input current	IIH	VI=VDD	-	-	1	uA	note2
'L' input current	IIL	VI=0V	-	-	-1	uA	note2
Pull-up resistance	Rup		10	-	200	Kohm	note3
'H' input voltage	VIH		VDD*0.7	-	VDD	V	-
'L' input voltage	VIL		0	-	VDD*0.3	V	-

note1. correspondence terminal: SCL, SDA, SPI_SCK0, SPI_DAT0, SPI_MISO0, SPI_CS0, SPI_SCK1, SPI_DAT1, SPI_CS1, SWCLK, SWDIO, GPIO10, GPIO11
note2. in condition that pull-up resistance is not connected. (The built-in pull-up resistor is disabled by the F/W.)
note3. correspondence terminal: SPI_SCK1, SPI_DAT1, SPI_CS1, SWCLK, SWDIO, GPIO10, GPIO11

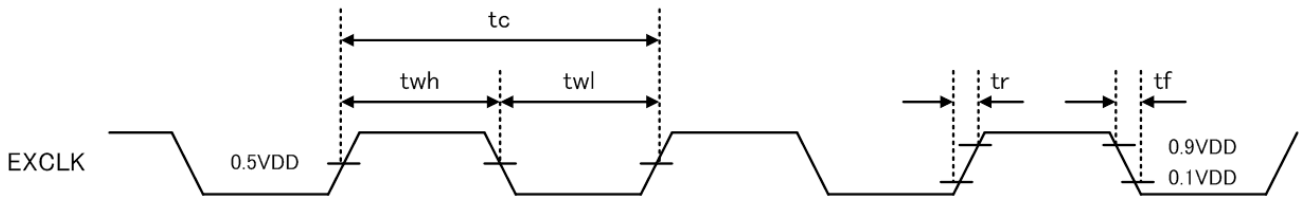
Electrical characteristics (Controller block)　Ta=25 degrees C

AC characteristics

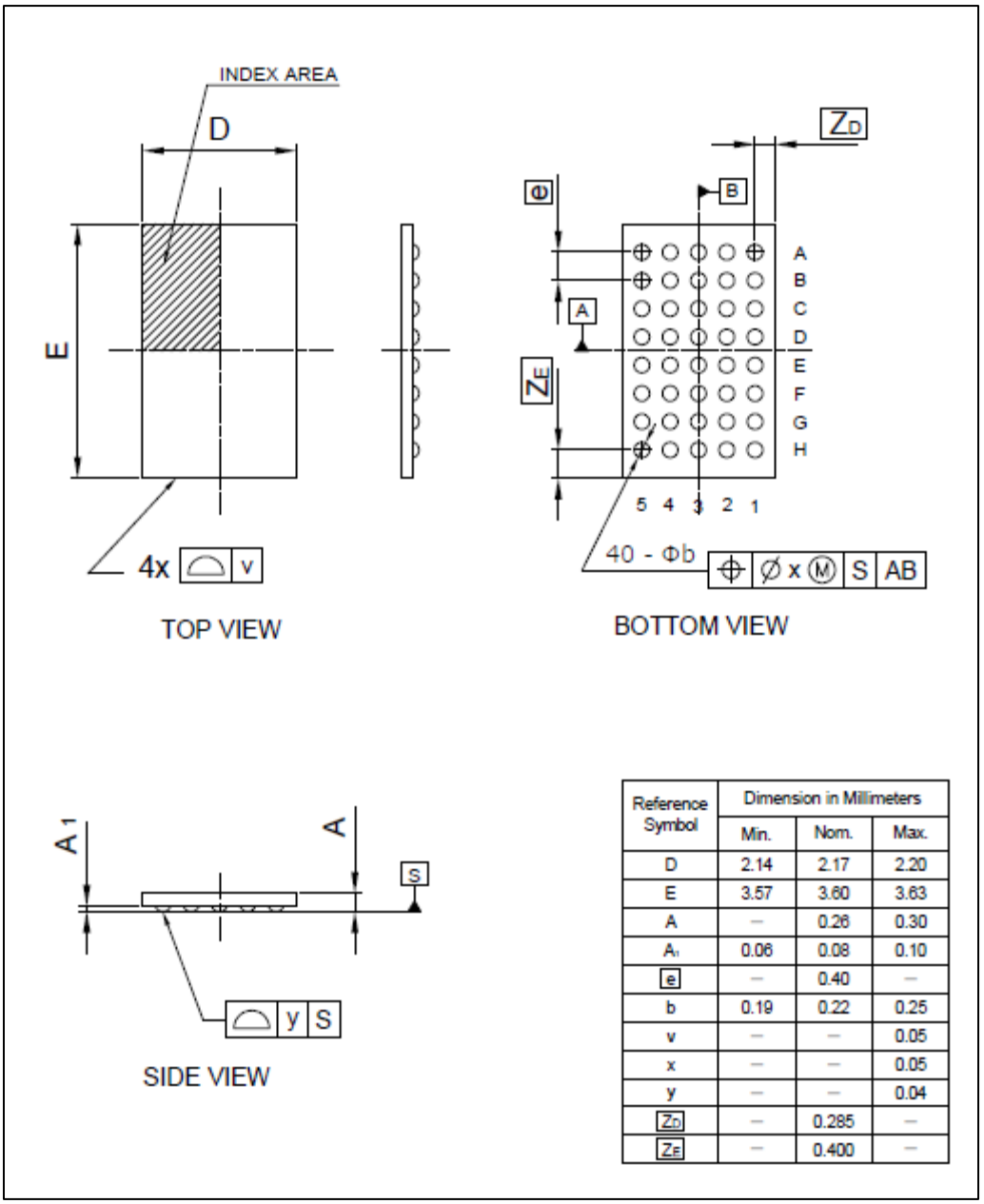
(1) EXTERNAL CLOCK (CLOCK)

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
Input Frequency	fclk	-	6	29	MHz	-
Input 'H' pulse width	twh	＞ 0.5VDD	14	-	ns	-
Input 'L' pulse width	twl	＜ 0.5VDD	14	-	ns	-
Input rise time	Tr	VDD voltage 10% to 90%	-	2	ns	-
Input fall time	Tf	VDD voltage 10% to 90%	-	2	ns	-
Cycle-to-cycle period jitter	tjit(CC)	-	-	2	%	-
Period Jitter	tjit(per)	-	-4	4	%	-



Outline drawing



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	2.14	2.17	2.20
E	3.57	3.60	3.63
A	—	0.26	0.30
A_1	0.06	0.08	0.10
e	—	0.40	—
b	0.19	0.22	0.25
v	—	—	0.05
x	—	—	0.05
y	—	—	0.04
ZD	—	0.285	—
ZE	—	0.400	—

Revision History

Rev	Date	Description	
		Page	Summary
Rev 1.06	16th.Mar.2021	-	New

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1.Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2.Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3.Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4.Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5.Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6.Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7.Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8.Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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