R1LV0216BSB

2Mb Advanced LPSRAM (128k word x 16bit)

R10DS0273EJ0101
Rev.1.01
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Description

The R1LV0216BSB is a family of low voltage 2-Mbit static RAMs organized as 131,072-word by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV0216BSB has realized higher density, higher performance and low power consumption. The R1LV0216BSB is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. The R1LV0216BSB has been packaged in 44-pin TSOP.

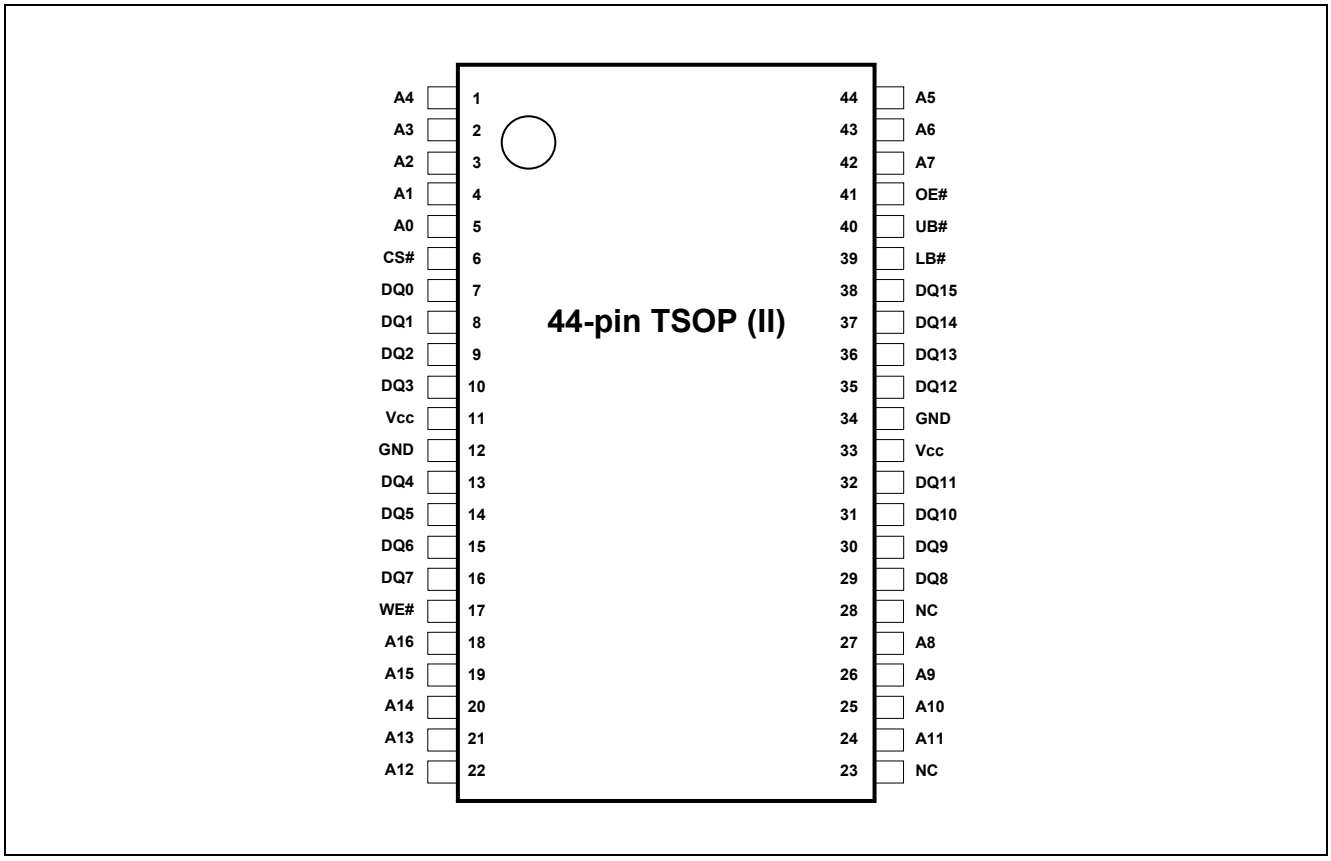
Features

- Single 2.7V~3.6V power supply
- Small stand-by current: 1µA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS#, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LV0216BSB-5SI#B1	55 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray
R1LV0216BSB-5SI#S1				Embossed tape

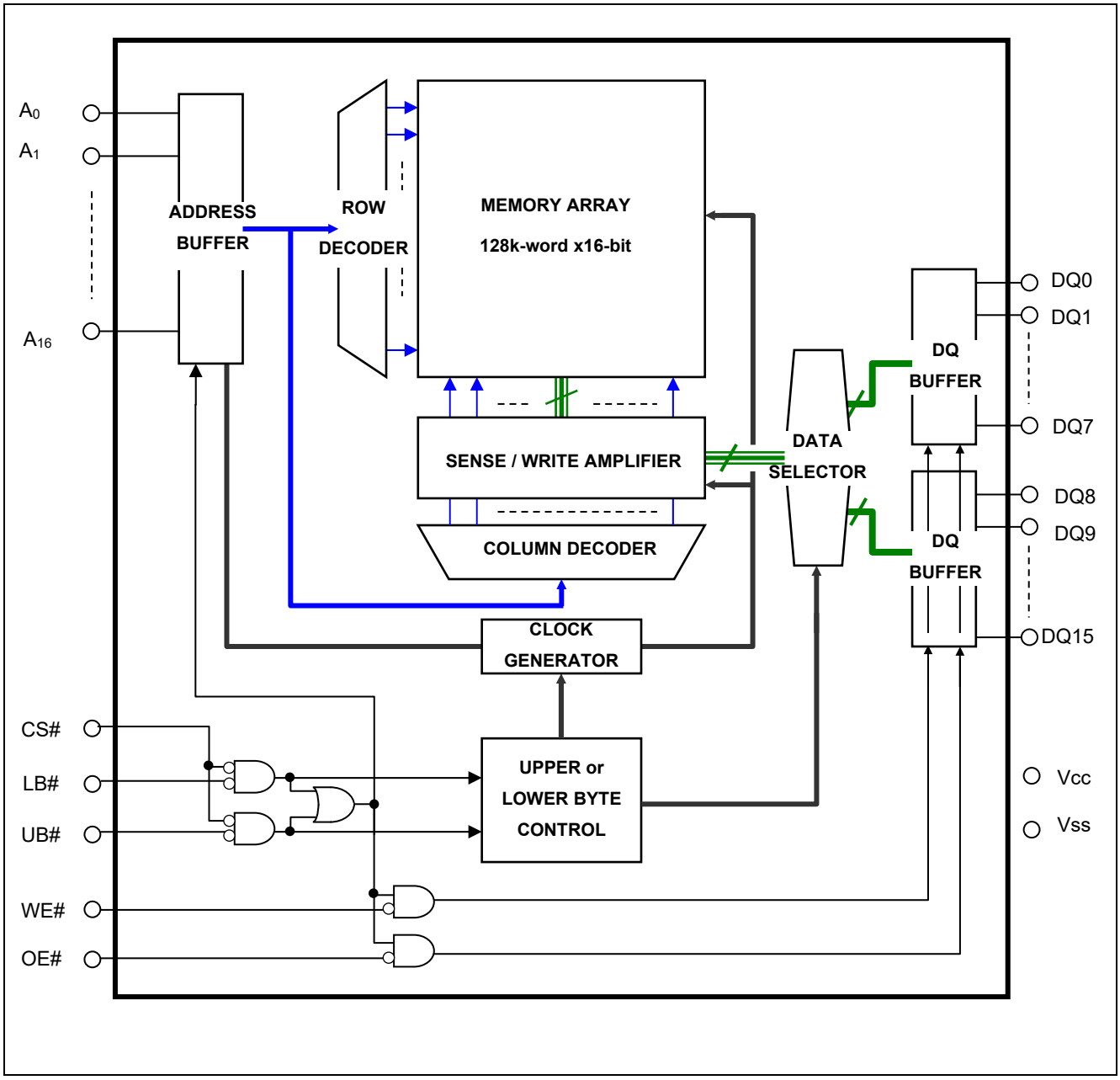
Pin Arrangement



Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A16	Address input
DQ0 to DQ15	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable
NC	Non connection

Block Diagram



Operation Table

CS#	LB#	UB#	WE#	OE#	DQ0~7	DQ8~15	Operation
H	X	X	X	X	High-Z	High-Z	Stand-by
X	H	H	X	X	High-Z	High-Z	Stand-by
L	L	H	L	X	Din	High-Z	Write in lower byte
L	L	H	H	L	Dout	High-Z	Read in lower byte
L	L	H	H	H	High-Z	High-Z	Output disable
L	H	L	L	X	High-Z	Din	Write in upper byte
L	H	L	H	L	High-Z	Dout	Read in upper byte
L	H	L	H	H	High-Z	High-Z	Output disable
L	L	L	L	X	Din	Din	Word write
L	L	L	H	L	Dout	Dout	Word read
L	L	L	H	H	High-Z	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	V_T	-0.5[*1] to Vcc+0.5[*2]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)
2. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	Vcc	2.7	3.0	3.6	V	
	Vss	0	0	0	V	
Input high voltage	V_{IH}	2.2	-	Vcc+0.3	V	
Input low voltage	V_{IL}	-0.3	-	0.6	V	1
Ambient temperature range	Ta	-40	-	+85	°C	

Note 1. –3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$\lvert I_{LI} \rvert$	-	-	1	µA	Vin = Vss to Vcc
Output leakage current	$\lvert I_{LO} \rvert$	-	-	1	µA	CS# = LB# = UB# = V_{IH} or OE# = V_{IH}, $V_{I/O}$ = Vss to Vcc
Average operating current	I_{CC1}	-	15	25	mA	Min. cycle, duty =100%, $I_{I/O}$ = 0mA, CS# = V_{IL}, Others = V_{IH}/V_{IL}
	I_{CC2}	-	2	5	mA	Cycle =1µs, duty =100%, $I_{I/O}$ = 0mA, CS# ≤ 0.2V, V_{IH} ≥ Vcc-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	-	-	0.5	mA	(1) CS# = V_{IH}, Others = V_{IH}/V_{IL} or (2) LB# = UB# = V_{IH}, Others = V_{IH}/V_{IL}
Standby current	I_{SB1}	-	1*1	2	µA	~+25°C — Vin = Vss to Vcc, (1) CS# ≥ Vcc-0.2V or (2) LB# = UB# ≥ Vcc-0.2V, CS# ≤ 0.2V
		-	-	3	µA	~+40°C
		-	-	8	µA	~+70°C
		-	-	10	µA	~+85°C
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -0.5mA
	V_{OH2}	Vcc - 0.5	-	-	V	I_{OH} = -0.05mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.

Capacitance

(Vcc = 2.7V ~ 3.6V, f = 1MHz, Ta = -40 ~ +85°C)

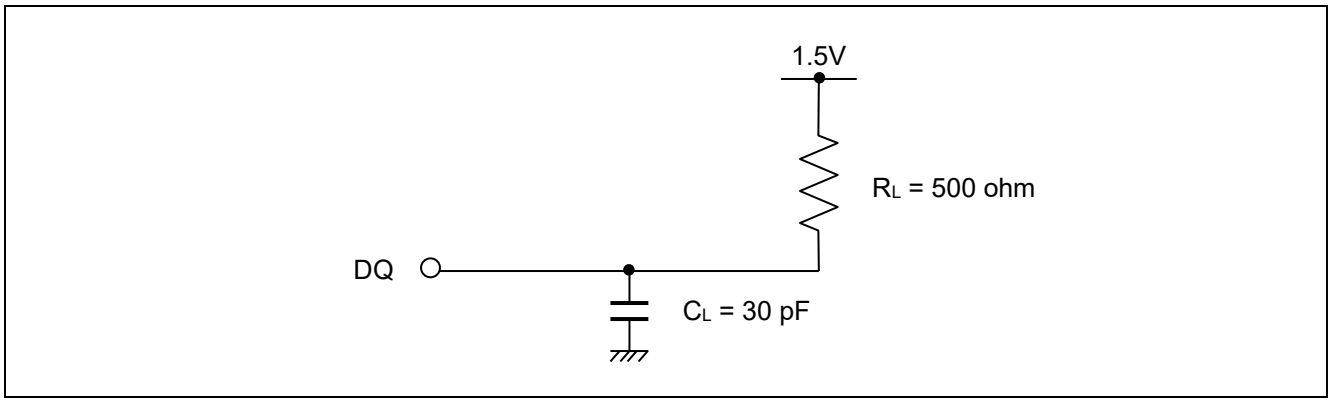
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	8	pF	Vin =0V	1
Input / output capacitance	$C_{I/O}$	-	-	10	pF	$V_{I/O}$ =0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels: VIL = 0.4V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55	-	ns	
Address access time	t_{AA}	-	55	ns	
Chip select access time	t_{ACS}	-	55	ns	
Output enable to output valid	t_{OE}	-	30	ns	
Output hold from address change	t_{OH}	10	-	ns	
LB#, UB# access time	t_{BA}	-	55	ns	
Chip select to output in low-Z	t_{CLZ}	10	-	ns	2,3
LB#, UB# enable to low-Z	t_{BLZ}	10	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ}	0	20	ns	1,2,3
LB#, UB# disable to high-Z	t_{BHZ}	0	20	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2,3

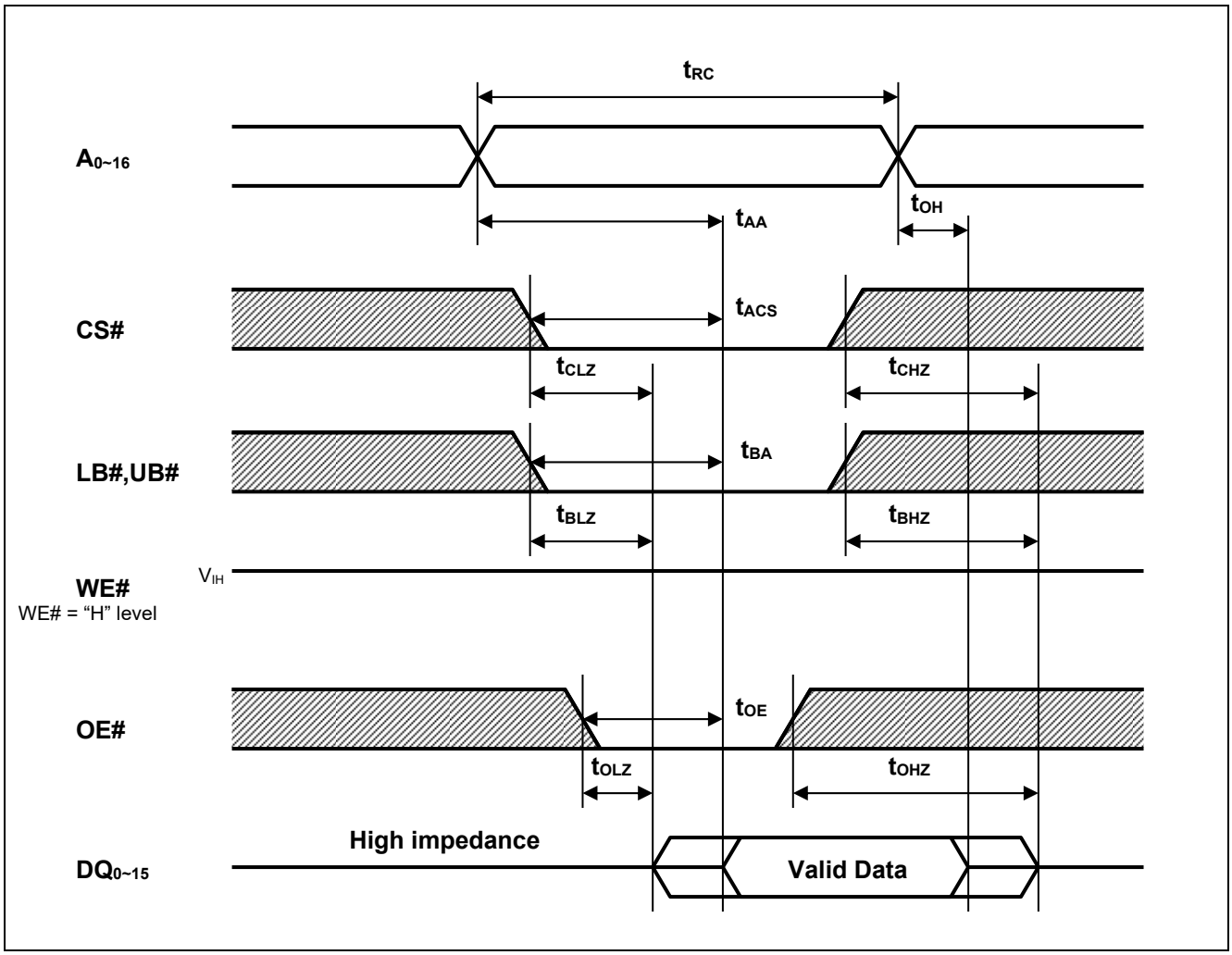
Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	-	ns	
Address valid to end of write	t_{AW}	50	-	ns	
Chip select to end of write	t_{CW}	50	-	ns	5
Write pulse width	t_{WP}	45	-	ns	4
LB#, UB# valid to end of write	t_{BW}	50	-	ns	
Address setup time	t_{AS}	0	-	ns	6
Write recovery time	t_{WR}	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	ns	
Data hold from write time	t_{DH}	0	-	ns	
Output enable from end of write	t_{OW}	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	ns	1,2

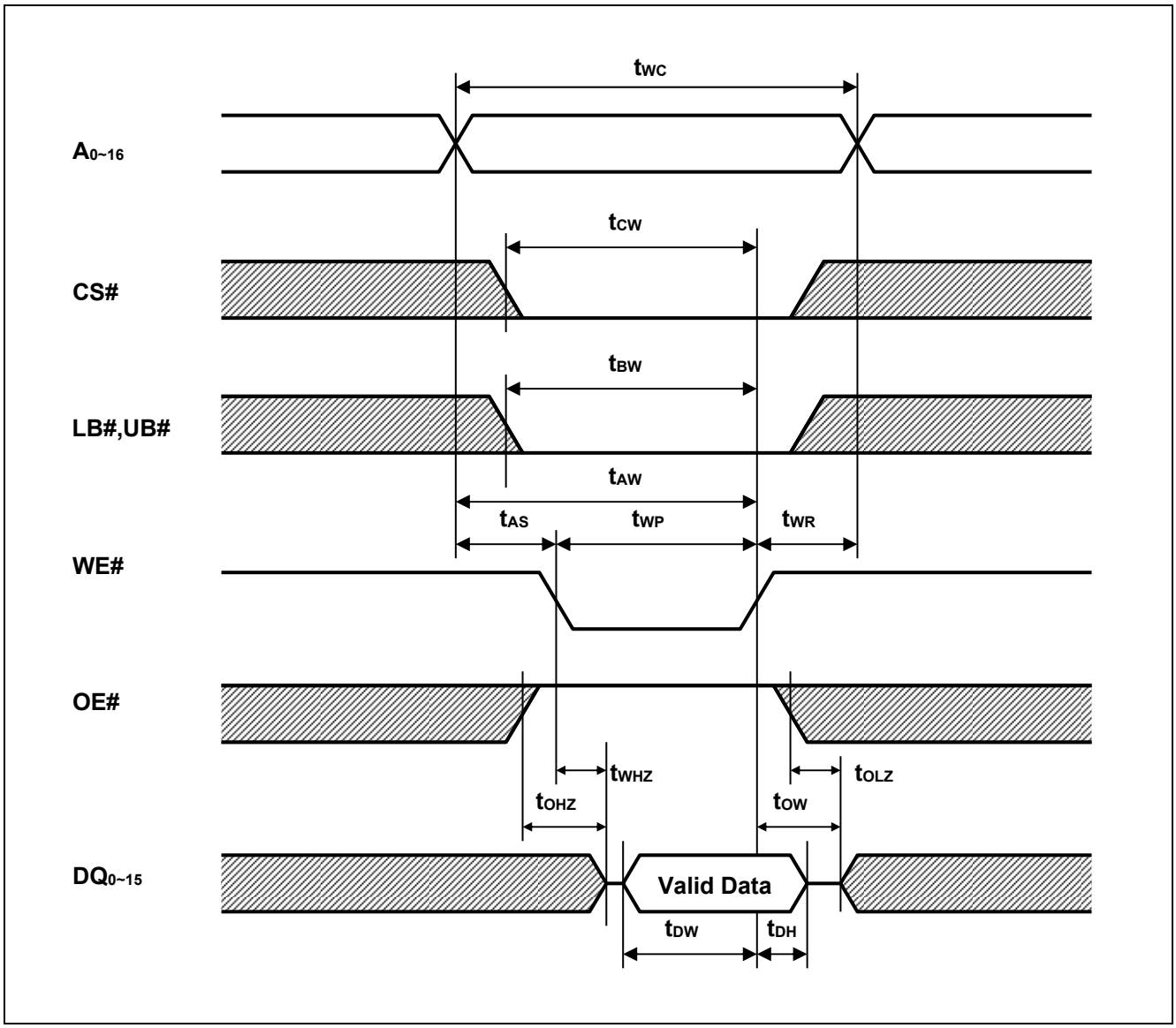
Note
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
   A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low.
   A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.
   t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS# going low to end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS#, WE#, LB# or UB# going high to the end of write cycle.
8. Don’t apply inverted phase signal externally when DQ pin is output mode.

Timing Waveforms

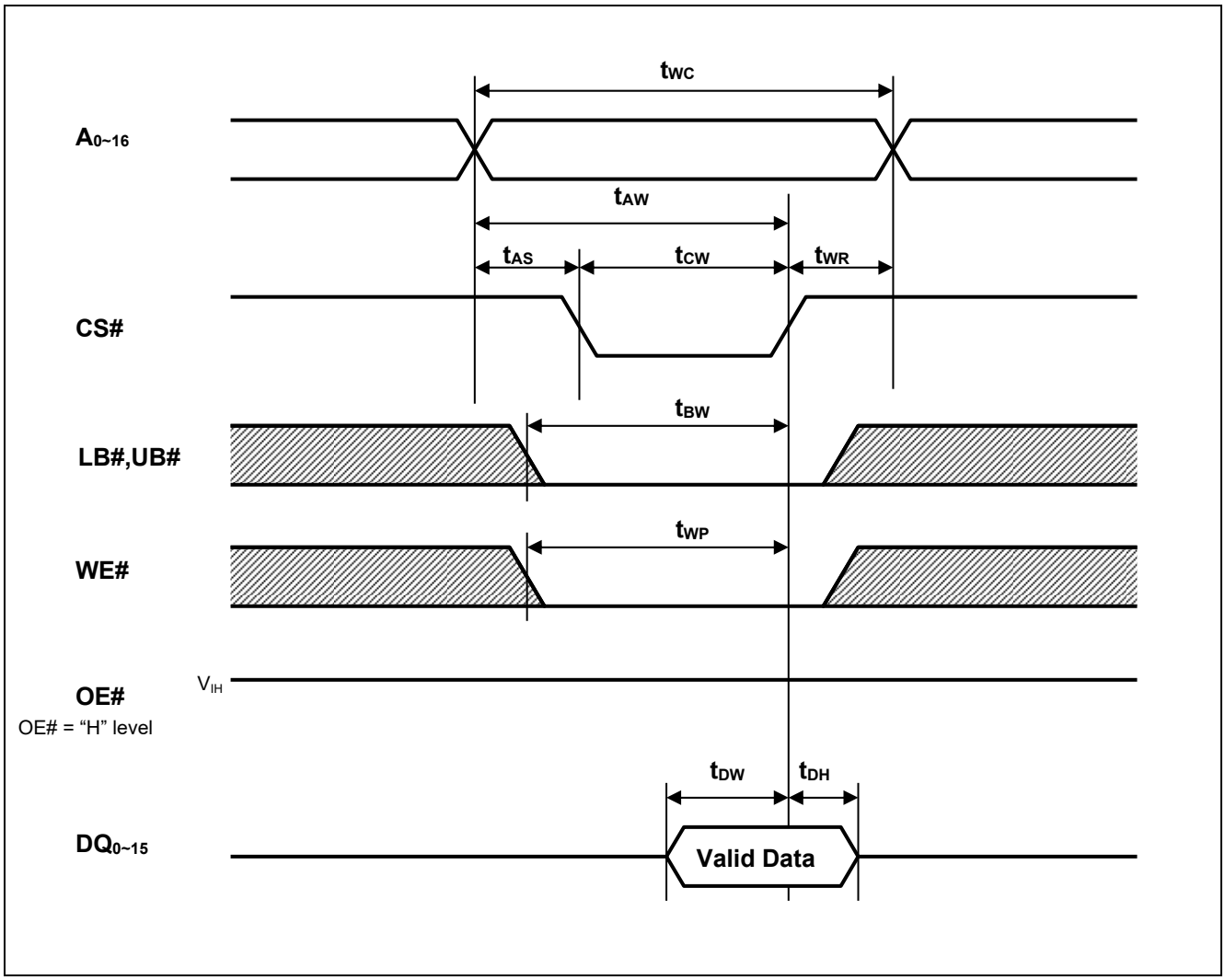
Read Cycle



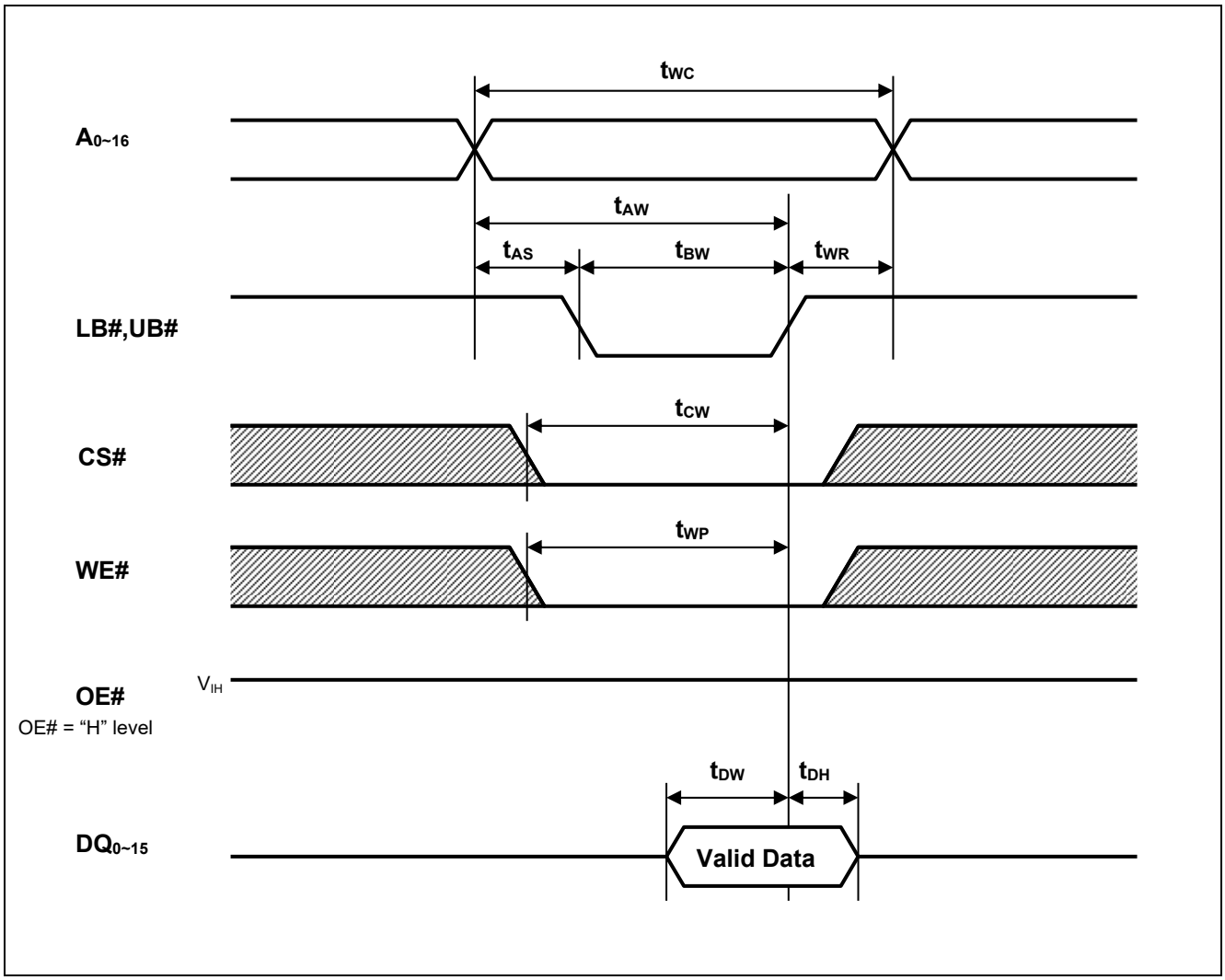
Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS# CLOCK)



Write Cycle (3) (LB#, UB# CLOCK)



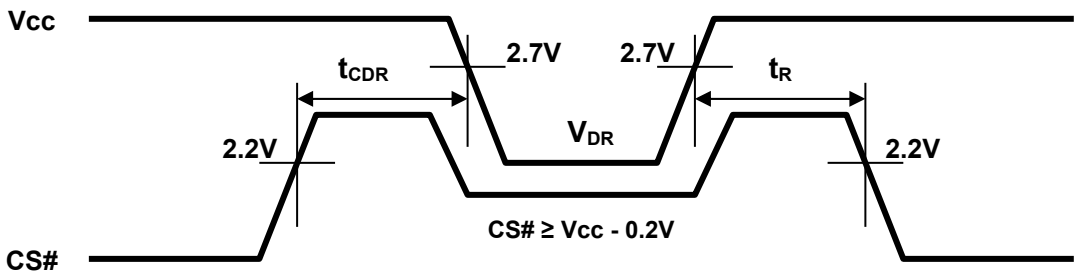
Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*2]	
V_{CC} for data retention	V_{DR}	2.0	-	3.6	V	Vin ≥ 0V, (1) CS# ≥ Vcc-0.2V or (2) LB# = UB# ≥ Vcc-0.2V, CS# ≤ 0.2V	
Data retention current	I_{CCDR}	-	1[*1]	2	µA	~+25°C	Vcc=3.0V, Vin ≥ 0V, (1) CS# ≥ Vcc-0.2V or (2) LB# = UB# ≥ Vcc-0.2V, CS# ≤ 0.2V
		-	-	3	µA	~+40°C	
		-	-	8	µA	~+70°C	
		-	-	10	µA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

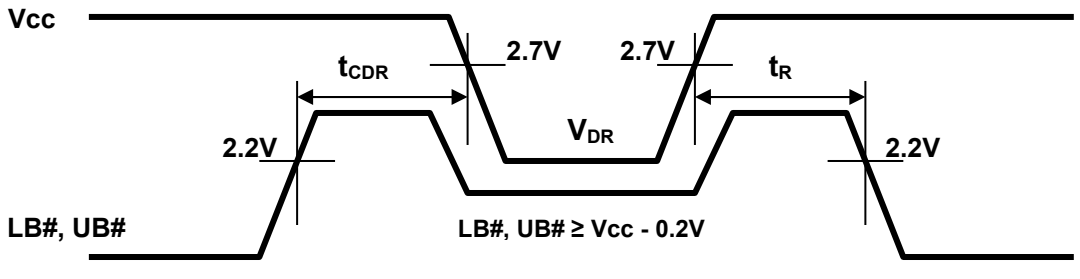
Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.
2. CS# controls address buffer, WE# buffer, OE# buffer, LB# buffer, UB# buffer and Din buffer. If CS# controls data retention mode, Vin levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms

(1) CS# Controlled



(2) LB#, UB# Controlled



Revision History	R1LV0216BSB Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	-	First Edition issued
1.01	2020.2.20	Last page	Updated the Notice to the latest version

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