

# NP90N04VDK

40 V – 90 A – N-channel Power MOS FET  
 Application: Automotive

R07DS1017EJ0200  
 Rev.2.00  
 May 24, 2018

## Description

The NP90N04VDK is N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

- Super low on-state resistance  
 $R_{DS(on)} = 2.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 45 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 3900 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

## Ordering Information

Part No.	Lead Plating	Packing		Package
NP90N04VDK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP90N04VDK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 90$	A
Drain Current (pulse) *1, 3	$I_{D(pulse)}$	$\pm 360$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	147	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.2	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *2, 3	$I_{AR}$	37	A
Repetitive Avalanche Energy *2, 3	$E_{AR}$	136	mJ

## Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3	1.02	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$ *3	125	$^\circ\text{C/W}$

Notes: \*1  $T_C = 25^\circ\text{C}$ ,  $P_w \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

\*3 Not subject of production test. Verified by design/characterization.

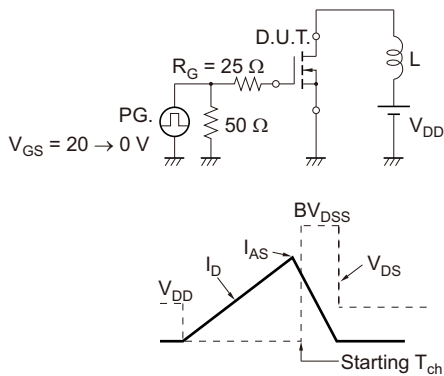
Electrical Characteristics (T<sub>A</sub> = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	1.5	1.8	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	44	88	—	S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 45 A
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>	—	2.35	2.80	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 45 A
	R <sub>DS(on)2</sub>	—	3.00	6.00	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 23 A
Input Capacitance *2	C <sub>iss</sub>	—	3900	5850	pF	V <sub>DS</sub> = 25 V V <sub>GS</sub> = 0 V f = 1 MHz
Output Capacitance *2	C <sub>oss</sub>	—	530	800	pF	
Reverse Transfer Capacitance *2	C <sub>rss</sub>	—	200	360	pF	
Turn-on Delay Time *2	t <sub>d(on)</sub>	—	18	40	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 45 A V <sub>GS</sub> = 10 V R <sub>G</sub> = 0 Ω
Rise Time *2	t <sub>r</sub>	—	8	21	ns	
Turn-off Delay Time *2	t <sub>d(off)</sub>	—	71	142	ns	V <sub>DD</sub> = 32 V V <sub>GS</sub> = 10 V I <sub>D</sub> = 90 A
Fall Time *2	t <sub>f</sub>	—	9	23	ns	
Total Gate Charge *2	Q <sub>G</sub>	—	68	102	nC	V <sub>DD</sub> = 32 V V <sub>GS</sub> = 10 V I <sub>D</sub> = 90 A
Gate to Source Charge	Q <sub>GS</sub>	—	17	—	nC	
Gate to Drain Charge	Q <sub>GD</sub>	—	11	—	nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>	—	0.9	1.5	V	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	—	43	—	ns	I <sub>F</sub> = 90 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	—	59	—	nC	di/dt = 100 A/μs

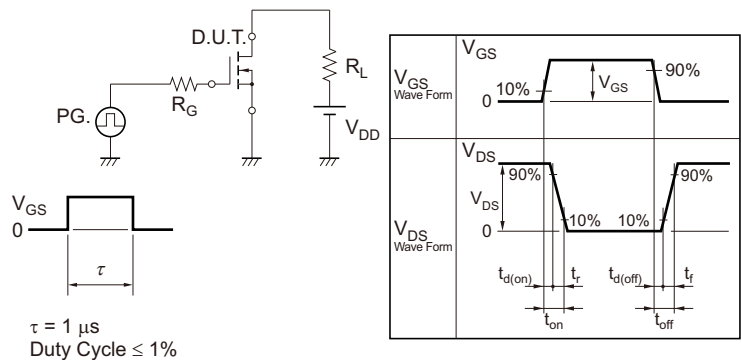
Note: \*1 Pulsed test

Note: \*2 Not subject of production test. Verified by design/characterization.

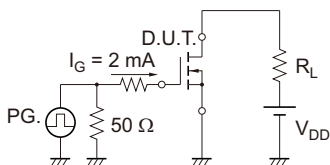
TEST CIRCUIT 1 AVALANCHE CAPABILITY



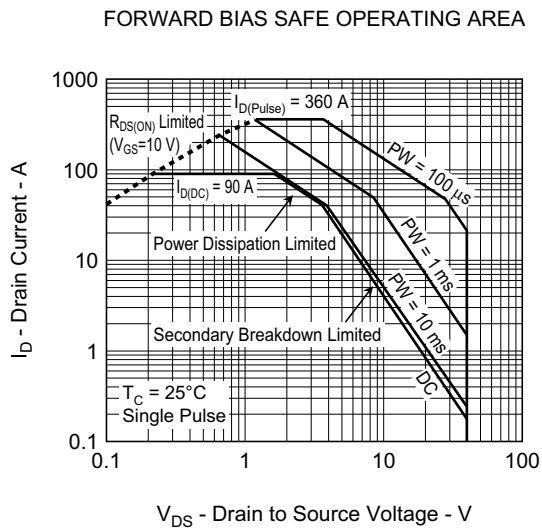
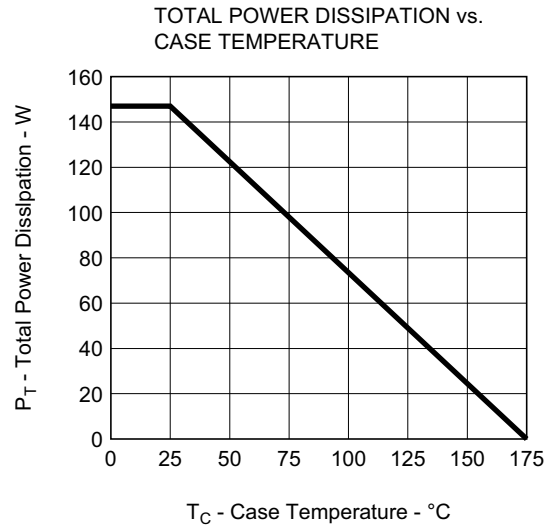
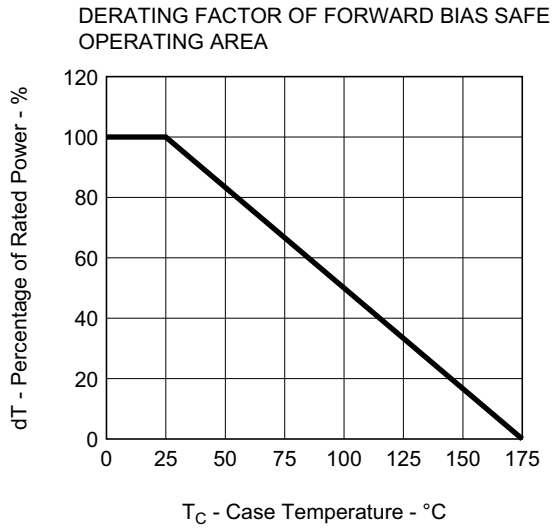
TEST CIRCUIT 2 SWITCHING TIME



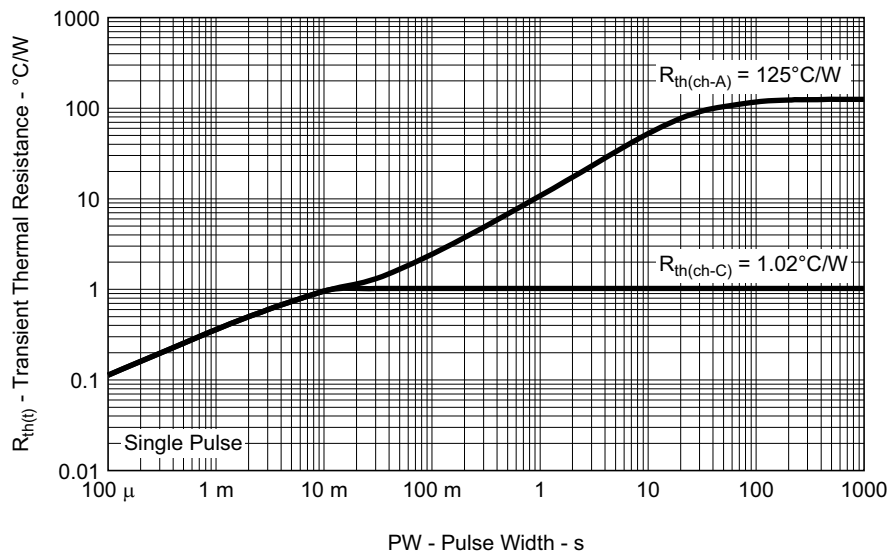
TEST CIRCUIT 3 GATE CHARGE



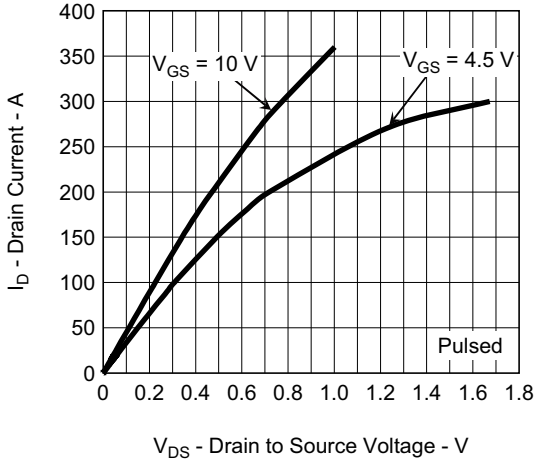
Typical Characteristics (T<sub>A</sub> = 25°C)



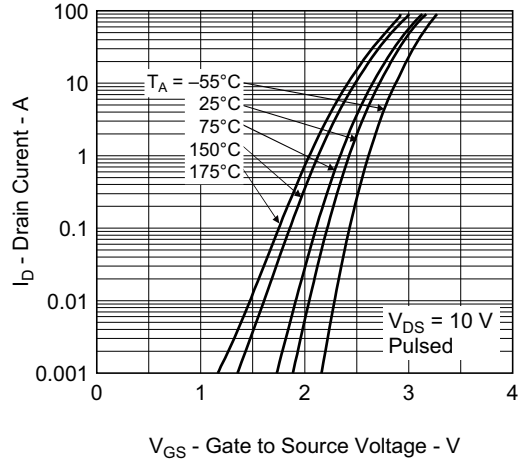
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



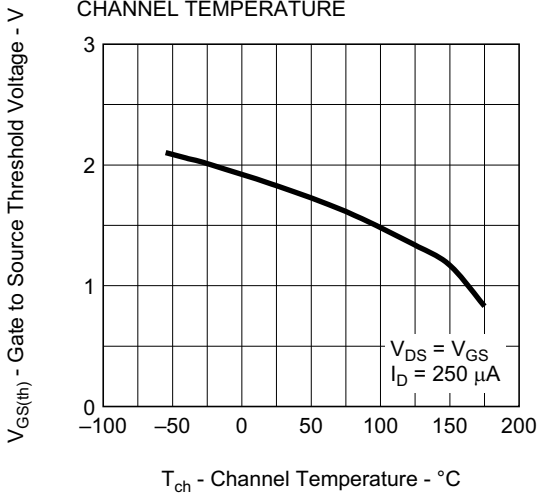
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



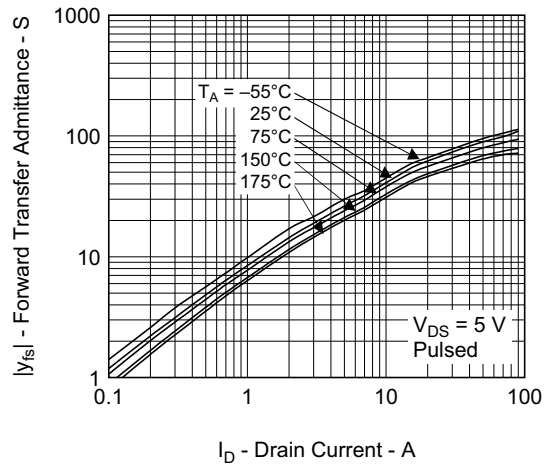
FORWARD TRANSFER CHARACTERISTICS



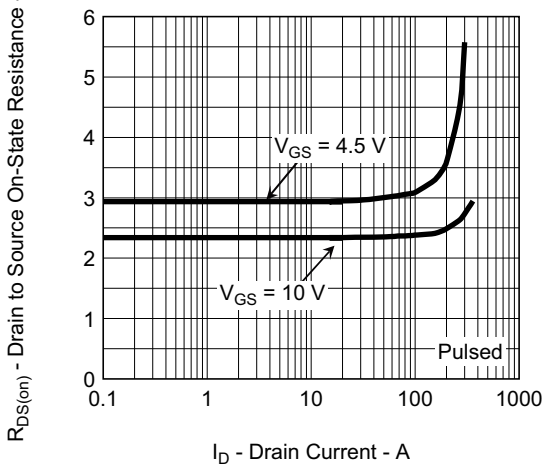
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



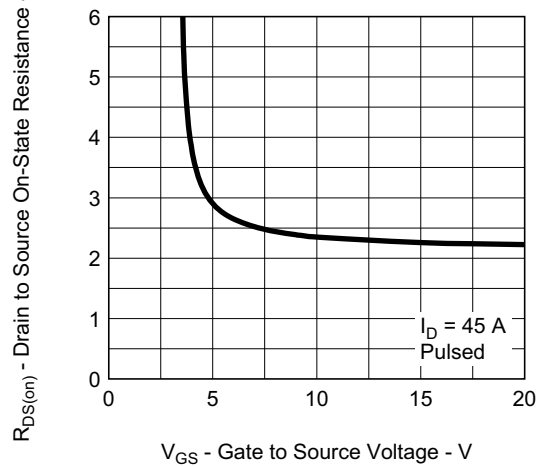
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



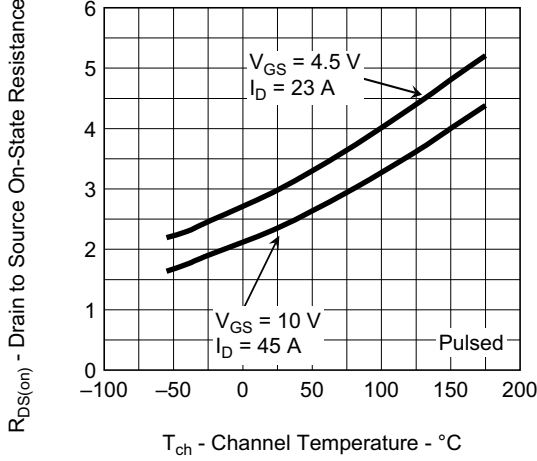
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



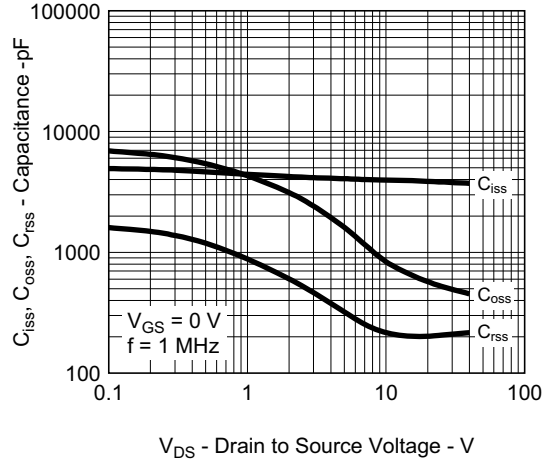
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



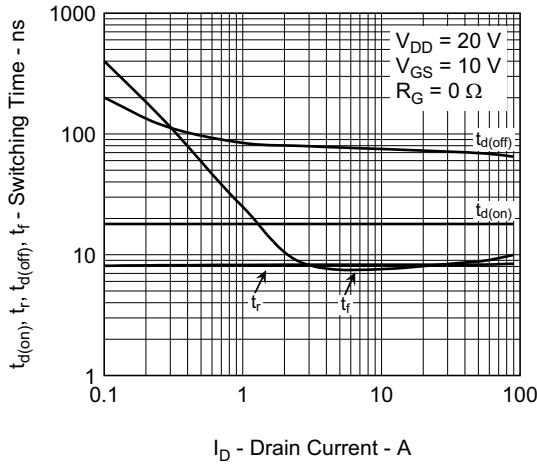
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



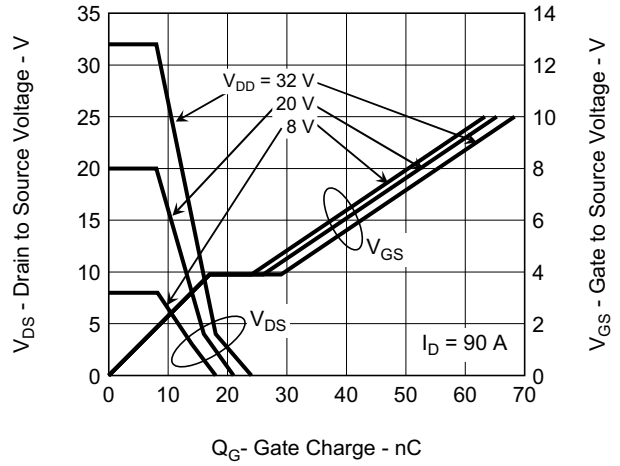
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



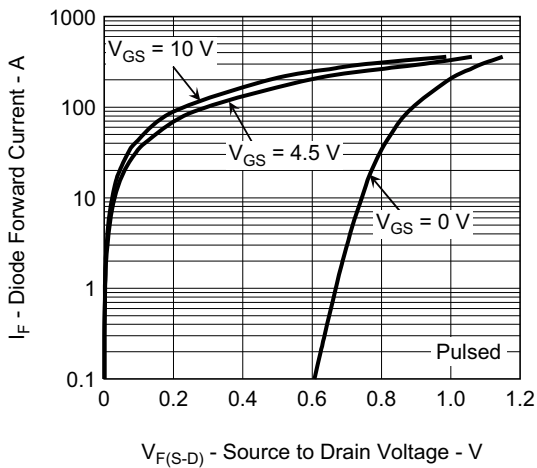
SWITCHING CHARACTERISTICS



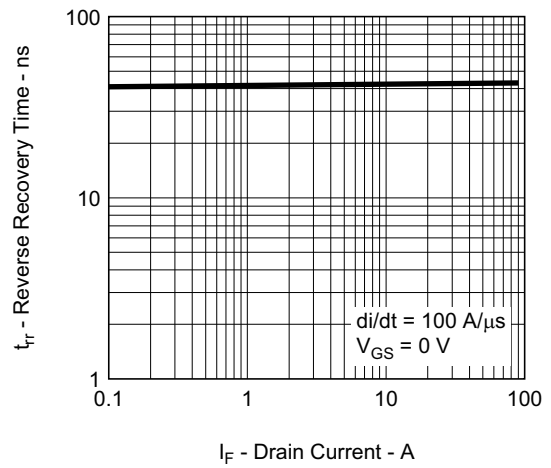
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

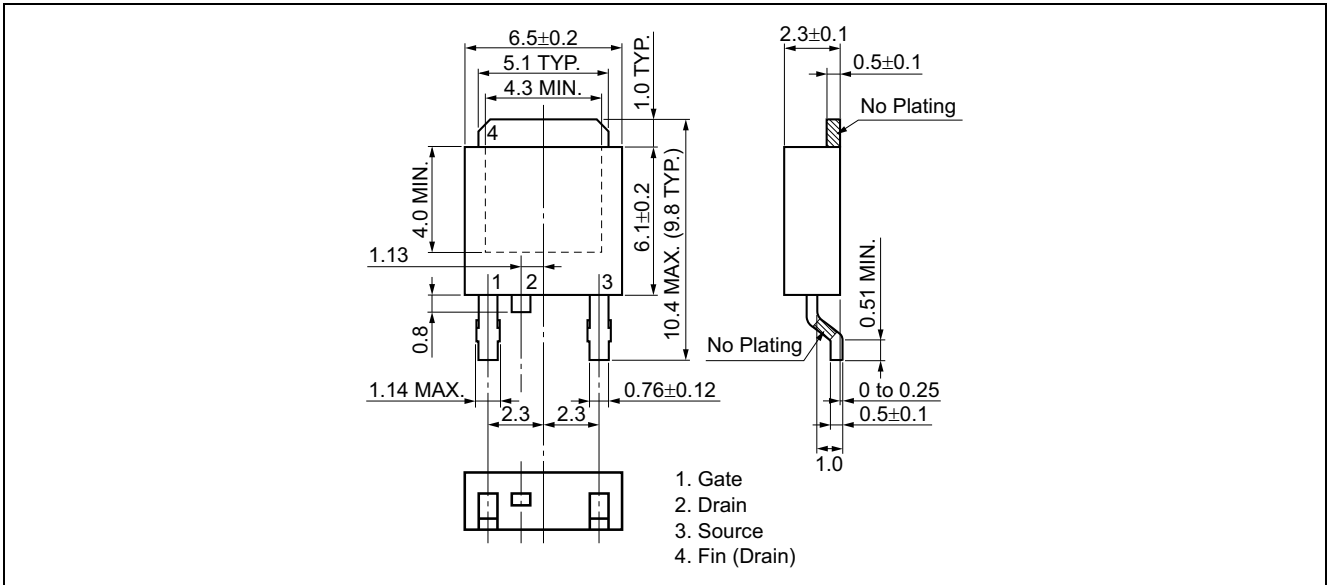


REVERSE RECOVERY TIME vs. DRAIN CURRENT

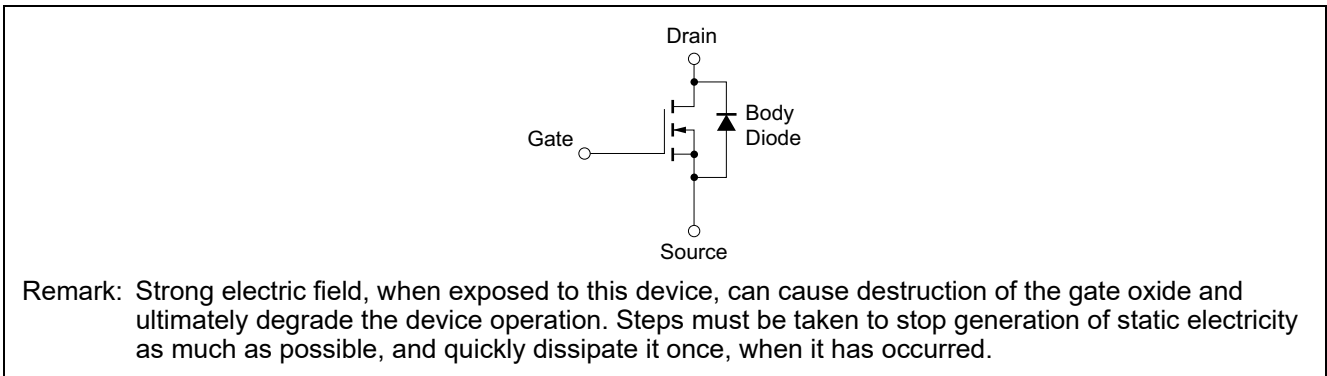


Package Drawing (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.3g TYP.)



Equivalent Circuit



<b>Revision History</b>	<b>NP90N04VDK Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 21, 2013	—	First Edition Issued
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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