

# NP160N04TUK

### MOS FIELD EFFECT TRANSISTOR

R07DS0543EJ0200 Rev. 2.00 May 24, 2018

### **Description**

NP160N04TUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### **Features**

· Super low on-state resistance

 $R_{DS(on)}$  = 1.5 m $\Omega$  MAX. (  $V_{GS}$  = 10 V,  $I_D$  = 80 A )

- · Low Ciss Ciss = 7200 pF TYP. ( $V_{DS}$  = 25 V)
- · Designed for automotive application and AEC-Q101 qualified

### **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP160N04TUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263-7pin(MP-25ZT)
NP160N04TUK-E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode.)

### **Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

ltem	Symbol	Ratings	Unit	
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V	
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V	
Drain Current (DC) (T <sub>C</sub> = 25 °C)	I <sub>D(DC)</sub>	±160	A	
Drain Current (pulse) *1,3	I <sub>D(pulse)</sub>	±640	A	
Total Power Dissipation (T <sub>C</sub> = 25 °C)	P <sub>T1</sub>	250	W	
Total Power Dissipation (T <sub>A</sub> = 25 °C)	P <sub>T2</sub>	1.8	W	
Channel Temperature	T <sub>ch</sub>	175	°C	
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C	
Repetitive Avalanche Current *2,3	I <sub>AR</sub>	56	A	
Repetitive Avalanche Energy *2,3	Ear	313	mJ	

### **Thermal Resistance**

Channel to Case Thermal Resistance	Rth(ch-C)*3	0.60	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)*3	83.3	°C/W

Notes \*1. TC = 25°C, PW  $\leq$  10  $\mu$  s, Duty Cycle  $\leq$  1%

\*2. RG = 25  $\Omega$ , VGS = 20  $\rightarrow$  0 V

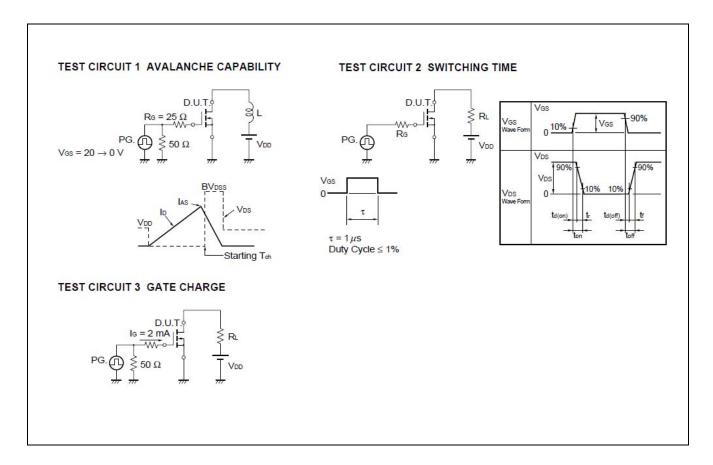
\*3. Not subject of production test. Verified by design/characterization.

### Electrical Characteristics (T<sub>A</sub>=25°C)

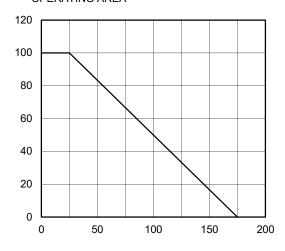
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	$V_{GS}$ = $\pm$ 20 V, $V_{DS}$ = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	60	120		S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 80 A
Drain to Source On-state	R <sub>DS(on)</sub>		1.25	1.50	mΩ	V <sub>G</sub> S = 10 V, I <sub>D</sub> = 80 A
Resistance *1						
Input Capacitance *2	C <sub>iss</sub>		7200	10800	pF	V <sub>DS</sub> = 25 V
Output Capacitance *2	C <sub>oss</sub>		1040	1560	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance *2	C <sub>rss</sub>		390	710	pF	f = 1 MHz
Turn-on Delay Time *2	t <sub>d(on)</sub>		30	70	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 80 A
Rise Time *2	t <sub>r</sub>		16	40	ns	V <sub>GS</sub> = 10 V
Turn-off Delay Time *2	t <sub>d(off)</sub>		100	200	ns	$R_G = 0 \Omega$
Fall Time *2	t <sub>f</sub>		13	40	ns	
Total Gate Charge *2	$Q_{G}$		126	189	nC	V <sub>DD</sub> = 32 V
Gate to Source Charge	Q <sub>GS</sub>		32		nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	$Q_{GD}$		31		nC	I <sub>D</sub> = 160 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I <sub>F</sub> = 160 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		62		ns	I <sub>F</sub> = 160 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>		110		nC	di/dt = 100 A/ <i>μ</i> s

Note. \*1 Pulse test

Note. \*2 Not subject of production test. Verified by design/characterization.

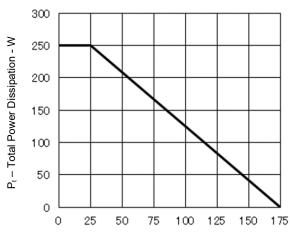


# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



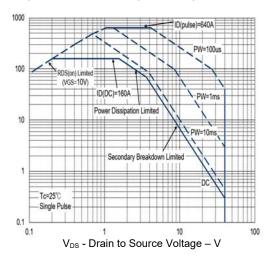
 $T_{\text{C}}$  - Case Temperature -  $^{\circ}\text{C}$ 

## TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

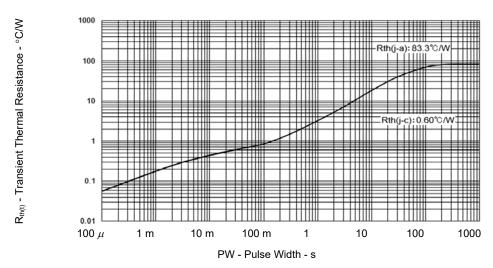


T<sub>C</sub> - Case Temperature - °C

### FORWARD BIAS SAFE OPERATING AREA



#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



Ip - Drain Current - A

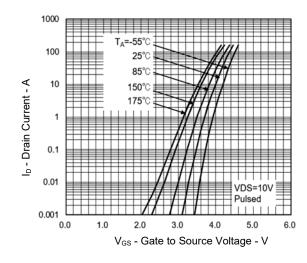
V<sub>GS(th)</sub> - Gate to Source Threshold Voltage - V

 $R_{DS(on)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

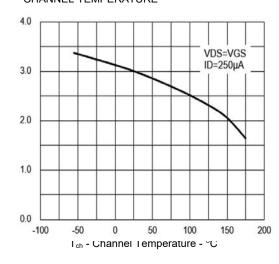
# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

## 700 600 500 400 300 200 100 0 0.2 0.4 0.6 0.8 1 V<sub>DS</sub> - Drain to Source Voltage - V

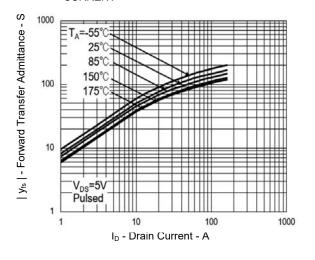
### FORWARD TRANSFER CHARACTERISTICS



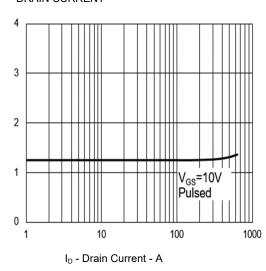
# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



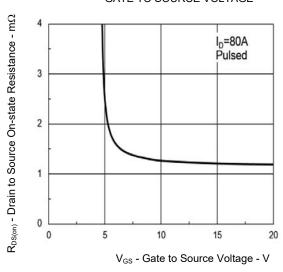
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



 $R_{\text{DS(on)}}$  - Drain to Source On-state Resistance -  $m\Omega$ 

### DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

### 4 V<sub>GS</sub>=10V I<sub>D</sub>=80A Pulsed 3 2 0 -100 -50 0 50 100 150 200

# $T_{\text{ch}}$ - Channel Temperature - $^{\circ}C$

## 100000 Ciss 10000 1000 Crss V<sub>GS</sub>=0V f=1MHz 100

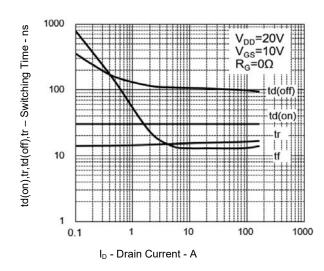
0.1

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

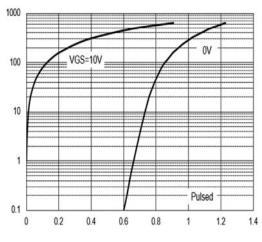
 $V_{\text{DS}}$  - Drain to Source Voltage - V

10

### SWITCHING CHARACTERISTICS

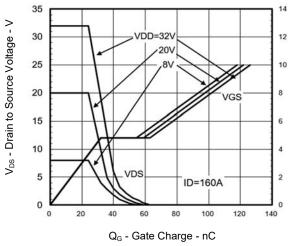


### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

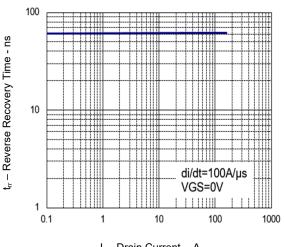


 $V_{\text{F(S-D)}}$  - Source to Drain Voltage - V

### DYNAMIC INPUT CHARACTERISTICS



### REVERSE RECOVERY TIME vs. DRAIN CURRENT

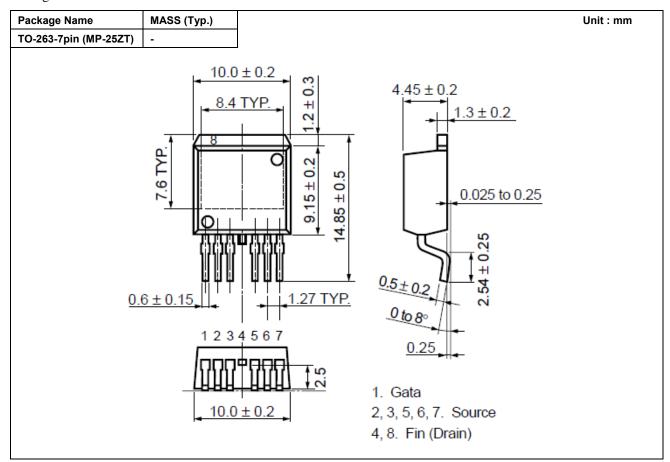


I<sub>F</sub> - Drain Current - A

100

IF - Diode Forward Current - A

### Package Dimensions





Equivalent circuit

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**Revision History** 

## NP180N04TUK Preliminary Datasheet

		Description		
Rev.	Date	Page	Summary	
0.01	Apr 26, 2010	-	1st edition	
2.00	May 24 ,2018	1	Note 3 was added	
		2	Note 2 was added	

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