MPEG AUDIO CLOCK SOURCE

MK1413

Description

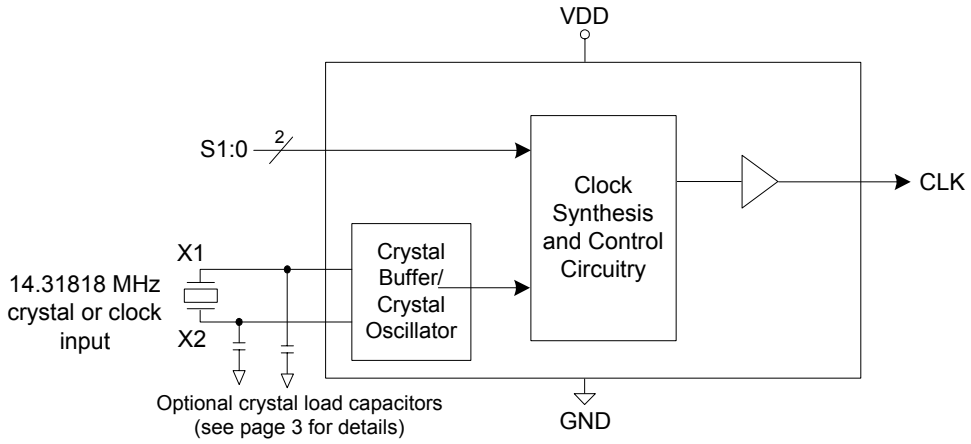
The MK1413 is the ideal way to generate clocks for MPEG audio devices in computers. The device uses IDT's proprietary mixture of analog and digital Phase-Locked Loop (PLL) technology to synthesize one of four frequencies from the 14.31818 MHz reference. In an 8-pin SOIC, the MK1413 can save component count, board space, and cost over crystals and oscillators, and increase reliability by eliminating three expensive mechanical devices from the board.

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

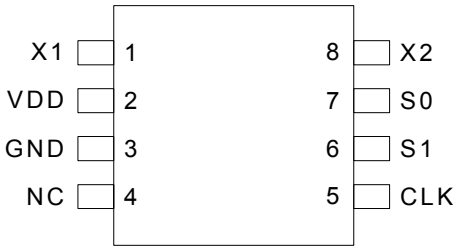
Features

- Packaged in 8-pin SOIC
- Pb (lead) free package
- Input crystal or clock frequency of 14.31818 MHz
- Provides master MPEG clocks for 32 kHz, 44.1 kHz, and 48 kHz sampling rates
- Output clock frequencies of 8.192 MHz, 11.2896 MHz, 12.288 MHz, and 16.9344 MHz
- Low jitter
- 25 mA drive capability at TTL levels (at 5.0 V)
- 3.3 V or 5.0 V (±10%) supply voltage
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8-pin SOIC

Audio Clock Output Selection Table

S1	S0	Audio Clock (pin 5)	Accuracy (ppm)
0	0	8.192 MHz	-2 ppm
0	1	11.2896 MHz	-24 ppm
1	0	12.288 MHz	-2 ppm
1	1	16.9344 MHz	-24 ppm

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	Input	Crystal connection. Connect this pin to a 14.31818 MHz crystal or clock.
2	VDD	Power	Connect to 3.3 V or 5 V.
3	GND	Power	Connect to ground.
4	NC	—	No connect.
5	CLK	Output	Audio clock output as per table above.
6	S1	Input	Frequency Select 1 input. Determines CLK output as per table above.
7	S0	Input	Frequency Select 0 input. Determines CLK output as per table above.
8	X2	Output	Crystal connection to a 14.31818 MHz crystal or leave unconnected for clock input.

Application Information

Series Termination Resistor

Clock output traces should use series termination. For series terminating a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line and as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for capacitors from X1 to ground and from X2 to ground, and a parallel rsonant 14.31818 MHz crystal is recommended. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. To reduce possible noise pickup, use very short PCB traces (and no vias) been the crystal and device.

The value (in pF) of each crystal load capacitor should equal (C_L -4) x2, where C_L is the crystal's load (correlation) capacitance in pF. The frequency tolerance of the crystal should be 50 ppm or better.For a clock input, connect X1 and leave X2 unconnected. Because these capacitors adjust the stray capacitance of the PCB, check the output frequency using your final layout to see if the value of C should be changed.

PCB Layout Recommendations

Observe the following guidelines for optimum device performance and lowest output phase noise:

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK1413. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1413. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature (max of 10 seconds)	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 5.0 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}	input clock only	(VDD/2)+1	VDD/2		V
Input Low Voltage	V_{IL}	input clock only		VDD/2	(VDD/2)-1	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Supply Current	IDD	5 V, no Load		12		mA
Supply Current	IDD	3.3 V, no Load		7		mA
Input Capacitance	C_{IN}	S0, S1 pins		7		pF
Synthesize Frequency Error		With exact crystal			25	ppm

AC Electrical Characteristics

Unless stated otherwise, **VDD = 5.0 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock or Crystal Frequency				14.31818		MHz
Input Crystal Accuracy					50	ppm
Input Clock Duty Cycle		Time above VDD/2	20		80	%
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		Time above VDD/2	40	50	60	%
Absolute Clock Period Jitter				200		ps
One Sigma, Clock Period Jitter				70		ps

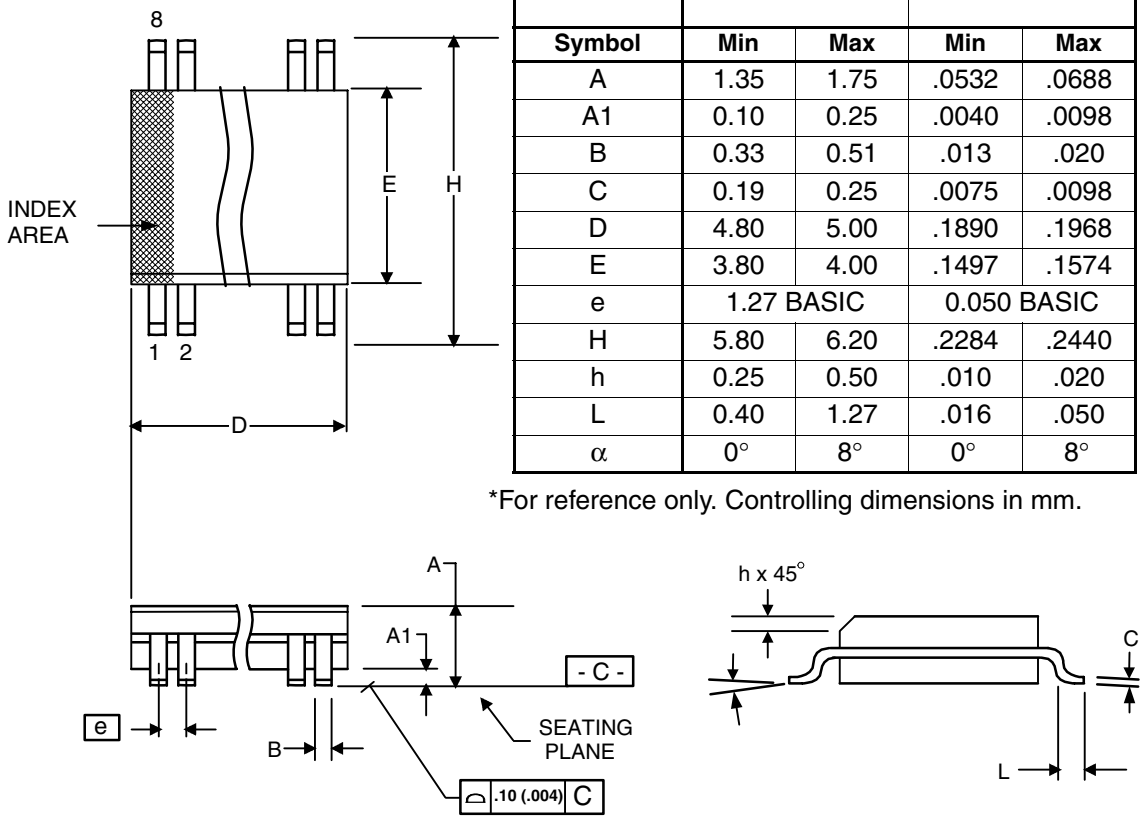
Note: Typical values are at 25°C

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1413SLF	MK1413SL	Tubes	8-pin SOIC	0 to +70° C
MK1413SLFTR	MK1413SL	Tape and Reel	8-pin SOIC	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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