ISL73840SEH

Radiation Tolerant 30V 16-Channel Analog Multiplexer

The ISL73840SEH is a radiation tolerant, 16-channel high ESD protected multiplexer fabricated using the Renesas proprietary P6SOI (Silicon On Insulator) process technology. It operates with a dual supply voltage ranging from ±10.8V to ±16.5V. It has a 4-bit address plus an enable pin that can be driven with adjustable logic thresholds to conveniently select one of 16 available channels. An inactive channel is separated from an active channel by a high impedance, which inhibits any interaction between them.

The ISL73840SEH's low r_{ON} allows for improved signal integrity and reduced power losses. The ISL73840SEH is also designed for cold sparing, making it excellent for high reliability applications that have redundancy requirements. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without loading signal sources. The ISL73840SEH also incorporates input analog overvoltage protection, which disables the switch to protect downstream devices.

The ISL73840SEH is available in a 28 Ld CDFP or die form and operates across the extended temperature range of -55°C to +125°C.

A 32-channel version in a 48 Ld CQFP is also available. Refer to the ISL73841SEH datasheet for more information. For a list of differences between the ISL73840SEH and ISL73841SEH, refer to Table 1 on page 3.

Features

- **DLA SMD #5962-15219**
- **Fabricated using P6SOI process technology**
- **ESD protection 8kV (HBM)**
- **Rail-to-rail operation**
- **Overvoltage protection**
- **Low r_{ON}. . . . . <500Ω (typical)**
- **Flexible split rail operation**
  - **Positive supply above GND (V^+) . . . . . +10.8V to +16.5V**
  - **Negative supply below GND (V^-) . . . . . -10.8V to -16.5V**
- **Adjustable logic threshold control with VREF pin**
- **Cold sparing capable (from ground). . . . . ±25V**
- **Analog overvoltage range (from ground). . . . . ±35V**
- **Off switch leakage . . . . . 100nA (maximum)**
- Transition times (t_R, t_F) . . . . . 500ns (typical)
- Break-before-make switching
- Grounded metal lid (internally connected)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - Low dose rate (0.01rad(Si)/s) . . . . 50krad(Si) (see Note 1)
  - SEB LET_{TH} . . . . . 86.4 MeV•cm^2/mg

NOTE:

1. Product capability established by initial characterization. All subsequent lots are assurance tested to 50krad (0.01rad(Si)/s) wafer-by-wafer.

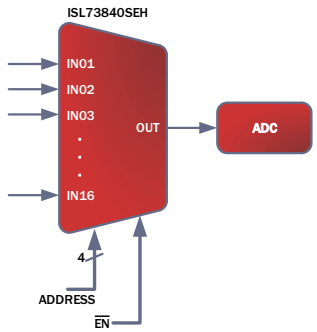


FIGURE 1. TYPICAL APPLICATION

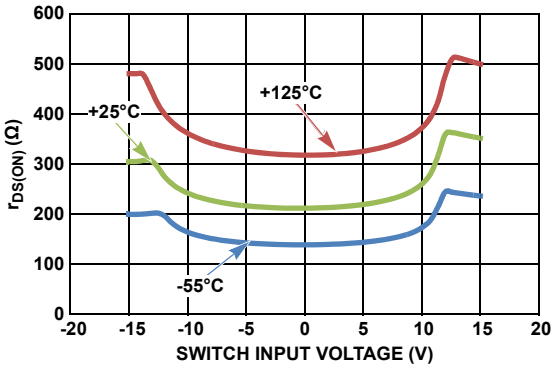


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY ACROSS SWITCH INPUT COMMON-MODE VOLTAGE AT +25°C

Table of Contents

Ordering Information

ORDERING/SMD NUMBER (Note 3)	PART NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	TEMP RANGE
5962L1521902VXC	ISL73840SEHVF	LDR to 50krad(Si)	28 LD CDFP	K28.A	-55 to +125°C
5962L1521902V9A	ISL73840SEHVX		Die	N/A	
N/A	ISL73840SEHF/PROTO (Note 5)	N/A	28 LD CDFP	K28.A	
N/A	ISL73840SEHX/SAMPLE (Note 5)		Die	N/A	

NOTES:

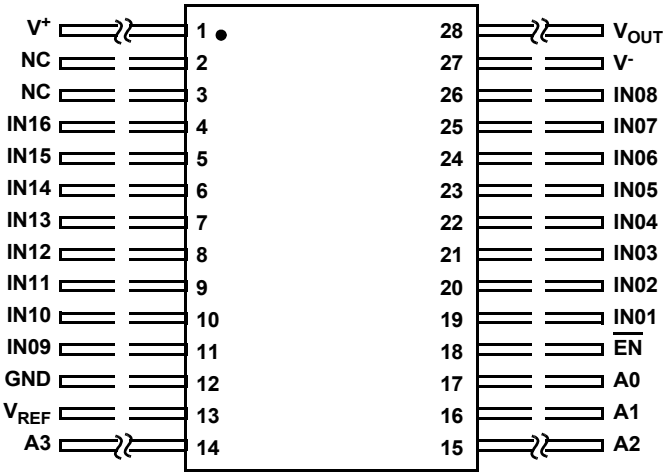
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications (±15V)" and "Electrical Specifications (±12V)".
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

TABLE 1. TABLE OF DIFFERENCES

SPECIFICATION	ISL73840SEH	ISL73841SEH
Number of Channels	16	32
Supply Current (I+/I-)	350µA (maximum)	400µA (maximum)
Output Leakage (+125°C)	60nA (maximum)	120nA (maximum)

Pin Configuration

ISL73840SEH
(28 LD CDFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{OUT}	28	Output for multiplexer (see Circuit 1 in Figure 3)
V^+	1	Positive power supply (see Circuit 3 in Figure 3)
V^-	27	Negative power supply (see Circuit 4 in Figure 3)
NC	2, 3	Not electrically connected
INx	4, 5, 6, 7, 8, 9, 10, 11, 19, 20, 21, 22, 23, 24, 25, 26	Input for multiplexer (see Circuit 2 in Figure 3)
Ax	14, 15, 16, 17	Address lines for multiplexer (see Circuit 3 in Figure 3)
$\overline{EN}$	18	Enable control for multiplexer (active low, see Circuit 3 in Figure 3)
V_{REF}	13	Reference voltage used to set logic thresholds (see Circuit 3 in Figure 3)
GND	12	Ground
LID	-	Package Lid is internally connected to GND (Pin 12)

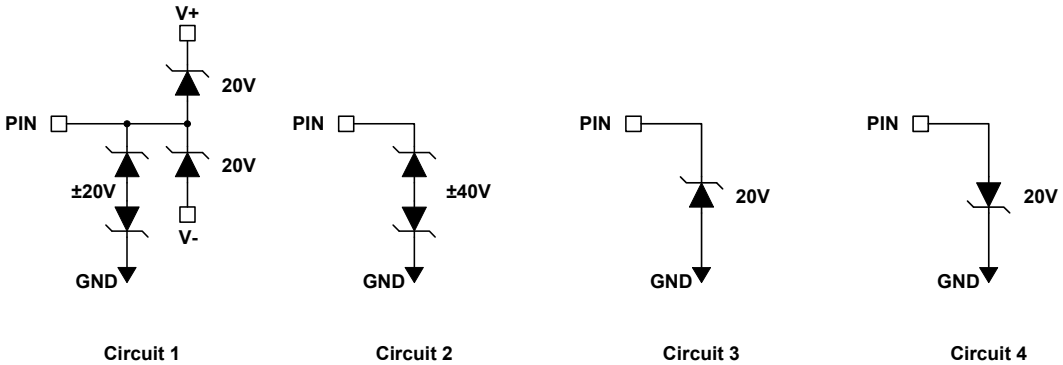


FIGURE 3. ESD Circuits

Absolute Maximum Ratings

Positive Supply Voltage above GND (V^+) (Note 8) . . . . . +20V
Negative Supply Voltage below GND (V^-) (Note 8) . . . . . -20V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 8) 40V
Maximum Current Through Selected Switch. 10mA
Analog Input Voltage (INx)
From GND (Note 8). . . . . ±35V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . . GND - 0.3V to +16.5V
VREF to GND (Note 8) . . . . . +16.5V
ESD Tolerance
Human Body Model (Tested per MIL-STD-883 TM 3015) 8kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A) 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld CDFP (Notes 6, 7)	48	4

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Positive Supply Voltage Above GND (V^+) . . . . . +10.8V to +16.5V
Negative Supply Voltage Below GND (V^-) . . . . . -10.8V to -16.5V
Supply Voltage Differential (V^+ to V^-) . . . . . 21.6V to 33V
VREF to GND . . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379 for details.
7. For θ_{JC}, the "case temp" location is the center of the package underside.
8. Tested in a heavy ion environment at LET = 86.3 MeV • cm^2/mg at +125°C.

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total Ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Analog Input Signal Range	V_S		V^-	-	V^+	V
Channel ON-Resistance	r_{ON}	V± = ±15.0V, ±16.5V, $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±15.0V, ±16.5V, $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
r_{ON} Match Between Channels	Δr_{ON}	V_{IN} = +5V, -5V; $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA	-	10	**20**	Ω
ON-Resistance Flatness	$R_{FLAT(ON)}$	V_{IN} = +5V, -5V, $V_{\overline{EN}}$ = 0V	-	-	**25**	Ω
Switch Off Leakage	$I_{S(OFF)}$	V_{IN} = V^+ - 5V, V± = ±16.5V, All unused inputs are tied to V^- + 5V	**-10**	-	**10**	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V^- + 5V, V± = ±16.5V, All other inputs = V^+ - 5V, T_A = +25°C	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-100	-	100	nA
Switch Off Leakage with Device Powered Off	$I_{S(OFF)\ POWER\ OFF}$	V_{IN} = +25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V, T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V, T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total Ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Switch Off Leakage with Device Powered OPEN	$I_{S(OFF)}$ POWER OPEN	V_{IN} = +25V, $V_{\overline{EN}}$ = V_A = V_{REF} = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, $V_{\overline{EN}}$ = V_A = V_{REF} = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA
Switch On Leakage Current into the Drain (Overvoltage)	$I_{D(ON)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-	**10**	nA
		Post radiation	**-10**	-	**10**	nA
		V_{IN} = -35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-	**10**	nA
		Post radiation	**-10**	-	**10**	nA
Switch On Leakage Current into the Source (Overvoltage)	$I_{S(ON)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**1**	250	**500**	µA
		Post radiation	**1**	-	**500**	µA
		V_{IN} = -35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-5.5	**-1**	µA
		Post radiation	**-10**	-	**-1**	µA
Switch Off Leakage Current into the Source (Overvoltage)	$I_{S(OFF)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-750	-	750	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = -55°C	-2	-	2	µA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-750	-	750	nA
Switch Off Leakage	$I_{D(OFF)}$	V_{OUT} = V^+ - 5V, All inputs = V^- + 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	0	-	60	nA
		Post radiation	-80	-	80	nA
		V_{OUT} = V^- + 5V, All inputs = V^+ - 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-60	-	0	nA
		Post radiation	-80	-	80	nA
Switch Off Leakage Current into the Drain (overvoltage)	$I_{D(OFF)\ OVERVOLT}$	V_{OUT} = 0V, V_{IN} = +35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA
		V_{OUT} = 0V, V_{IN} = -35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA

Electrical Specifications (±15V) V^+ = 15V, V^- = -15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Switch On Leakage Current into the Source/Drain	$I_{D(ON)}$	V_{IN} = V_{OUT} = V^+ - 5V, $V_{\overline{EN}}$ = 0V, T_A = +25°C, -55°C, All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	0	-	60	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V_{OUT} = V^- + 5V, $V_{\overline{EN}}$ = 0V, T_A = +25°C, -55°C, All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-60	-	0	nA
		Post radiation	-100	-	100	nA
Logic Input High/Low Voltage	$V_{AH/L}$, $V_{ENH/L}$	V_{REF} = 5.0V	**1.2**	-	**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V_A = $V_{\overline{EN}}$ = 4.0V V^+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V_A = $V_{\overline{EN}}$ = 0.8V V^+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Quiescent Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**350**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**-350**	-	-	µA
Standby Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**350**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**-350**	-	-	µA
Quiescent Supply Current Into V_{REF}	I_{REF}	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**35**	µA
Standby Current Into V_{REF}	$I_{REF(STBY)}$	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**35**	µA
DYNAMIC						
Transition Time	t_{ALH}	Figures 5, 6	-	0.5	**800**	ns
	t_{AHL}	Figures 5, 6	-	0.5	**800**	ns
Break-Before-Make Delay	t_{BBM}	Figures 9, 10	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
Enable Turn-On Time	t_{ENABLE}	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
Disable Turn-Off Time	$t_{DISABLE}$	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, (Figure 7)	-	2	5	pC
OFF Isolation	V_{ISO}	$V_{\overline{EN}}$ = 4V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	75	-	-	dB
Crosstalk	V_{CT}	$V_{\overline{EN}}$ = 0.8V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	47	-	-	dB
Digital Input Capacitance	C_A	f = 1MHz, V^+ = V^- = 0V	-	-	**7**	pF
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz, V^+ = V^- = 0V	-	-	**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz, V^+ = V^- = 0V	-	-	**50**	pF

Electrical Specifications (±12V)

$V^+ = 12V$, $V^- = -12V$, $V_{AH} = 4.0V$, $V_{AL} = 0.8V$, $V_{REF} = V_{\overline{EN}} = 5.0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Analog Input Signal Range	V_S		V^-		V^+	V
Channel ON-Resistance	r_{ON}	V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = +5V, -5V, $V_{\overline{EN}}$ = 0V	-	-	**500**	Ω
		V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = V^+, V^-, $V_{\overline{EN}}$ = 0V	-	-	**700**	Ω
r_{ON} Match Between Channels	Δr_{ON}	V_{IN} = +5V, -5V; I_{OUT} = -1mA, $V_{\overline{EN}}$ = 0V	-	10	**20**	Ω
ON-Resistance Flatness	$R_{FLAT(ON)}$	V_{IN} = +5V, -5V, V± = ±13.2V, $V_{\overline{EN}}$ = 0V	-	-	**25**	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, $V_{\overline{EN}}$ = 0V T_A = +25°C, -55°C, +125°C	-	-	30	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, $V_{\overline{EN}}$ = 0V, post radiation	-	-	40	Ω
Quiescent Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	-	-	**350**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-350**	-	-	µA
Standby Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	-	-	**350**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	**-350**	-	-	µA
Quiescent Supply Current Into V_{REF}	I_{REF}	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	-	-	**35**	µA
Standby Current Into V_{REF}	$I_{REF(STBY)}$	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	-	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 5, 6	-	0.5	**800**	ns
t_{AHL}		Figures 5, 6	-	0.5	**800**	ns
t_{BBM}	Break-Before-Make Delay	Figures 9, 10	**5**	50	**200**	ns
		Post radiation	-	-	**400**	ns
t_{ENABLE}	Enable Turn-On Time	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
$t_{DISABLE}$	Disable Turn-Off Time	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

TABLE 2. TRUTH TABLE

A3	A2	A1	A0	EN	"ON" CHANNEL
X	X	X	X	1	None
0	0	0	0	0	1
0	0	0	1	0	2
0	0	1	0	0	3
0	0	1	1	0	4
0	1	0	0	0	5
0	1	0	1	0	6
0	1	1	0	0	7
0	1	1	1	0	8
1	0	0	0	0	9
1	0	0	1	0	10
1	0	1	0	0	11
1	0	1	1	0	12
1	1	0	0	0	13
1	1	0	1	0	14
1	1	1	0	0	15
1	1	1	1	0	16

NOTE:

10. X = Don't care, "1" = Logic High, "0" = Logic Low.

Block Diagram

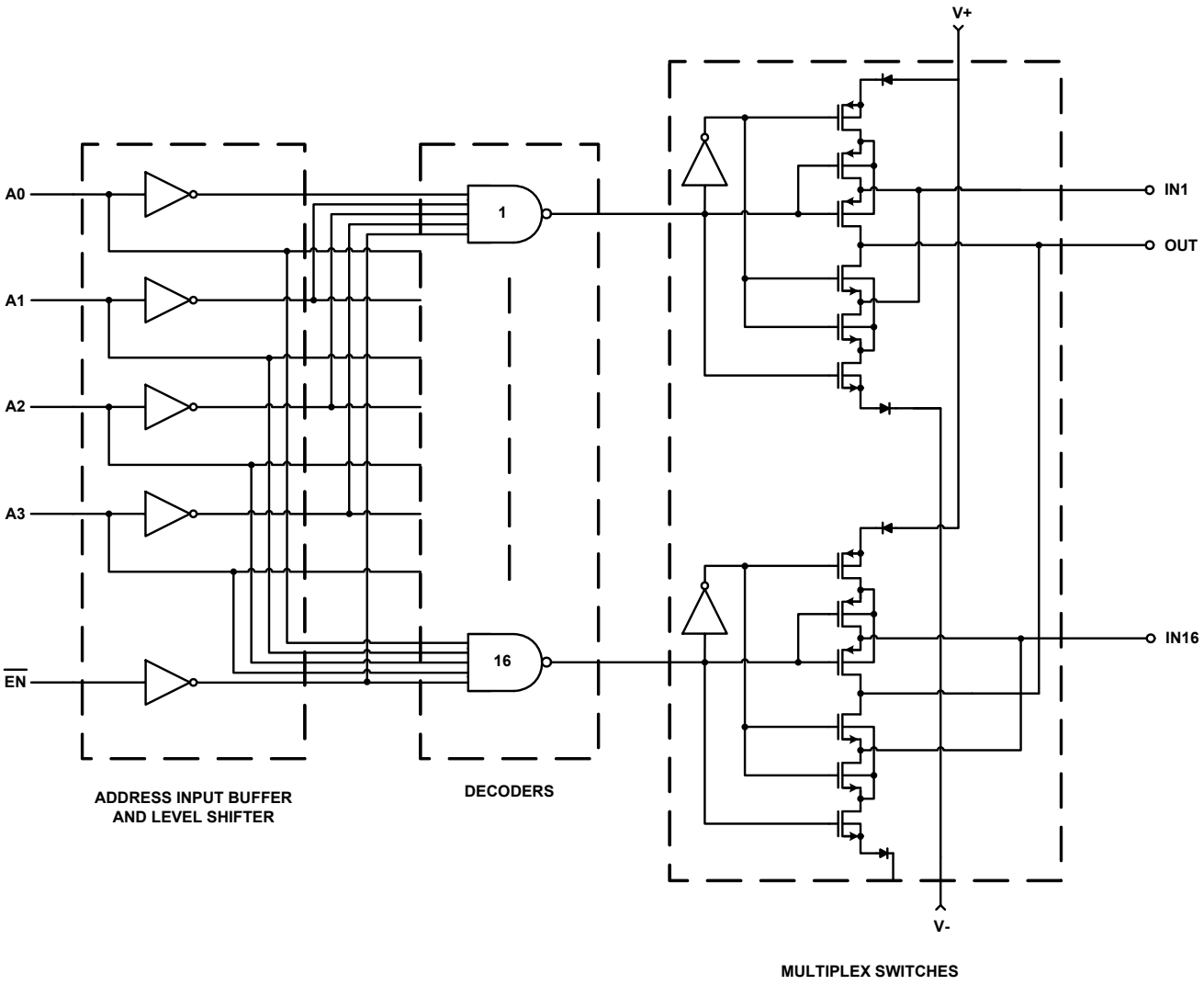


FIGURE 4. BLOCK DIAGRAM

Timing Diagrams

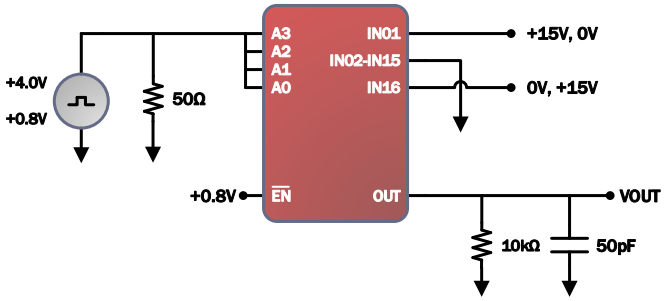


FIGURE 5. ADDRESS TIME TO OUTPUT TEST CIRCUIT

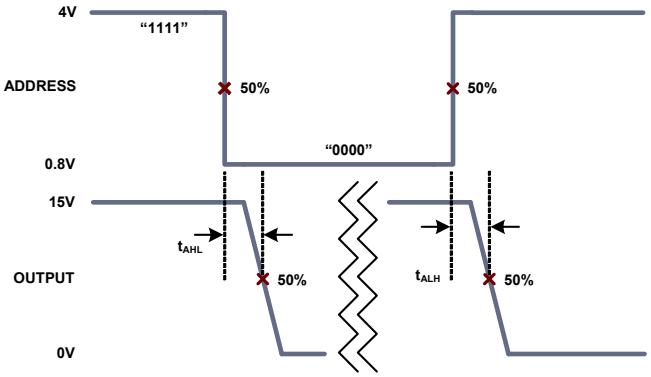


FIGURE 6. ADDRESS TIME TO OUTPUT DIAGRAM

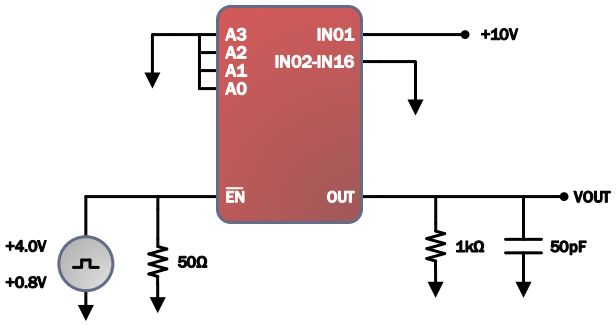


FIGURE 7. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

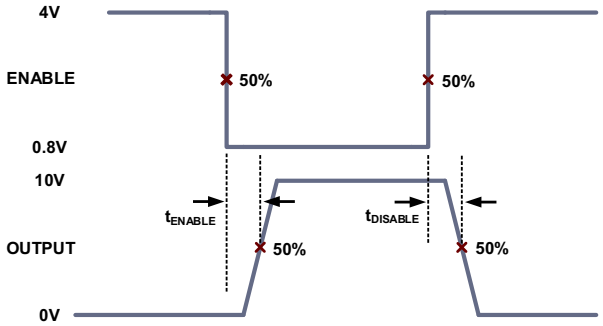


FIGURE 8. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

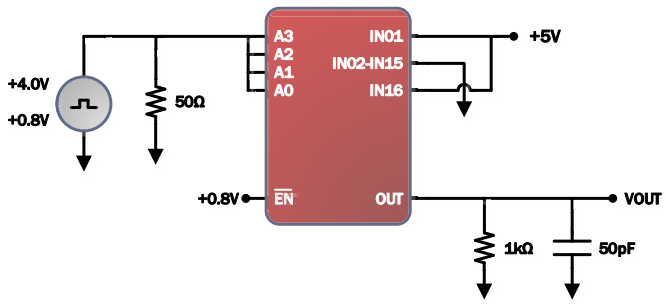


FIGURE 9. BREAK-BEFORE-MAKE TEST CIRCUIT

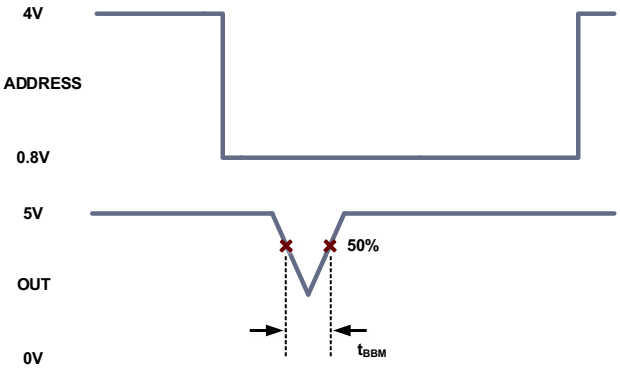


FIGURE 10. BREAK-BEFORE-MAKE DIAGRAM

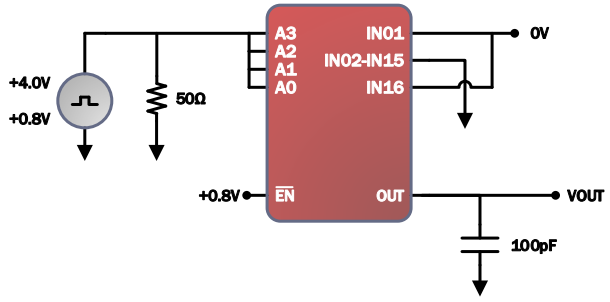


FIGURE 11. CHARGE INJECTION TEST CIRCUIT

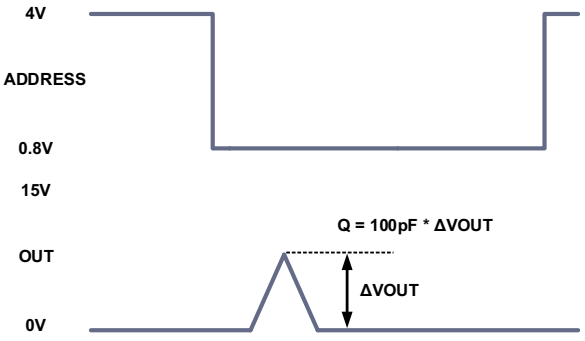


FIGURE 12. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified.

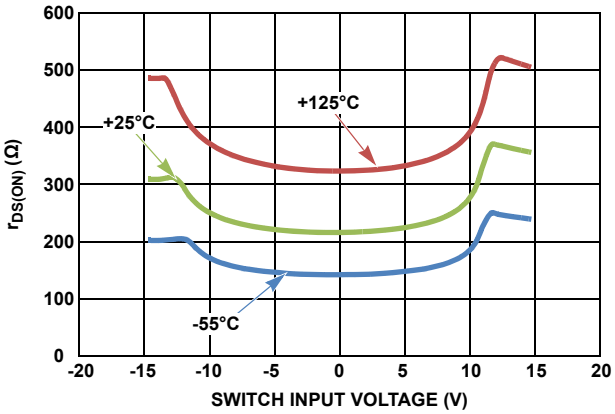


FIGURE 13. $r_{DS(ON)}$ vs VCM (V± = 14.5V)

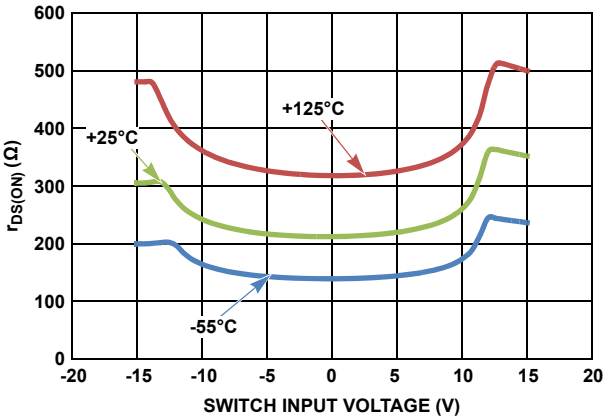


FIGURE 14. $r_{DS(ON)}$ vs VCM (V± = 15.0V)

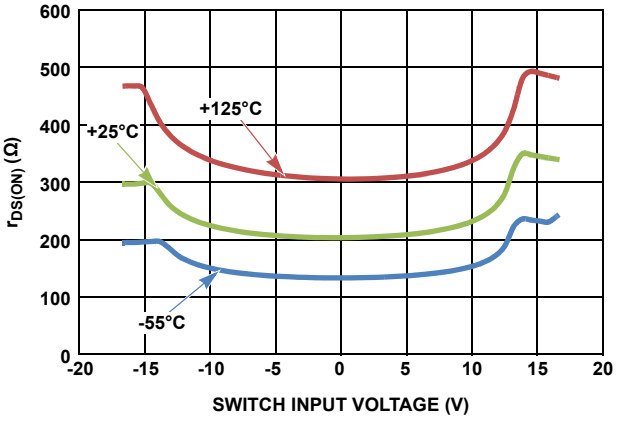


FIGURE 15. $r_{DS(ON)}$ vs VCM (V± = 16.5V)

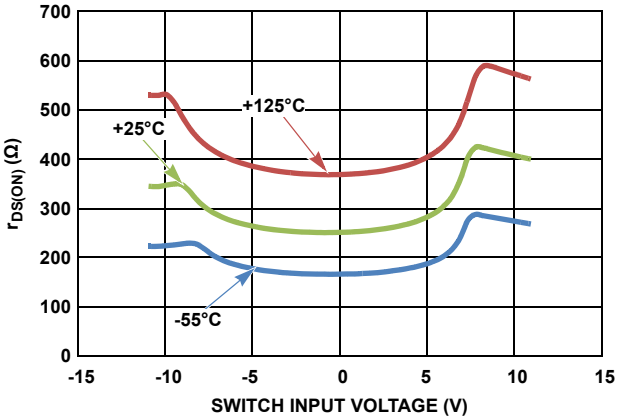


FIGURE 16. $r_{DS(ON)}$ vs VCM (V± = 10.8V)

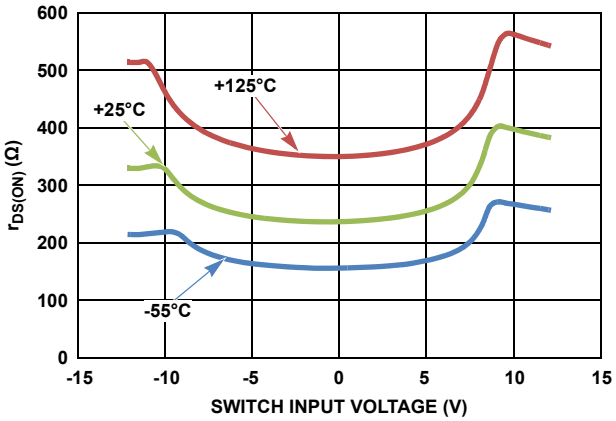


FIGURE 17. $r_{DS(ON)}$ vs VCM (V± = 12.0V)

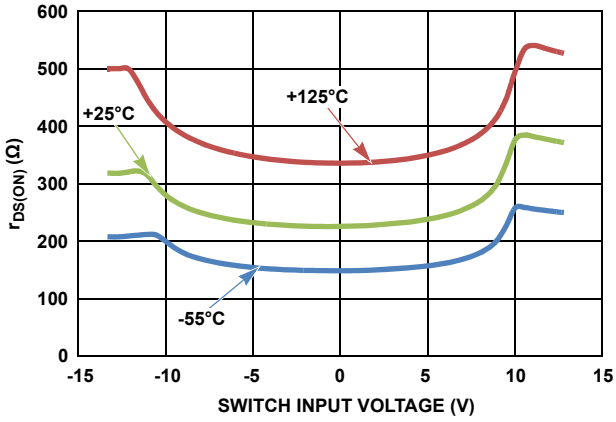


FIGURE 18. $r_{DS(ON)}$ vs VCM (V± = 13.2V)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

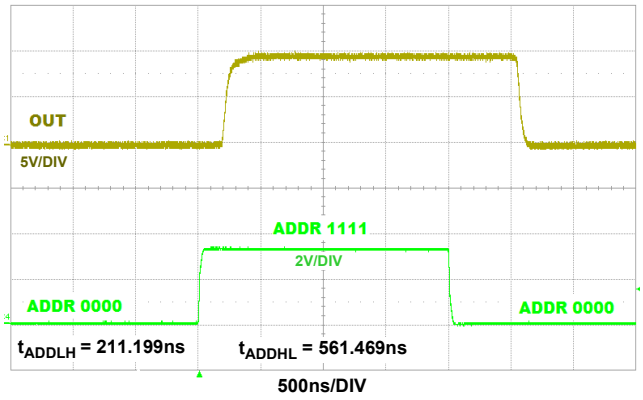


FIGURE 19. TYPICAL ADDRESS TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

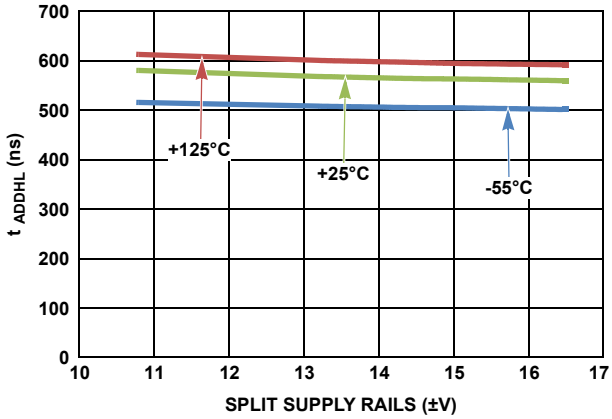


FIGURE 20. ADDRESS TO OUTPUT DELAY (HIGH TO LOW)

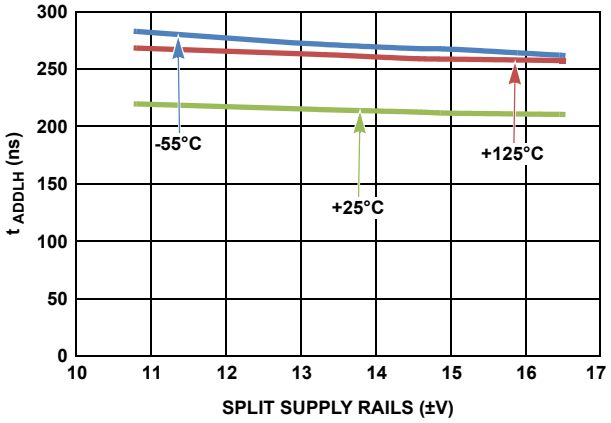


FIGURE 21. ADDRESS TO OUTPUT DELAY (LOW TO HIGH)

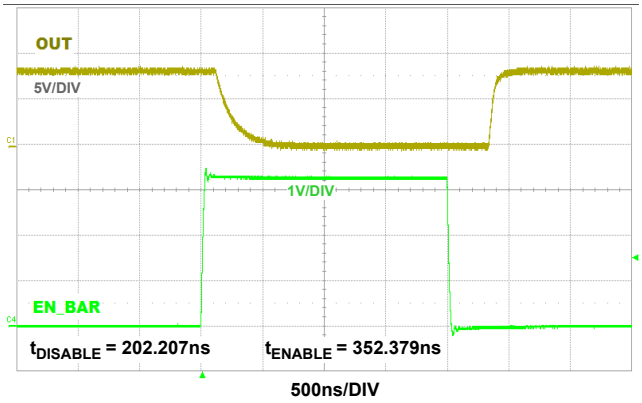


FIGURE 22. TYPICAL ENABLE TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

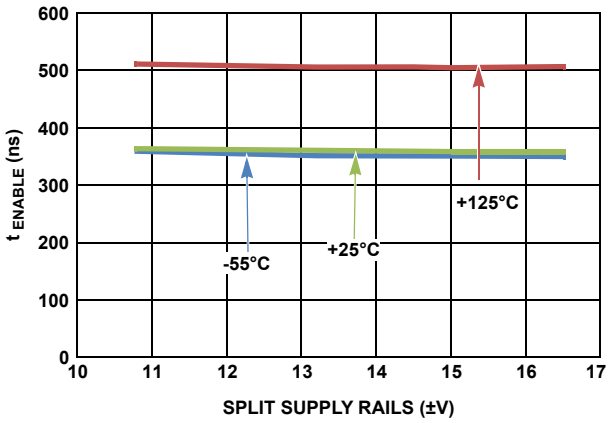


FIGURE 23. ENABLE TO OUTPUT DELAY (LOW TO HIGH)

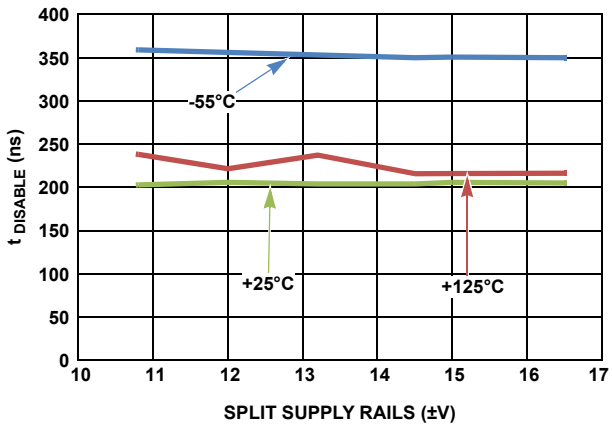


FIGURE 24. DISABLE TO OUTPUT DELAY (LOW TO HIGH)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

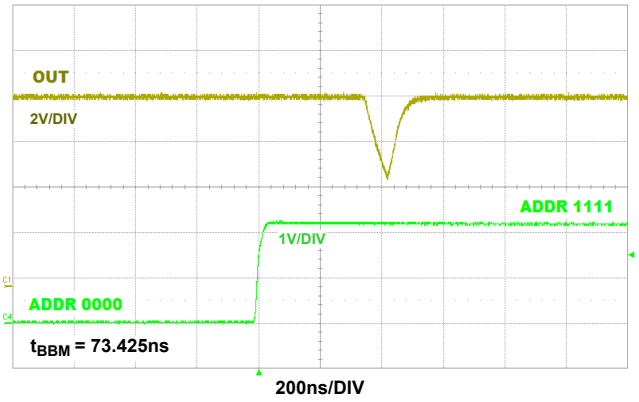


FIGURE 25. TYPICAL BREAK-BEFORE-MAKE DELAY ($V\pm = 15V$, $+25°C$)

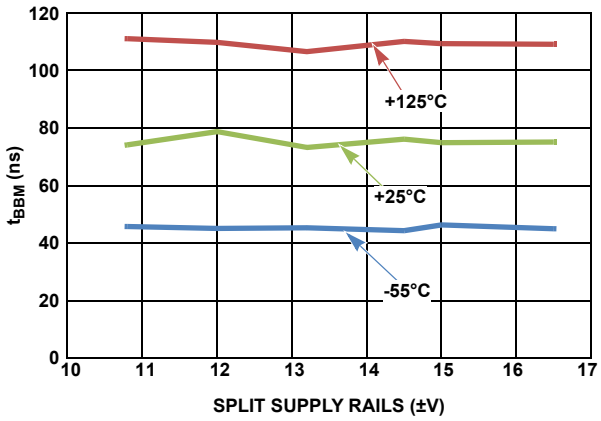


FIGURE 26. BREAK-BEFORE-MAKE DELAY

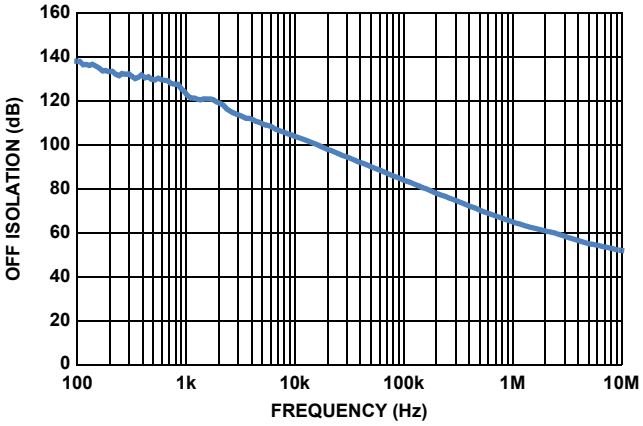


FIGURE 27. OFF ISOLATION ($V\pm = \pm15V$, $R_L = 1k\Omega$, $+25°C$)

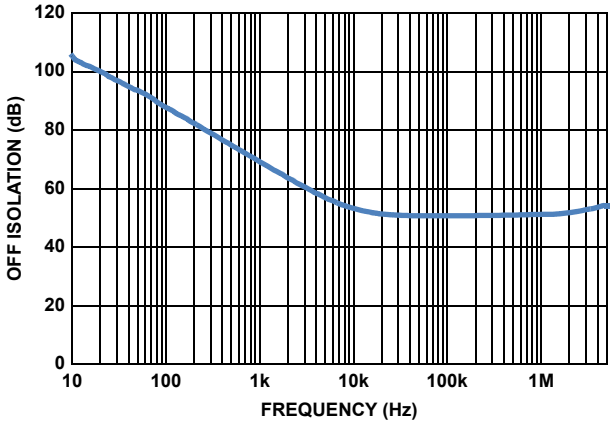


FIGURE 28. OFF ISOLATION ($V\pm = \pm15V$, R_L = OPEN, $+25°C$)

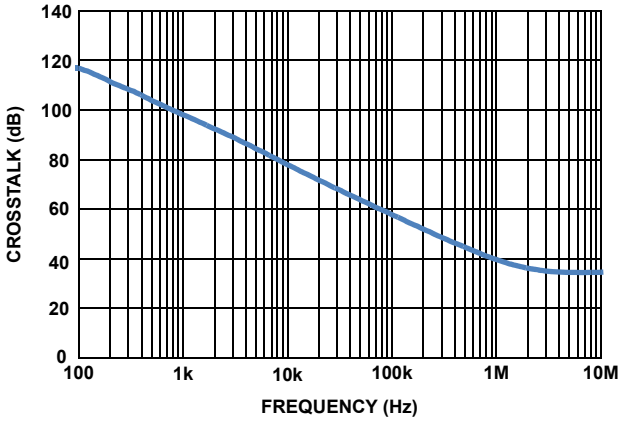


FIGURE 29. CROSSTALK ($V\pm = \pm15V$, $R_L = 1k\Omega$, $+25°C$)

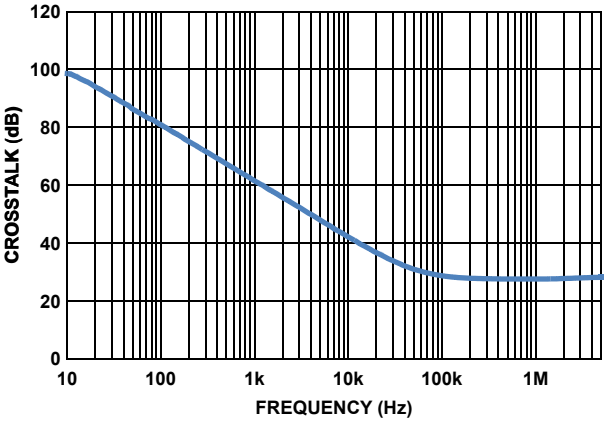


FIGURE 30. CROSSTALK ($V\pm = \pm15V$, R_L = OPEN, $+25°C$)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

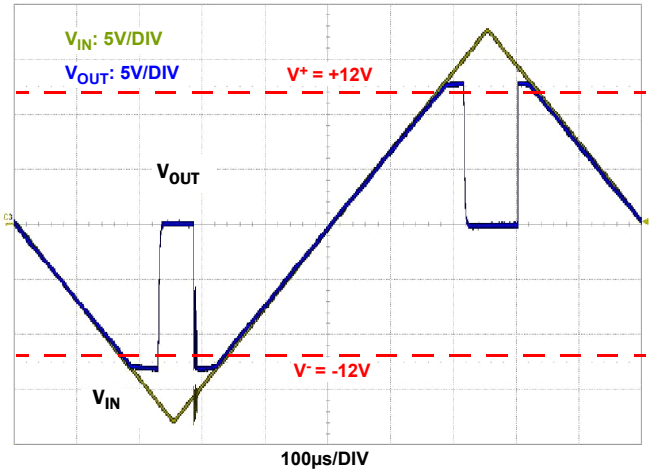


FIGURE 31. OVERVOLTAGE/UNDERVOLTAGE PROTECTION (+25°C)

Post Low Dose Rate Radiation Characteristics ($V\pm = \pm15V$)

Unless otherwise specified, $V\pm = \pm15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

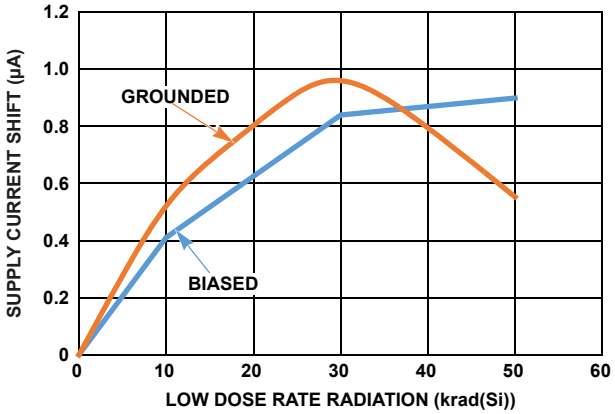


FIGURE 32. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

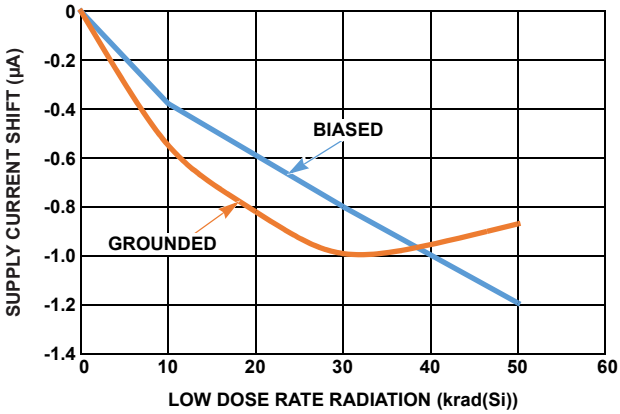


FIGURE 33. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

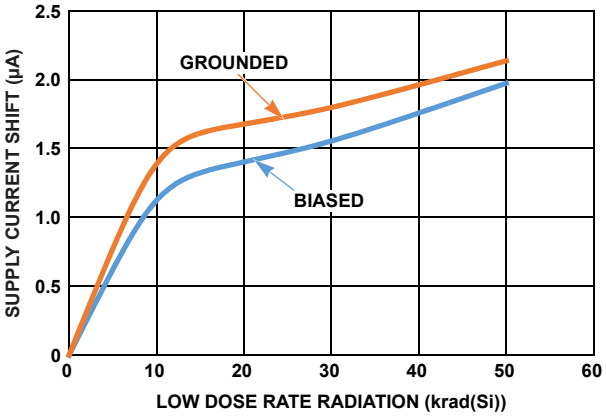


FIGURE 34. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

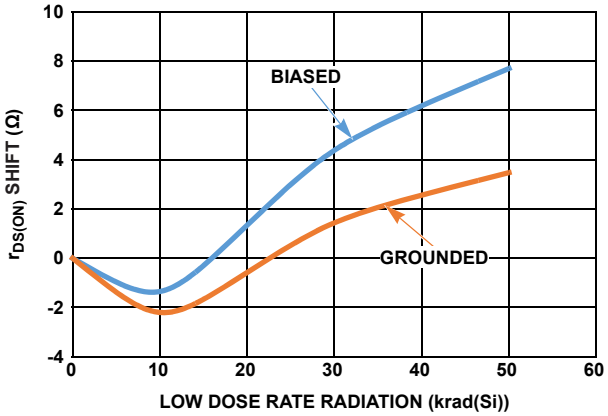


FIGURE 35. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

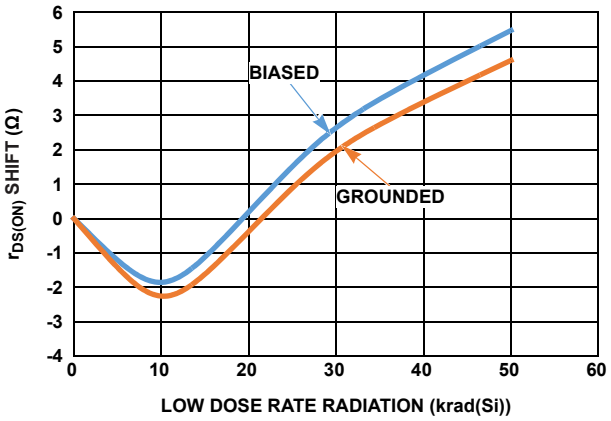


FIGURE 36. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

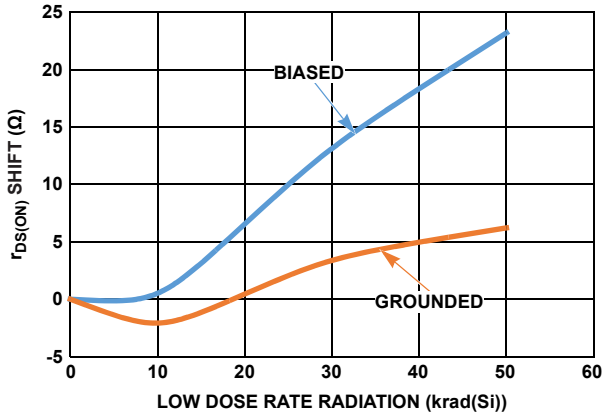


FIGURE 37. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

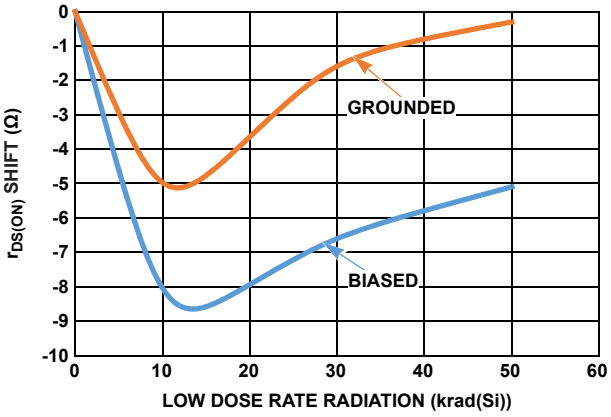


FIGURE 38. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

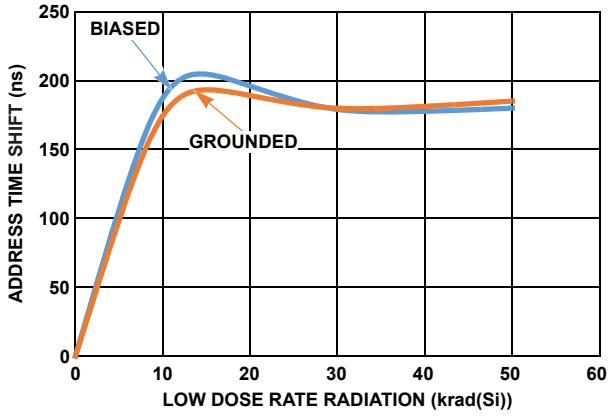


FIGURE 39. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

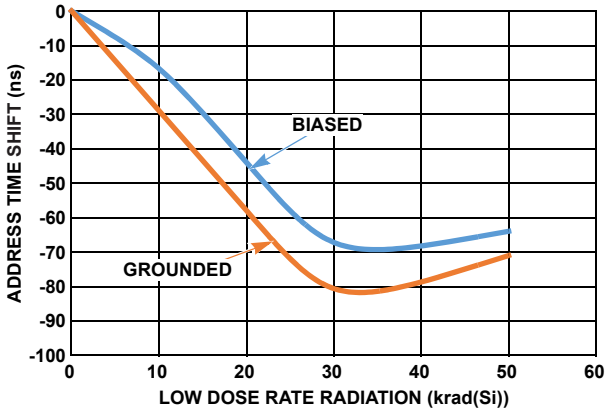


FIGURE 40. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

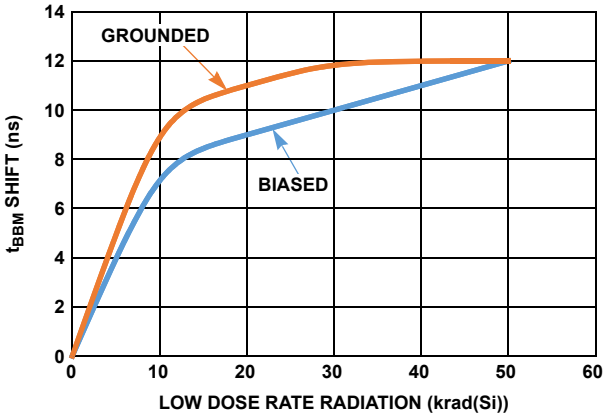


FIGURE 41. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

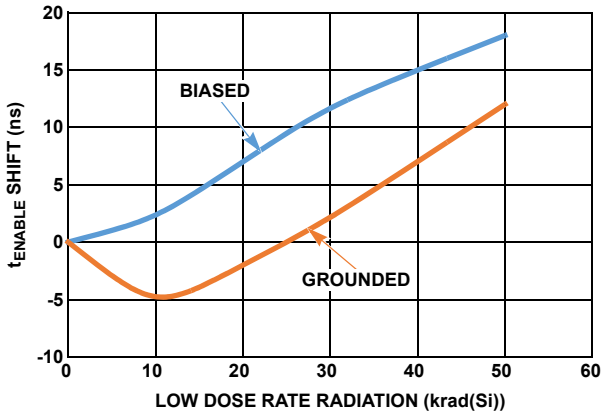


FIGURE 42. t_{ENABLE} SHIFT vs LDR RADIATION

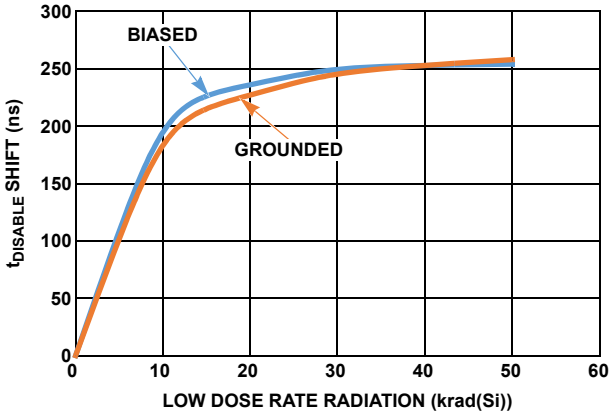


FIGURE 43. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

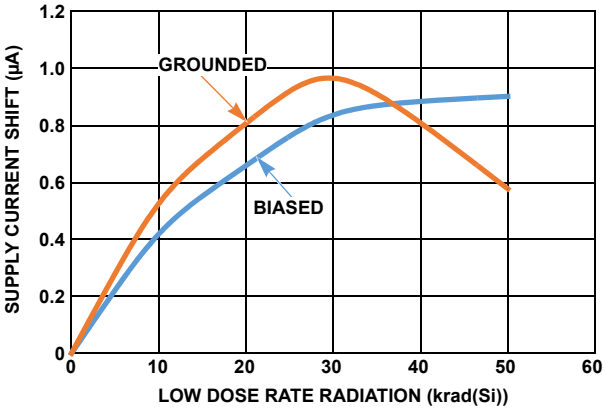


FIGURE 44. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

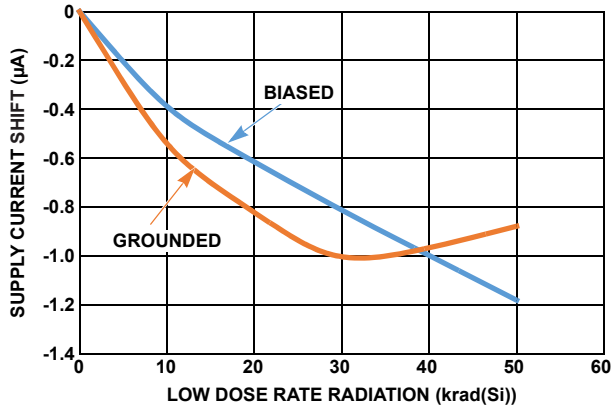


FIGURE 45. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

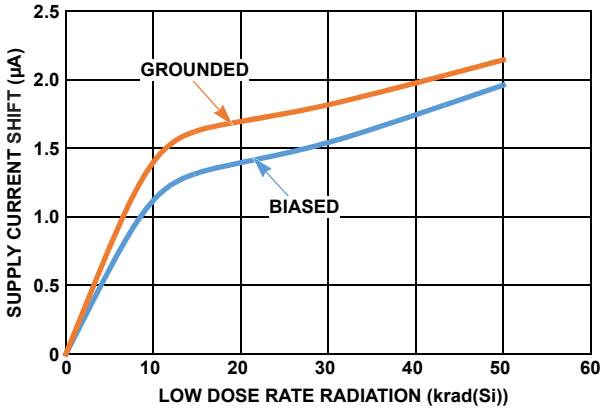


FIGURE 46. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

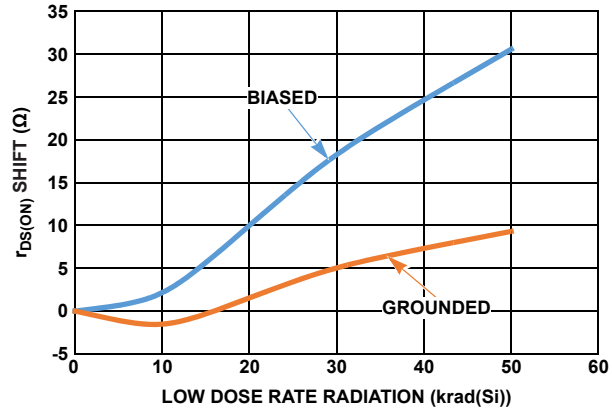


FIGURE 47. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics ($V\pm = \pm12V$)

Unless otherwise specified, $V\pm = \pm12V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

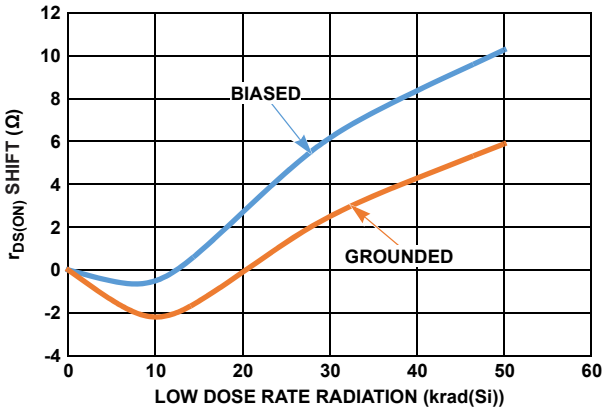


FIGURE 48. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

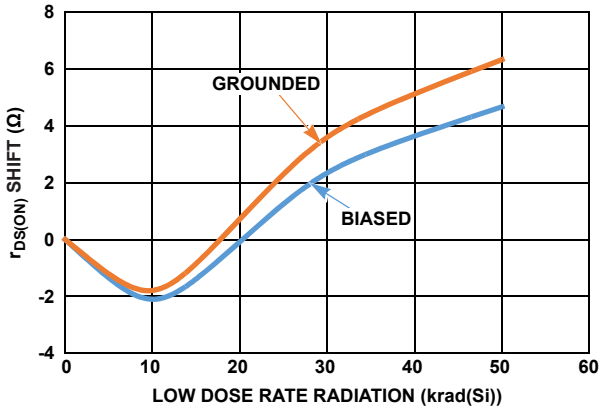


FIGURE 49. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

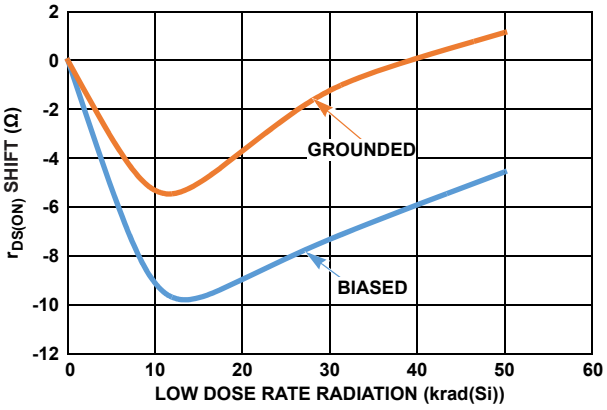


FIGURE 50. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

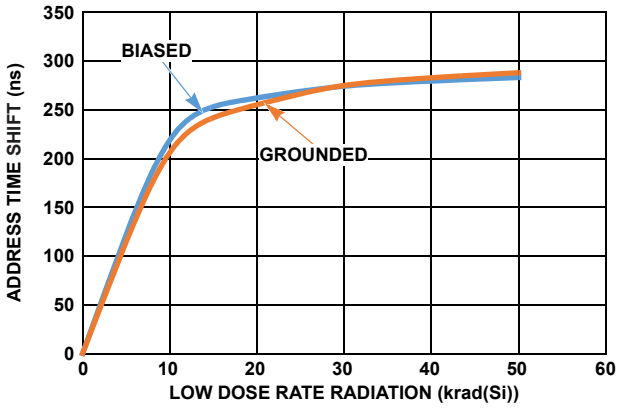


FIGURE 51. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

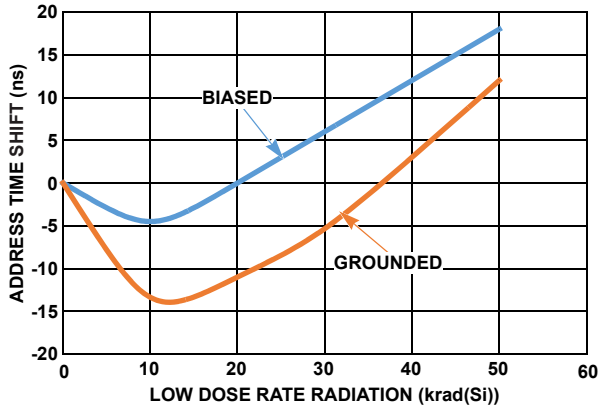


FIGURE 52. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

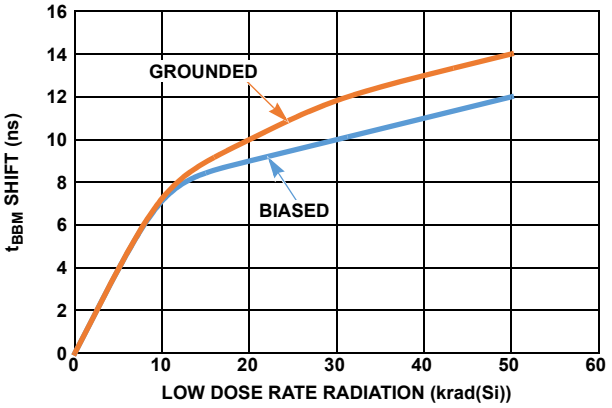


FIGURE 53. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

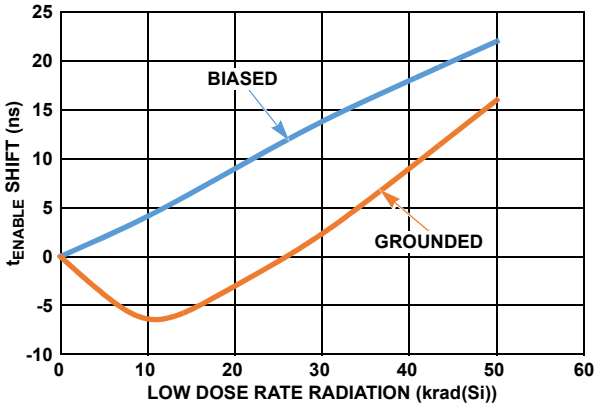


FIGURE 54. t_{ENABLE} SHIFT vs LDR RADIATION

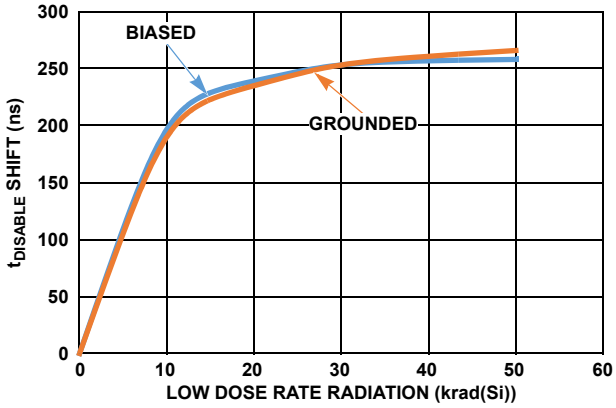


FIGURE 55. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+, V^-, and VREF; however, it is recommended that all supplies power up relatively close to each other.

Overvoltage Protection

The ISL73840SEH has overvoltage protection on both the input and the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition (3V to 4V) past the rail, the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL73840SEH. The range for VREF is between 4.5V and 5.5V with a nominal voltage of 5V. The address pins and enable are compared against roughly 30% of V_{REF} voltage (refer to Figure 56). With 5V on V_{REF}, the switching point is set to around 1.4V. This switching point allows for both 5V and 3.3V logic control.

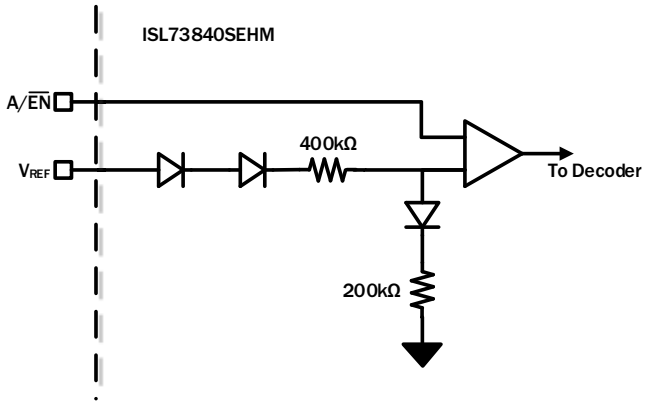


FIGURE 56. SIMPLIFIED V_{REF} CIRCUITRY

Considerations for Redundant Applications

When using the ISL73840SEH in a cold sparing application, it is recommended to keep the ground pin connected to system ground at all times. All supply pins (V+, V-, and VREF) should either be grounded or floating together.

If the supply pins are floating, it is recommended to place a high value bleed resistor (~1MΩ) in parallel with the decoupling capacitors on each supply pin to ensure that the supply voltage is discharged in a predictable manner. Figures 57 and 58 illustrate the recommended cold sparing setup for both shorted or floating supplies.

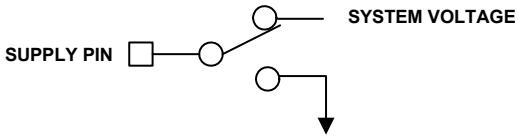


FIGURE 57. COLD SPARING SETUP WITH SUPPLIES SHORTED

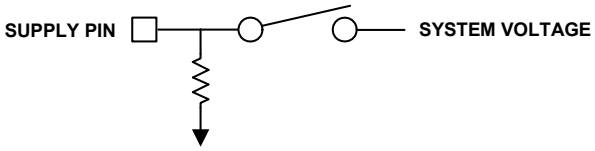


FIGURE 58. COLD SPARING SETUP WITH SUPPLIES FLOATING

ISL73840SEH vs ISL73841SEH

The ISL73841SEH, a 32-channel version of the ISL73840SEH, is available in a 48 Ld CQFP. The parts' performance specifications are very similar. Apart from the apparent increase in channel density, the ISL73841SEH has slightly higher output leakage compared to the ISL73840SEH because it has more channels connected to the output. The supply current for the ISL73841SEH is also slightly higher compared to the ISL73840SEH. Refer to Table 1 on page 3 for a comparison of the two devices.

Die Characteristics

Die Dimensions

2820µm x 4080µm (111 mils x 161 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6×10^5 A/cm^2

TRANSISTOR COUNT

5682

Weight of Packaged Device

2.096 grams

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package Pin 12

Metalization Mask Layout

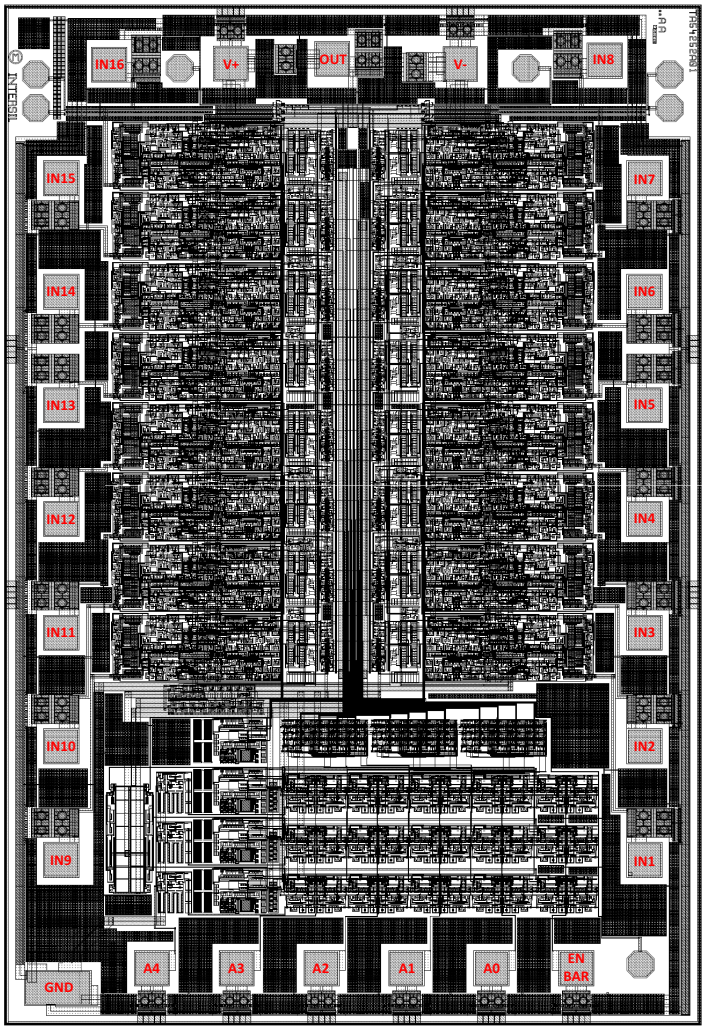


TABLE 3. ISL73840SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN8	P26	127	127	979.5	1768.5
3	V+	P27	125	125	417.5	1754.5
4	OUT	P28	125	125	-79.5	1774.5
5	V-	P1	125	125	-474.5	1756.5
7	IN16	P4	127	127	-947.5	1752.5
10	IN15	P5	127	127	-1133.5	1310.5
11	IN14	P6	127	127	-1133.5	868.5
12	IN13	P7	127	127	-1133.5	426.5
13	IN12	P8	127	127	-1133.5	-15.5
14	IN11	P9	127	127	-1133.5	-457.5
15	IN10	P10	127	127	-1133.5	-899.5
16	IN9	P11	127	127	-1133.5	-1341.5
17	GND	P12	250	125	-1147	-1839.5
18	VREF	P13	127	127	-781.5	-1763.5
19	A3	P14	127	127	-451.5	-1763.5
20	A2	P15	127	127	-121.5	-1763.5
21	A1	P16	127	127	208.5	-1763.5
22	A0	P17	127	127	538.5	-1763.5
23	EN_B	P18	127	127	868.5	-1763.5
25	IN1	P19	127	127	1133.5	-1341.5
26	IN2	P20	127	127	1133.5	-899.5
27	IN3	P21	127	127	1133.5	-457.5
28	IN4	P22	127	127	1133.5	-15.5
29	IN5	P23	127	127	1133.5	426.5
30	IN6	P24	127	127	1133.5	868.5
31	IN7	P25	127	127	1133.5	1310.5

NOTE: Origin of coordinates is the center of the die.

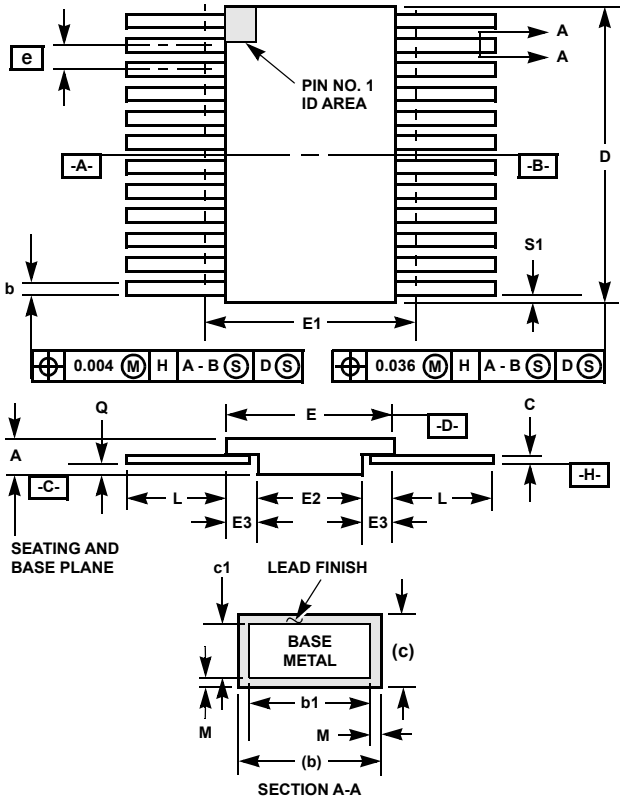
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Aug 10, 2023	4.00	Removed Related Literature section. Updated Ordering Information table and notes In ABS MAX RATINGS Section on page 5 changed Digital Input Voltage Range ($\overline{EN}$, Ax) from “GND to V+” to “GND - 0.3V to +16.5V”. Updates to the Electrical Specifications (±15V) table are as follows: • On page 5, for parameters Channel On-Resistance, r_{ON} Match Between Channels, and ON-Resistance Flatness added $V_{\overline{EN}}$ = 0V to the Test Conditions. • On page 6, for parameter Switch Off Leakage with Device Powered OFF changed it to Switch Off Leakage with Device Powered OPEN. • On page 6, added new parameter Switch On Leakage Current into the Drain (Overvoltage) specifications. • On page 6, for parameter Switch On Leakage Current into the Source (Overvoltage) update the limits values and units to µA. • On page 6, for parameter Switch Off Leakage Current into the Source (Overvoltage) added a new T_A = -55°C” specification. • On page 7, for parameter Switch On Leakage Current into the Source/Drain added $V_{\overline{EN}}$ = 0V to the Test Conditions. • Changed the I+, I- Quiescent & Standby Supply Current parameters to V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V. • Changed parameter nomenclature for Supply Current Into V_{REF} to Quiescent Supply Current Into V_{REF}. • Added new specification parameter Standby Current Into V_{REF}. Updates to the Electrical Specifications (±12V) table on page 8 are as follows: • On page 8, for parameters Channel On-Resistance, r_{ON} Match Between Channels, and ON-Resistance Flatness added $V_{\overline{EN}}$ = 0V to the Test Conditions. • Changed the I+, I- Quiescent & Standby Supply Current parameters to V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V. • Changed parameter nomenclature for Supply Current Into V_{REF} to Quiescent Supply Current Into V_{REF}. • Added new specification parameter Standby Current Into V_{REF}.
Feb 23, 2018	3.00	Added “Considerations for Redundant Applications” on page 19. Removed About Intersil and updated disclaimer.
Dec 7, 2017	2.00	Added Related Literature section on page 1. Added Note 4 to Ordering Information on page 3. Added ESD circuit images in Figure 3 on page 4.
May 31, 2016	1.00	Added SMD in Features. Updated Ordering Information table on page 3. Updated header in 1st and 2nd columns of “Electrical Specifications (±15V)” on page 5 and “Electrical Specifications (±12V)” on page 8 from “Parameter” and “Description” to “Symbol” and “Parameter”
May 13, 2016	0.00	Initial release

Package Outline Drawing

For the most recent package outline drawing, see K28.A.



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.