ISL6336D

VR11.1, 6-Phase PWM Controller with Phase Dropping, Droop Disabled and Load Current Monitoring Features

FN8320
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The ISL6336D controls voltage regulators by driving up to 6 interleaved synchronous-rectified buck channels in parallel. This multiphase architecture results in multiplying channel ripple frequency and reducing input and output ripple currents. Lower ripple results in fewer components, lower cost, reduced power dissipation, and smaller implementation area.

The ISL6336D utilizes Intersil's proprietary Active Pulse Positioning (APP), Adaptive Phase Alignment (APA) modulation scheme, active phase adding and dropping to achieve and maintain the extremely fast transient response with fewer output capacitors and high efficiency from light to full load.

The ISL6336D is designed to be completely compliant with Intel VR11.1 specifications with exception of droop disabled. It accurately reports the load current via the IMON pin to the microprocessor, which sends an active low PSI# signal to the controller at low power mode. The controller then enters 1- or 2-phase operation option to reduce magnetic core and switching losses, yielding high efficiency at light load. After the PSI# signal is deasserted, the dropped phase(s) are added back to sustain heavy load transient response and efficiency.

The ISL6336D senses the output current continuously by utilizing patented techniques to measure the voltage across the dedicated current sense resistor or the DCR of the output inductor. Current sensing circuits also provide the needed signals for channel-current balancing, average overcurrent protection and individual phase current limiting. An NTC thermistor's temperature is sensed via the TM pin and internally digitized for thermal monitoring and for integrated thermal compensation of the current sense elements.

A unity gain, differential amplifier is provided for remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL6336D with any other voltage rail. Dynamic VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting.

Features

- Intel VR11.1 compliant with droop disabled
- Proprietary active pulse positioning (APP) and adaptive phase alignment (APA) modulation scheme
- Proprietary active phase adding and dropping for high light load efficiency
- Precision multiphase core voltage regulation
  - Differential remote voltage sensing
  - ±0.5% closed-loop system accuracy over load, line and temperature
  - Bidirectional, adjustable reference-voltage offset
- Precision resistor or DCR differential current sensing
  - Accurate channel-current balancing
  - Accurate load current monitoring via IMON pin
- Microprocessor voltage identification input
  - Dynamic VID™ technology for VR11.1 requirement
  - 8-bit VID, VR11 compatible
- Average overcurrent protection and channel current limit
- Precision overcurrent protection on IMON pin
- Thermal monitoring and overvoltage protection
- Integrated programmable temperature compensation
- Integrated open sense line protection
- 1- to 6-phase operation, coupled inductor compatibility
- Adjustable switching frequency up to 1MHz per phase
- Package option
  - QFN compliant to JEDEC PUB95 MO-220 QFN - quad flat no leads - product outline
- Pb-free (RoHS compliant)

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Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6336DIRZ	ISL6336D IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7

NOTES:

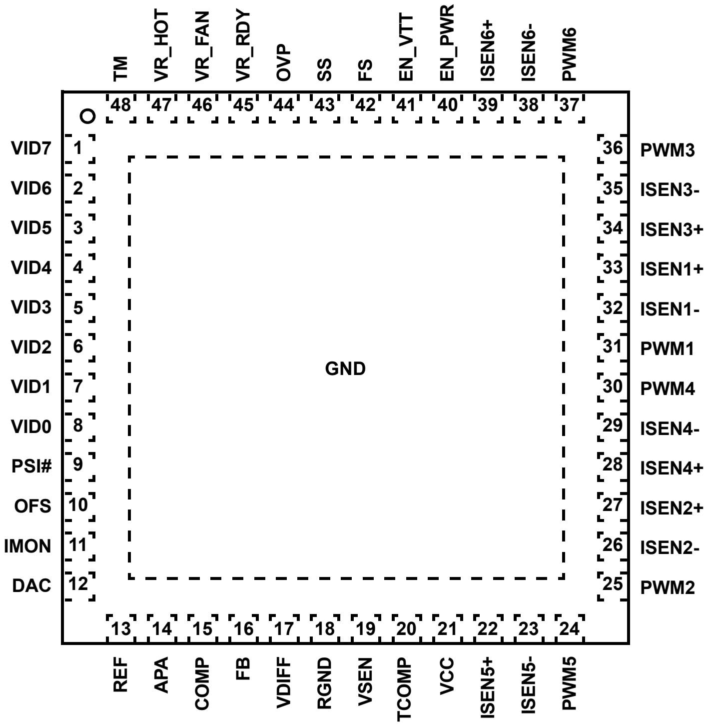
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6336D. For more information on MSL please see TB363.

TABLE 1. ISL6336x/4x FAMILY SUMMARY

INTERSIL PN	NUMBER OF PHASES	DIODE EMULATION	DROOP	H_CPURST_N INPUT	TARGETED APPLICATIONS
ISL6336	6	Yes	Yes	No	VR11.x CPU
ISL6336A	6	No	Yes	No	VR11.x CPU
ISL6336B	6	Yes	Yes	Yes	VR11.x CPU
ISL6336D	6	No	No	No	General Purpose, Memory
ISL6334	4	Yes	Yes	No	VR11.x CPU
ISL6334A	4	No	Yes	No	VR11.x CPU
ISL6334B	4	Yes	Yes	Yes	VR11.x CPU
ISL6334C	4	No	No	Yes	VR11.x CPU
ISL6334D	4	No	No	No	General Purpose, Memory

Pin Configuration

ISL6336D
(48 LD QFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1, 2, 3, 4, 5, 6, 7, 8	VID7, VID6, VID5, VID4, VID3, VID2, VID1, VID0	These are the inputs to the internal DAC that generate the reference voltage for output regulation. All VID pins have no internal pull-up current sources until after TD3. Connect these pins either to open-drain outputs with external pull-up resistors or to active pull-up outputs, as high as VCC plus 0.3V.
9	PSI#	A low input signal indicates the low power mode operation of the processor. The controller drops the number of active phases to single or 2-phase operation, according to the logic on Table 2 on page 14. The PSI# pin, SS, and FS pins are used to program the controller in operation of noncoupled, 2-Phase coupled, or (n-x)-Phase coupled inductors when PSI# is asserted (active low). Different cases yield different PWM output behavior on both dropped phase(s) and remaining phase(s) as PSI# is asserted and deasserted. A high input signal pulls the controller back to normal operation.
10	OFS	The OFS pin can be used to program a DC offset current, which will generate a DC offset voltage between the REF and DAC pins. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated.
11	IMON	IMON is the output pin of sensed, thermally compensated (if internal thermal compensation is used) average current. The voltage at IMON pin is proportional to the load current and the resistor value, and internally clamped to 1.11V plus the remote ground potential difference. If the clamped voltage (1.11V) is triggered, it will initiate the overcurrent shutdown. By choosing the proper value for the resistor at IMON pin, the overcurrent trip level can be set to be lower than the fixed internal overcurrent threshold. During the dynamic VID, the OCP function of this pin is disabled to avoid false triggering. Tie it to GND if not used.
12, 13	DAC, REF	The DAC pin is the output of the precision internal DAC reference. The REF pin is the positive input of the Error Amplifier. In typical applications, a 1kΩ, 1% resistor is used between DAC and REF to generate a precision offset voltage. This voltage is proportional to the offset current determined by the offset resistor from OFS to ground or VCC. A capacitor is used between REF and ground to smooth the voltage transition during Dynamic VID™ operations.
14	APA	The APA pin is used to adjust the Adaptive Phase Alignment trip level. A 50µA current source flows into this pin. A resistor connected from this pin to COMP sets the voltage trip level. A small decoupling capacitor should be placed in parallel with the resistor for high frequency decoupling.

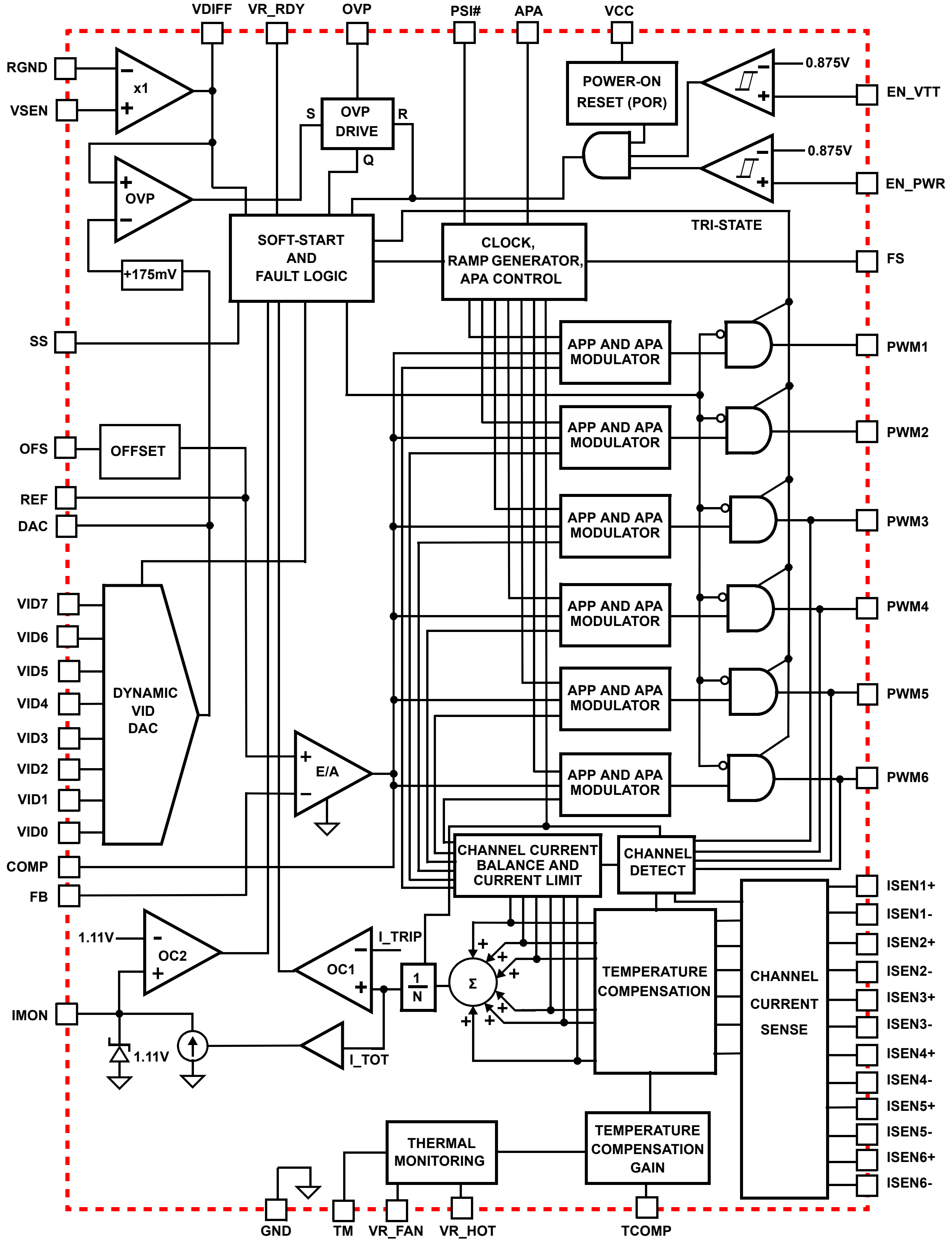
Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
16, 15	FB, COMP	Inverting input and output of the error amplifier respectively. FB can be connected to VDIFF through a resistor. COMP is tied back to FB through an external R-C network to compensate the regulator.
17, 19, 18	VDIFF, VSEN, RGND	VSEN and RGND form the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and RGND to the sense pins of the remote load.
20	TCOMP	Temperature compensation scaling input. The voltage sensed on the TM pin is utilized as the temperature input to adjust IMON and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element. To implement the integrated temperature compensation, a resistor divider circuit is needed with one resistor being connected from TCOMP to VCC of the controller and another resistor being connected from TCOMP to GND. Changing the ratio of the resistor values will set the gain of the integrated thermal compensation. When integrated temperature compensation function is not used, connect TCOMP to GND.
21	VCC	Supplies the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply.
22, 23, 26, 27, 28, 29, 32, 33, 34, 35, 38, 39	ISEN5+, ISEN5-, ISEN2-, ISEN2+, ISEN4+, ISEN4-, ISEN1-, ISEN1+, ISEN3+, ISEN3-, ISEN6-, ISEN6+	The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers. The sensed current is used for channel current balancing and overcurrent protection. Inactive channels should have their respective current sense inputs left open (for example, open ISEN6+ and ISEN6- for 5-phase operation). For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sense current is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISEN}. To match the time delay of the internal circuit, a capacitor is needed between each ISEN+ pin and GND, as described in "Current Sensing" on page 14.
24, 25, 30, 31, 36, 37	PWM5, PWM2, PWM4, PWM1, PWM3, PWM6	Pulse width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC. The number of active channels is determined by the state of PWM2, PWM3, PWM4, PWM5 and PWM6. Tie PWM2 to VCC to configure for 1-phase operation. Tie PWM3 to VCC to configure for 2-phase operation. Tie PWM4 to VCC to configure for 3-phase operation. Tie PWM5 to VCC to configure for 4-phase operation. Tie PWM6 to VCC to configure for 5-phase operation. In addition, tie PSI# to GND to configure for single phase operation as well.
40	EN_PWR	This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN_PWR through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN_PWR is driven above 0.875V, the ISL6336D is active depending on status of the EN_VTT, the internal POR, and pending fault states. Driving EN_PWR below 0.745V will clear all fault states and prime the ISL6336D to soft-start when reenabled.
41	EN_VTT	This pin is another threshold-sensitive enable input for the controller. It's typically connected to VTT output of VTT voltage regulator in the computer mother board. When EN_VTT is driven above 0.875V, the ISL6336D is active depending on status of the EN_PWR, the internal POR, and pending fault states. Driving EN_VTT below 0.745V will clear all fault states and prime the ISL6336D to soft-start when reenabled.
42	FS	Use this pin to set up the desired switching frequency. A resistor placed from FS to ground/VCC will set the switching frequency. The relationship between the value of the resistor and the switching frequency will be approximated by Equation 3. This pin is also used with SS and PSI# pins for phase dropping decoding (see Table 2 on page 14).
43	SS	Use this pin to set up the desired start-up oscillator frequency. A resistor placed from SS to ground/VCC will set up the soft-start ramp rate. The relationship between the value of the resistor and the soft-start ramp-up time will be approximated by Equations 14 and 15. This pin is also used with FS and PSI# pins for phase dropping decoding (see Table 2 on page 14).
44	OVP	The overvoltage protection output indication pin. This pin can be pulled to VCC and is latched when an overvoltage condition is detected. When the OVP indication is not used, keep this pin open.
45	VR_RDY	VR_RDY indicates that soft-start has completed and the output voltage is within the regulated range around the VID setting. It is an open-drain logic output. When OCP or OVP occurs, VR_RDY will be pulled to low. It will also be pulled low if the output voltage is below the undervoltage threshold.
46	VR_FAN	VR_FAN is an output pin with open-drain logic output. It will be pulled low if the measured VR temperature is less than a certain level, and open when the measured VR temperature reaches a certain level. An external pull-up resistor is needed.

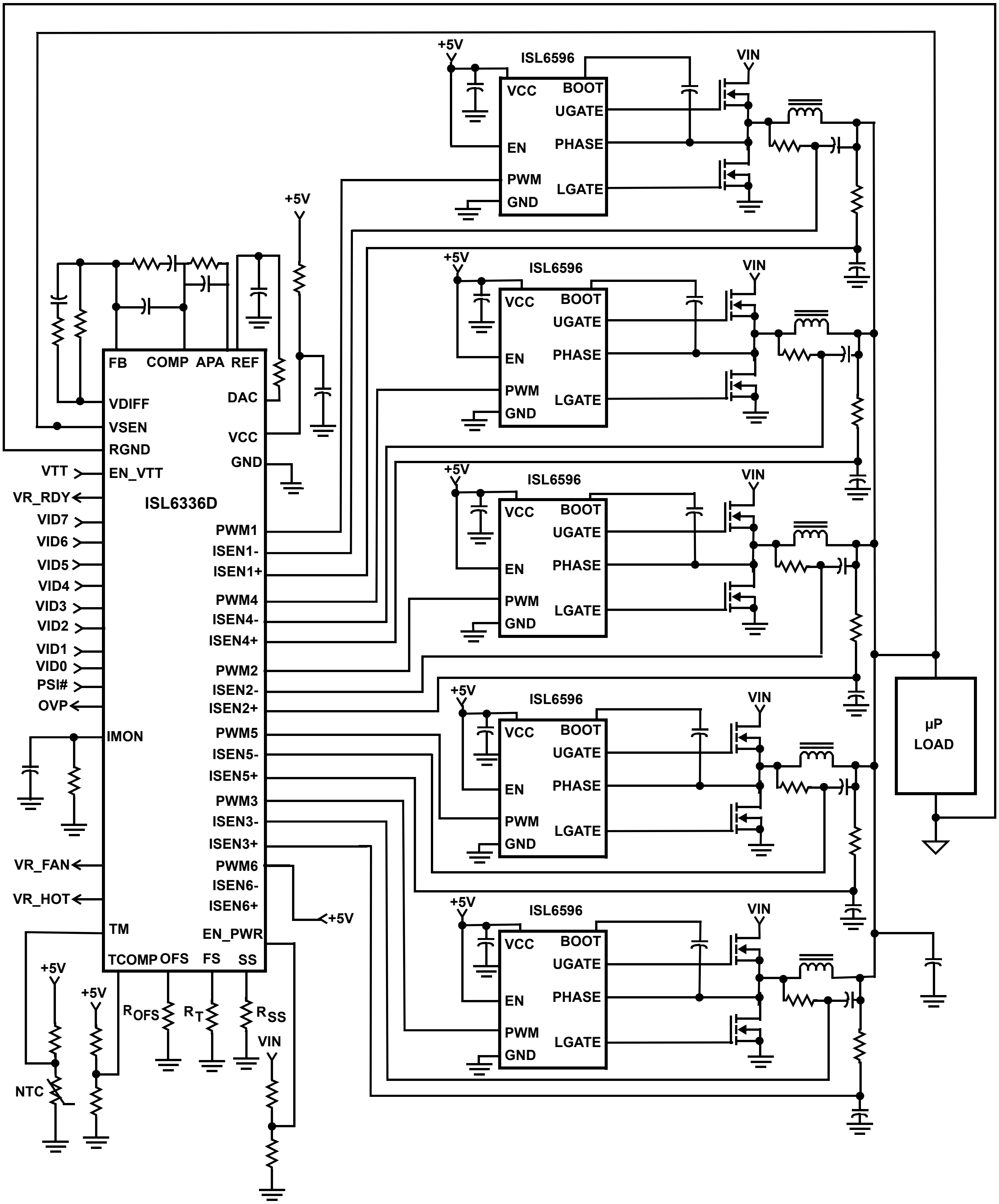
Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
47	VR_HOT	VR_HOT is used as an indication of high VR temperature. It is an open-drain logic output. It will be pulled low if the measured VR temperature is less than a certain level, and open when the measured VR temperature reaches a certain level. An external pull-up resistor is needed.
48	TM	TM is an input pin for the VR temperature measurement. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is reverse proportional to the VR temperature. The ISL6336D monitors the VR temperature based on the voltage at the TM pin and outputs VR_HOT and VR_FAN signals.
	GND	Bias and reference ground for the IC. The bottom metal base of ISL6336D is the GND.

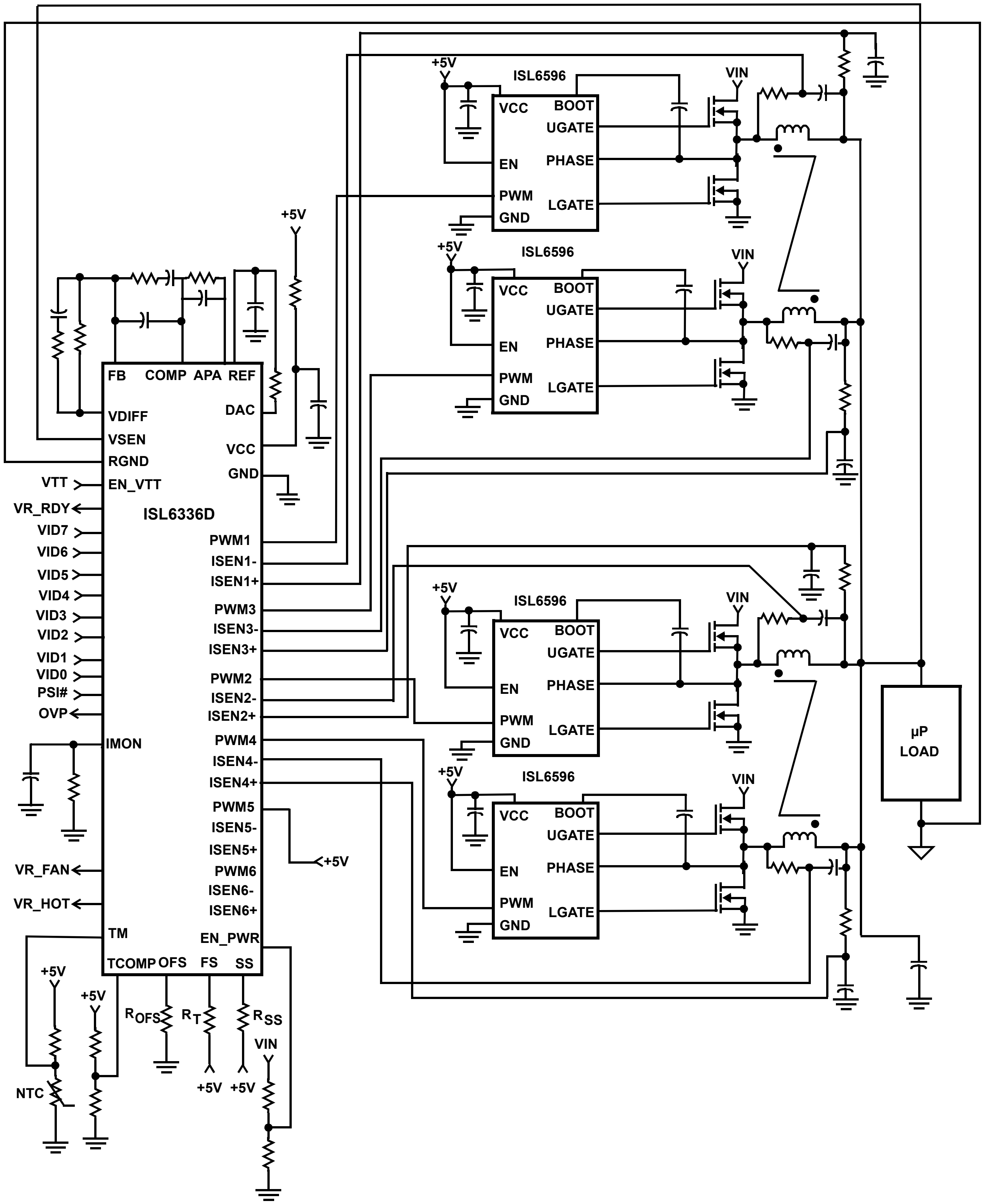
ISL6336D Block Diagram



Typical Application: 5-Phase VR with PSI# and No Droop



Typical Application - 4-Phase Couple Inductor VR with 2-Phase PSI# and No Droop



Absolute Maximum Ratings

Supply Voltage, VCC	+6V
All Pins	GND -0.3V to V_{CC} + 0.3V

Operating Conditions

Supply Voltage, VCC	+5V ±5%
Ambient Temperature	
ISL6336DIRZ	-40°C to +85°C
ESD Rating	
Human Body Model (Tested per JESD22-A114E)	2.5kV
Charged Device Model (Tested per JESD22-C101F	1.5kV
Machine Model (Tested per JESD22-A115-A)	200V
Latch-up (Tested per JESD-78B; Class 2, Level A)	100mA at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld 7x7 QFN Package (Notes 4, 5)	29	2

Maximum Junction Temperature	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, Unless Otherwise Specified. **Boldface limits apply across the operating temperature ranges, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN_PWR = 5VDC; R_T = 100kΩ, ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80µA	-	16	**20**	mA
Shutdown Supply	VCC = 5VDC; EN_PWR = 0VDC; R_T = 100kΩ	-	14	**17**	mA
POWER-ON RESET AND ENABLE					
VCC Rising POR Threshold		**4.3**	4.4	**4.5**	V
VCC Falling POR Threshold		**3.75**	3.88	**4.0**	V
EN_PWR Rising Threshold		**0.830**	0.850	**0.870**	V
EN_PWR Falling Threshold		**0.735**	0.752	**0.770**	V
EN_VTT Rising Threshold		**0.830**	0.850	**0.870**	V
EN_VTT Falling Threshold		**0.735**	0.752	**0.770**	V
REFERENCE VOLTAGE AND DAC					
System Accuracy of ISL6336DIRZ (VID = 1V to 1.6V, T_J = -40°C to +85°C)	(Note 7, Closed-Loop)	**-0.6**	-	**0.6**	%VID
System Accuracy of ISL6336DIRZ (VID = 0.8V to 1V, T_J = -40°C to +85°C)	(Note 7, Closed-Loop)	**-6**	-	**6**	mV
System Accuracy of ISL6336DIRZ (VID = 0.5V to 0.8V, T_J = -40°C to +85°C)	(Note 7, Closed-Loop)	**-7**	-	**7**	mV
VID Pull-up	After t_{D3}	**30**	40	**50**	µA
VID Input Low Level		**-**	-	**0.4**	V
VID Input High Level		**0.8**	-	**-**	V
Max DAC Source Current		**3.5**	-	**-**	mA
Max DAC Sink Current		**100**	-	**-**	µA
Max REF Source/Sink Current	(Note 8)	**50**	-	**-**	µA

Electrical Specifications

Operating Conditions: V_{CC} = 5V, Unless Otherwise Specified. **Boldface limits apply across the operating temperature ranges, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
PIN-ADJUSTABLE OFFSET					
Voltage at OFS Pin	Offset resistor connected to ground	**390**	400	**415**	mV
	Voltage below VCC, offset resistor connected to VCC	**1.574**	1.60	**1.635**	V
OSCILLATORS					
Accuracy of Switching Frequency Setting	R_T = 100kΩ	**225**	250	**275**	kHz
Adjustment Range of Switching Frequency	(Note 8)	**0.08**	-	**1.0**	MHz
Soft-start Ramp Rate	R_{SS} = 100kΩ (Notes 8, 9, 10)	-	1.563	-	mV/µs
Adjustment Range of Soft-Start Ramp Rate	(Note 8)	**0.625**	-	**6.25**	mV/µs
PWM GENERATOR					
Sawtooth Amplitude	(Note 8)	-	1.5	-	V
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground (Note 8)	-	96	-	dB
Open-Loop Bandwidth	(Note 8)	-	80	-	MHz
Slew Rate	(Note 8)	-	25	-	V/µs
Maximum Output Voltage		**3.8**	4.4	**4.9**	V
Output High Voltage at 2mA		**3.6**	-	-	V
Output Low Voltage at 2mA		-	-	**1.6**	V
REMOTE-SENSE AMPLIFIER (Note 8)					
Bandwidth		-	20	-	MHz
Output High Current	VSEN - RGND = 2.5V	**-500**	-	**500**	µA
Output High Current	VSEN - RGND = 0.6	**-500**	-	**500**	µA
PWM OUTPUT					
Sink Impedance	PWM = Low with 1mA Load	**100**	220	**300**	Ω
Source Impedance	PWM = High, Forced to 3.7V	**200**	320	**400**	Ω
PSI# INPUT					
Low Signal Threshold		-	-	**0.4**	V
High Signal Threshold		**0.8**	-	-	V
CURRENT SENSE AND OVERCURRENT PROTECTION					
Sensed Current Tolerance	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 40µA; CS Offset and Mirror Error Included, R_{ISENx} = 200Ω	**36.5**	-	**42**	µA
	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80µA; CS Offset and Mirror Error Included, R_{ISENx} = 200Ω	**74**	-	**83**	µA
Overcurrent Trip Level for Average Current At Normal CCM PWM Mode (PSI# = 1)	CS Offset and Mirror Error Included, R_{ISENx} = 200Ω	**96**	105	**117**	µA
Overcurrent Trip Level for Average Current at PSI# Mode (PSI# = 0)	N = 6, Drop to 1-Phase	-	135	-	µA
Peak Current Limit for Individual Channel		**115**	129	**146**	µA
IMON Clamped and OCP Trip Level		**1.085**	1.11	**1.14**	V

Electrical Specifications Operating Conditions: V_{CC} = 5V, Unless Otherwise Specified. **Boldface limits apply across the operating temperature ranges, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
THERMAL MONITORING AND FAN CONTROL					
TM Input Voltage for VR_FAN Trip		**38.7**	39.1	**39.6**	%VCC
TM Input Voltage for VR_FAN Reset		**44.6**	45.1	**45.5**	%VCC
TM Input Voltage for VR_HOT Trip		**32.9**	33.3	**33.7**	%VCC
TM Input Voltage for VR_HOT Reset		**38.7**	39.1	**39.6**	%VCC
Leakage Current of VR_FAN	With external pull-up resistor connected to VCC	-	-	**5**	µA
VR_FAN Low Voltage	With 1.24k resistor pull-up to VCC, I_{VR_FAN} = 4mA	-	-	**0.3**	V
Leakage Current of VR_HOT	With external pull-up resistor connected to VCC	-	-	**5**	µA
VR_HOT Low Voltage	With 1.24k resistor pull-up to VCC, I_{VR_HOT} = 4mA	-	-	**0.3**	V
VR READY AND PROTECTION MONITORS					
Leakage Current of VR_RDY	With pull-up resistor externally connected to VCC	-	-	**5**	µA
VR_RDY Low Voltage	I_{VR_RDY} = 4mA	-	-	**0.3**	V
Undervoltage Threshold	VDIFF Falling	**48**	50	**52**	%VID
VR_RDY Reset Voltage	VDIFF Rising	**57**	59.6	**62**	%VID
Overvoltage Protection Threshold	Before valid VID	**1.250**	1.273	**1.300**	V
	After valid VID, the voltage above VID	**158**	175	**190**	mV
Overvoltage Protection Reset Hysteresis		-	100	-	mV

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
8. Limits should be considered typical and are not production tested.
9. During soft-start, VDAC rises from 0V to 1.1V first and then ramp to VID voltage after receiving valid VID.
10. Soft-start ramp rate is determined by the adjustable soft-start oscillator frequency at the speed of 6.25mV per cycle.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter (which are both cost-effective and thermally viable), have forced a change to the cost-saving approach of multiphase. The ISL6336D controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagrams on pages 7, 8, and 9 provide top level views of multiphase power conversion using the ISL6336D controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency 3x greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has 3x the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The DC components of the inductor currents combine to feed the load.

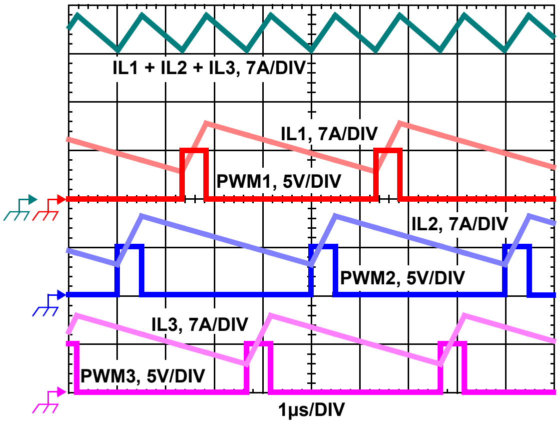


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_{SW} V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_{SW} is the switching frequency.

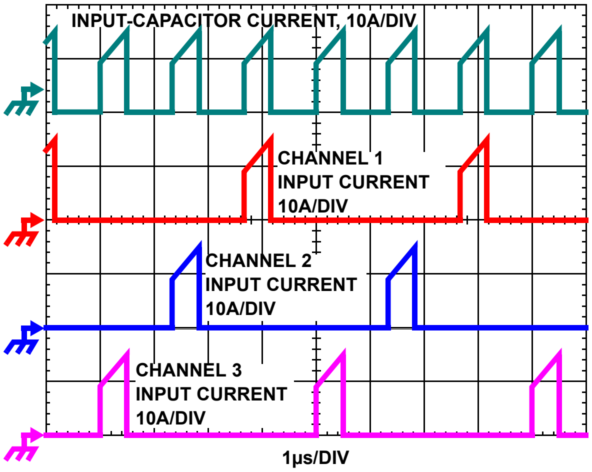


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{L f_{SW} V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a 3-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9ARMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent 3-phase converter.

Figures 23, 24 and 25 in the section entitled "Input Capacitor Selection" on page 27 can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 26 shows the single phase input-capacitor RMS current for comparison.

PWM Modulation Scheme

The ISL6336D adopts Intersil's proprietary Active Pulse Positioning (APP) modulation scheme to improve transient performance. APP control is a unique dual-edge PWM modulation scheme with both PWM leading and trailing edges being independently moved to give the best response to transient loads. The PWM frequency, however, is constant and set by the external resistor between the FS pin and GND. To further improve the transient response, the ISL6336D also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique. APA, with sufficiently large load step currents, can turn on all phases together. With both APP and APA control, ISL6336D can achieve excellent transient performance and reduce demand on the output capacitors.

Under steady state conditions, the operation of the ISL6336D PWM modulators appear to be that of a conventional trailing edge modulator. Conventional analysis and design methods can therefore be used for steady state and small signal operation.

PWM and PSI# Operation

The timing of each channel is set by the number of active channels. The default channel setting for the ISL6336D is four. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

For the default 6-channel operation, the channel firing order is 1-2-3-4-5-6. The PWM2 pulse happens 1/6 of a cycle after PWM1, the PWM3 pulse happens 1/6 of a cycle after PWM2, etc. In PSI# low power mode, the remaining active phase(s) is 1 and/or 4.

For 5-channel operation (PWM6 = 5V), the channel firing order is 1-2-3-4-5. In PSI# low power mode, the remaining active phase(s) is 1 and/or 3. For 4-channel operation (PWM5 = 5V), the channel firing order is 1-2-3-4. In PSI# low power mode, the remaining active phase(s) is 1 and/or 3.

Connecting PWM4 to VCC selects three channel operation and the pulse times are spaced in 1/3 cycle increments. In PSI# low power mode, the remaining active phase(s) is 1 and/or 2. If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse happens 1/2 of a cycle after PWM1 pulse. In PSI# low power mode, the remaining active phase(s) is 1 and/or 2. If PWM2 is connected to VCC, only Channel 1 operation is selected.

When PSI# is asserted low, indicating the low power mode operation of the processor, the controller drops the number of active phases according to the logic on Table 2 for high light-load efficiency performance. SS and FS pins are used to program the controller in operation of noncoupled, 2-phase coupled, or (n-x)-Phase coupled inductors. Different cases yield different PWM output behaviors on both dropped phase(s) and remaining phase(s) as PSI# is asserted and deasserted. A high PSI# input signal pulls the controller back to normal CCM PWM operation to sustain an immediate heavy transient load and high efficiency.

Note that "n-x" means n-x phase coupled and x-phase(s) are uncoupled.

TABLE 2. PSI# OPERATION DECODING

	PSI#	FS	SS
Non CI or (n-1) CI Drops to 1-phase	0	0	0
Non CI or (n-2) CI Drops to 2-phase	0	0	1
2-phase CI Drops to 1-phase	0	1	0
2-phase CI Drops to 2-phase	0	1	1
Normal CCM PWM Mode	1	x	x

While the controller is operational (VCC above POR, EN_VTT and EN_PWR are both high, valid VID inputs), it can pull the PWM pins to ~40% of VCC (~2V for 5V VCC bias) during various stages, such as soft-start delay, phase shedding operation, or fault conditions (OC or OV events). The matching driver's internal PWM resistor divider can further raise the PWM potential, but not lower it below the level set by the controller IC. Therefore, the controller's PWM outputs are directly compatible with Intersil drivers that require 5V PWM signal amplitudes. Drivers requiring 3.3V PWM signal amplitudes are generally incompatible.

Switching Frequency

Switching frequency is determined by the selection of the frequency-setting resistor, R_T, which is connected from FS pin to GND or VCC. Equation 3 and Figure 3 are provided to assist in selecting the correct resistor value.

$$R_T = \frac{2.5X10^{10}}{f_{SW}} \qquad \text{(EQ. 3)}$$

where f_{SW} is the switching frequency of each phase.

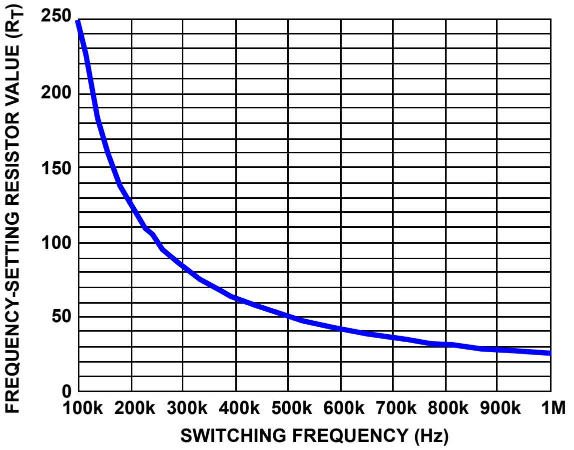


FIGURE 3. SWITCHING FREQUENCY vs RT

Current Sensing

The ISL6336D senses current continuously for fast response. The ISL6336D supports inductor DCR sensing, or resistive sensing techniques. The associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance and overcurrent protection.

The internal circuitry, shown in Figures 4 and 5, represents one channel of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM2, PWM3 and PWM4 pins, as described in "PWM and PSI# Operation" on page 14. The input bias current of the current sensing amplifier is typically 60nA; less than 5kΩ input impedance is preferred to minimized the offset error.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 4 shows the S-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \qquad \text{(EQ. 4)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 4.

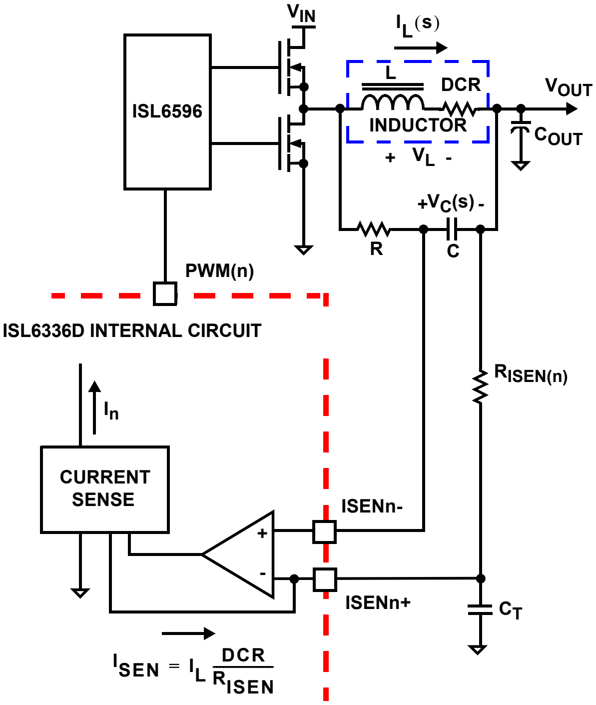


FIGURE 4. DCR SENSING CONFIGURATION

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L (see Equation 5).

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \qquad \text{(EQ. 5)}$$

If the R-C network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of ISEN+ pin, I_{SEN}, is proportional to the inductor current.

Because of the internal filter at ISEN- pin, one capacitor, C_T, is needed to match the time delay between the ISEN- and ISEN+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.

Equation 6 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \qquad \text{(EQ. 6)}$$

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Positive Temperature Coefficient (PTC) resistor can be selected for the sense resistor R_{ISEN}, or the integrated temperature compensation function of ISL6336D should be utilized. The integrated temperature compensation function is described in "External Temperature Compensation" on page 24.

RESISTIVE SENSING

For accurate current sense, a dedicated current-sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 5). This technique is more accurate, but reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

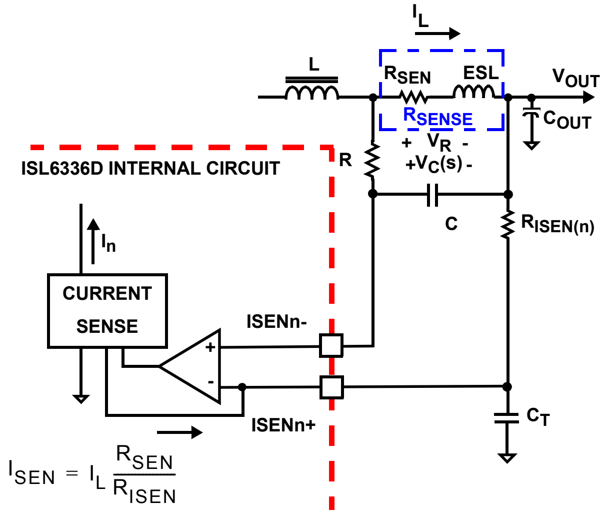


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

A current sensing resistor has a distributed parasitic inductance, known as ESL (equivalent series inductance, typically less than 1nH) parameter. Consider the ESL as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, will also pass through the ESL. Equation 7 shows the s-domain equivalent voltage across the resistor V_R.

$$V_R(s) = I_L \cdot (s \cdot ESL + R_{SEN}) \qquad \text{(EQ. 7)}$$

A simple R-C network across the current sense resistor extracts the R_{SEN} voltage, as shown in Figure 5.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L. See Equation 8.

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \qquad \text{(EQ. 8)}$$

If the R-C network components are selected such that the RC time constant matches the ESL-RSEN time constant (R*C = ESL/R_{SEN}), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, i.e., proportional to the channel current. As an example, a typical 1mΩ sense resistor can use R = 348 and C = 820pF for the matching. Figures 6 and 7 show the sensed waveforms without and with matching RC when using resistive sense.

Because of the internal filter at the ISENn- pin, one capacitor, C_T, is needed to match the time delay between the ISENn- and ISENn+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.

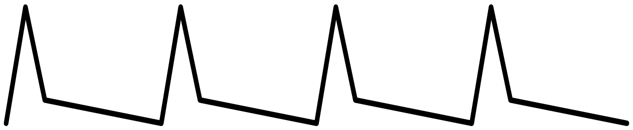


FIGURE 6. VOLTAGE ACROSS R WITHOUT RC

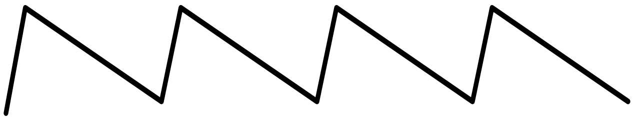


FIGURE 7. VOLTAGE ACROSS C WITH MATCHING RC

Equation 9 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} \qquad \text{(EQ. 9)}$$

L/DCR OR ESL/R_{SEN} MATCHING

Assuming the compensator design is correct, Figure 8 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current has a square change, the IMON voltage (VIMON) without a decoupling capacitor also has a square response. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R_{SEN} matching calculation. Fine tuning the matching is necessarily done in the board level to improve overall transient performance and system reliability.

If the R-C timing constant is too large or too small, V_C(s) will not accurately represent real-time I_{OUT}(s) and will worsen fault response at the transient event. Figure 9 shows the IMON transient voltage response when the R-C timing constant is too small. V_{IMON} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 10 shows the transient response when the R-C timing constant is too large. V_{IMON} is sluggish in reaching its final value. The excessive delay on current sensing will not provide a fast OCP response and hurt system reliability.

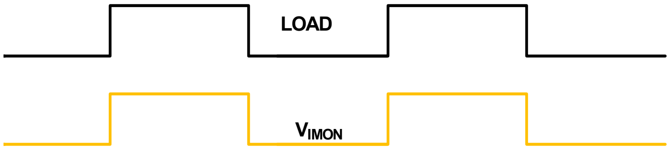


FIGURE 8. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

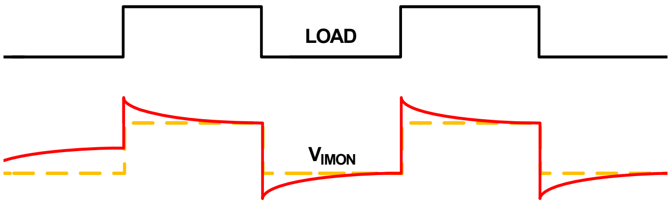


FIGURE 9. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

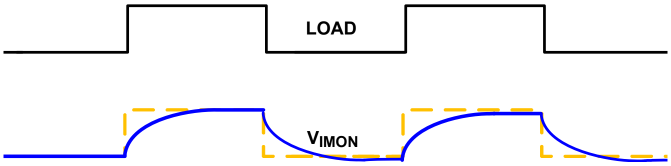


FIGURE 10. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

Channel-Current Balance

The sensed current I_n from each active channel is summed together and divided by the number of active channels. The resulting average current I_{AVG} provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWM duty cycle of each channel with Intersil's patented current-balance method.

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

Voltage Regulation

The compensation network shown in Figure 11 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6336D to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is compared to sawtooth waveforms to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry, which control voltage regulation, are illustrated in Figure 11.

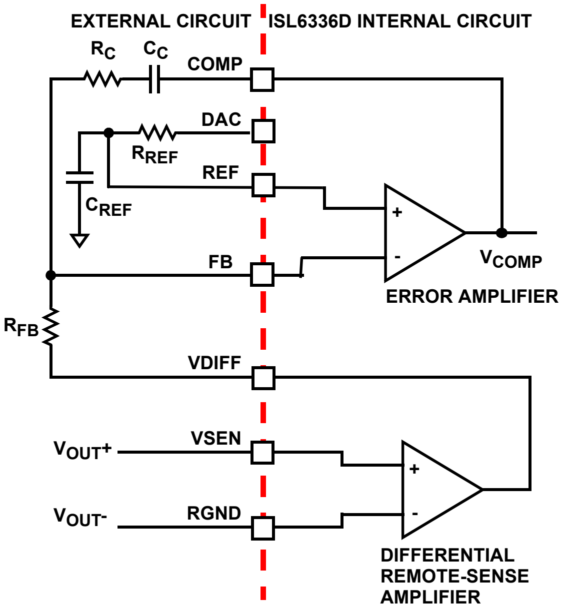


FIGURE 11. OUTPUT VOLTAGE REGULATION LOOP

The ISL6336D incorporates an internal differential remote sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the noninverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF}, is connected to the inverting input of the error amplifier through an external resistor.

A digital-to-analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID7 through VID0. The DAC decodes the eight 6-bit logic signal (VID) into one of the discrete voltages shown in Table 3. All VID pins have no internal pull-up current sources before t_{D3}. After t_{D3}, each VID input offers a minimum 30µA pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources in case leakage into the driving device is greater than 30µA.

TABLE 3. VR11 VID 8-BIT

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625

TABLE 3. VR11 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625

TABLE 3. VR11 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625

TABLE 3. VR11 VID 8-BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Output-Voltage Offset Programming

The ISL6336D allows the designer to accurately adjust the offset voltage. When a resistor, R_{OFS}, is connected between OFS to VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into OFS. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.4V, and I_{OFS} flows out of OFS. A resistor between DAC and REF, R_{REF}, is selected so that the product (I_{OFS} x R_{OFS}) is equal to the desired offset voltage. These functions are shown in Figure 12.

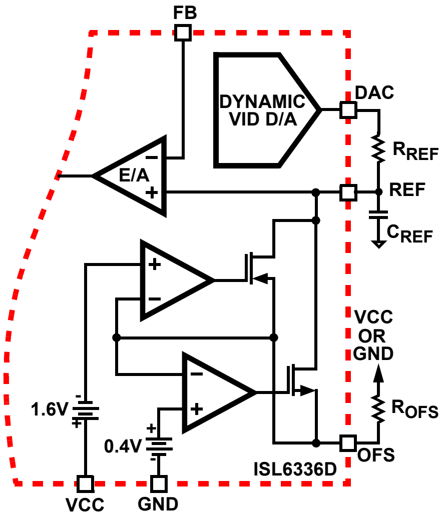


FIGURE 12. OUTPUT VOLTAGE OFFSET PROGRAMMING

Once the desired output offset voltage has been determined, use Equations 10 and 11 to calculate R_{OFS}.

For Positive Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.6 \times R_{REF}}{V_{OFFSET}} \quad \text{(EQ. 10)}$$

For Negative Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.4 \times R_{REF}}{V_{OFFSET}} \quad \text{(EQ. 11)}$$

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs during regulator operation. The power management solution is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

In order to ensure the smooth transition of output voltage during VID change, a VID step change smoothing network, composed of R_{REF} and C_{REF}, as shown in Figure 12, can be used. The selection of R_{REF} is based on the desired offset voltage, as detailed in "Output-Voltage Offset Programming" on page 19. The selection of C_{REF} is based on the time duration for 1-bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1-bit every t_{VID}, the relationship between the time constant of R_{REF} and C_{REF} network and t_{VID} is given by Equation 12.

$$C_{REF}R_{REF} = t_{VID} \quad \text{(EQ. 12)}$$

During dynamic VID transition and VID step-up, the overcurrent trip point increases by 140% to avoid falsely triggering OCP circuits, while the overvoltage trip point is set to its maximum VID OVP trip level. If the dynamic VID occurs at PSI# asserted, the system should exit PSI# and complete the transition, and then resume PSI# operation 50µs after the transition.

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, VR_RDY asserts logic high.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the ISL6336D is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6336D are guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, ISL6336D will not inadvertently turn off unless the bias voltage drops substantially (see "Electrical Specifications" table beginning on page 10).
2. The ISL6336D features an enable input (EN_PWR) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6336D in shutdown until the voltage at EN_PWR rises above 0.875V. The enable comparator has about 130mV of hysteresis to prevent bounce. It is important that the driver reaches its POR level before the ISL6336D becomes enabled. The schematic in Figure 13 demonstrates sequencing the ISL6336D with the ISL66xx family of Intersil MOSFET drivers, which require 12V bias.
3. The voltage on EN_VTT must be higher than 0.875V to enable the controller. This pin is typically connected to the output of VTT VR.

When all conditions previously mentioned are satisfied, ISL6336D begins the soft-start and ramps the output voltage to 1.1V first. After remaining at 1.1V for some time, ISL6336D reads the VID code at VID input pins. If the VID code is valid, ISL6336D will regulate the output to the final VID setting. If the VID code is OFF code, ISL6336D will shut down, and cycling VCC, EN_PWR or EN_VTT is needed to restart.

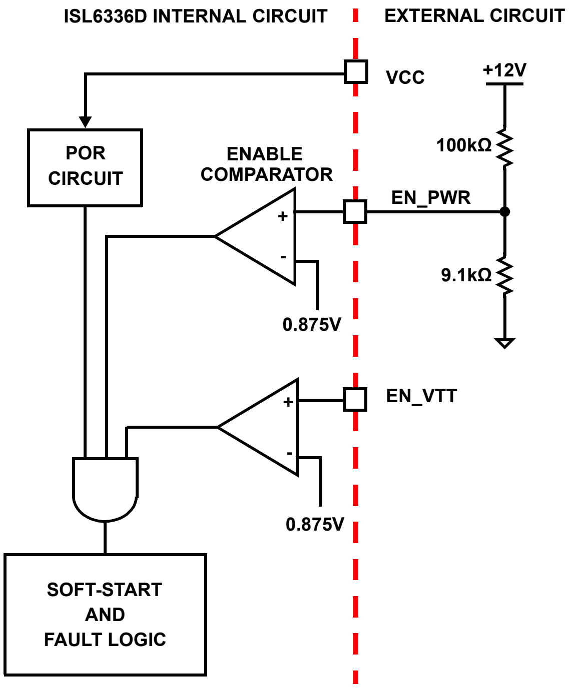


FIGURE 13. POWER SEQUENCING USING THRESHOLD SENSITIVE ENABLE (EN) FUNCTION

Soft-Start

ISL6336D based VR has 4 periods during soft-start, as shown in Figure 14. After VCC, EN_VTT and EN_PWR reach their POR/enable thresholds, the controller will have a fixed delay period t_{D1}. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V VBOOT voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed period t_{D3}. At the end of t_{D3} period, ISL6336D reads the VID signals. If the VID code is valid, ISL6336D will initiate the second soft-start ramp until the voltage reaches the VID voltage minus offset voltage.

The soft-start time is the sum of the 4 periods, as shown in Equation 13.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \quad \text{(EQ. 13)}$$

t_{D1} is a fixed delay with the typical value as 1.36ms. t_{D3} is determined by the fixed 85µs plus the time to obtain valid VID voltage. If the VID is valid before the output reaches the 1.1V, the minimum time to validate the VID input is 500ns. Therefore, the minimum t_{D3} is about 86µs.

During t_{D2} and t_{D4}, ISL6336D digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator, which is defined by the resistor R_{SS} from SS pin to GND. The second soft-start ramp time t_{D2} and t_{D4} can be calculated based on Equations 14 and 15:

$$t_{D2} = \frac{1.1xR_{SS}}{6.25x25}(\mu s) \quad \text{(EQ. 14)}$$

$$t_{D4} = \frac{(V_{VID} - 1.1)xR_{SS}}{6.25x25}(\mu s) \quad \text{(EQ. 15)}$$

For example, when VID is set to 1.5V and R_{SS} is set at 100kΩ, the first soft-start ramp time t_{D2} will be 704µs and the second soft-start ramp time t_{D4} will be 256µs.

After the DAC voltage reaches the final VID setting, VR_RDY will be set to high with the fixed delay t_{D5}. The typical value for t_{D5} is 85µs. Before the VR_RDY is released, the controller disregards the PSI# input and always operates in normal CCM PWM mode.

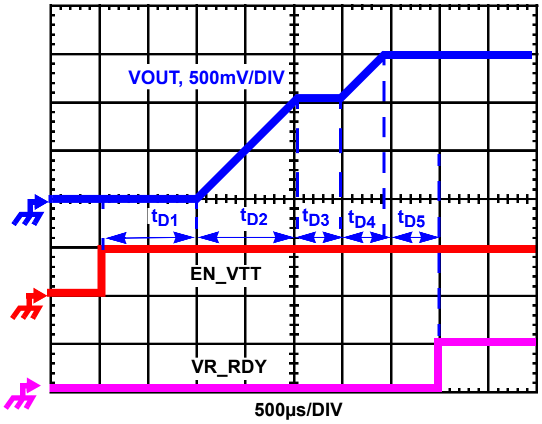


FIGURE 14. SOFT-START WAVEFORMS

Current Sense Output

The current flowing out of the IMON pin is equal to the sensed average current inside ISL6336D. In typical applications, a resistor is placed from the IMON pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 16:

$$V_{IMON} = \frac{R_{IOUT}}{N}\frac{R_X}{R_{ISEN}}I_{LOAD} \quad \text{(EQ. 16)}$$

where V_{IMON} is the voltage at the IMON pin, R_{IOUT} is the resistor between the IMON pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IMON pin to GND should be chosen to ensure that the voltage at the IMON pin is less than 1.11V under the maximum load current. If the IMON pin voltage is higher than 1.11V, overcurrent shutdown will be triggered, as described in "Overcurrent Protection" on page 22.

A small capacitor can be placed between the IMON pin and GND to reduce the noise impact. If this pin is not used, tie it to GND.

Fault Monitoring and Protection

The ISL6336D actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power-good indicator is provided for linking to external system monitors. The schematic in Figure 15 outlines the interaction between the fault monitors and the VR_RDY signal.

VR_RDY Signal

The VR_RDY pin is an open-drain logic output which indicates that the soft-start period is complete and the output voltage is within the regulated range. VR_RDY is pulled low during shutdown and releases high after a successful soft-start and a fixed delay t_{D5}. VR_RDY will be pulled low when an undervoltage or overvoltage condition is detected, or the controller is disabled by a reset from EN_PWR, EN_VTT, POR, or VID OFF-code.

Undervoltage Detection

The undervoltage threshold is set at 50% of the VID code. When the output voltage at VSEN is below the undervoltage threshold, VR_RDY is pulled low.

Overvoltage Protection

Regardless of the VR being enabled or not, the ISL6336D overvoltage protection (OVP) circuit will be active after its POR. The OVP thresholds are different under different operation conditions. When VR is not enabled and during the soft-start intervals t_{D1}, t_{D2} and t_{D3}, the OVP threshold is 1.273V. Once the controller detects valid VID input, the OVP trip point will be changed to DAC plus 175mV.

Two actions are taken by ISL6336D to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly (less than 20ns). This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level to avoid damaging the load. When the VDIFF voltage falls below the DAC plus 75mV, PWM signals enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, ISL6336D will again command the lower MOSFETs to turn on. The ISL6336D will continue to protect the load in this fashion as long as the overvoltage condition occurs.

Once an overvoltage condition is detected, normal PWM operation ceases until ISL6336D is reset. Cycling the voltage on EN_PWR, EN_VTT or VCC below the POR-falling threshold will reset the controller. Cycling the VID codes will not reset the controller.

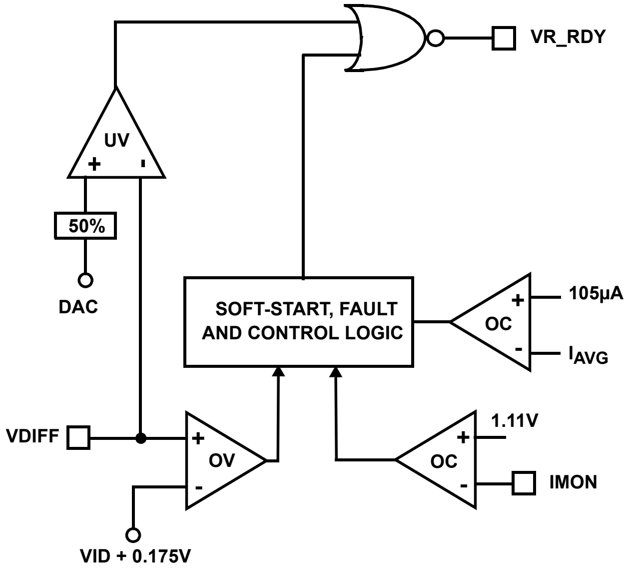


FIGURE 15. VR_RDY AND PROTECTION CIRCUITRY

Overcurrent Protection

The ISL6336D has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition by limiting its peak current, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, ISL6336D utilizes the sensed average current I_{AVG} to detect an overcurrent condition. See "Voltage Regulation" on page 16 for more details on how the average current is measured. The average current is continually compared with a constant 105µA reference current, as shown in Figure 15. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown.

The current out of IMON pin is equal to the sensed average current I_{AVG}. With a resistor from IMON to GND, the voltage at IMON will be proportional to the sensed average current and the resistor value. The ISL6336D continuously monitors the voltage at IMON pin. If the voltage at IMON pin is higher than 1.11V, a comparator triggers the overcurrent shutdown. By increasing the resistor between IMON and GND, the overcurrent protection threshold can be adjusted to be less than 105µA. For example, the overcurrent threshold for the sensed average current I_{AVG} can be set to 95µA by using a 11.8kΩ resistor from IMON to GND.

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state within 20ns, commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (see Figure 16) until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation.

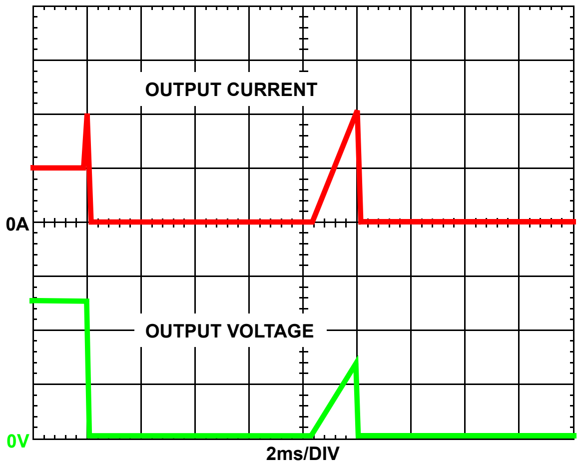


FIGURE 16. OVERCURRENT BEHAVIOR IN HICCUP MODE
f_{SW} = 500kHz

For the individual channel overcurrent protection, ISL6336D continuously compares the sensed current signal of each channel with the 129µA reference current. If one channel current exceeds the reference current, ISL6336D will pull the PWM signal of this channel to low for the rest of the switching cycle. This PWM signal can be turned on next cycle if the sensed channel current is less than the 129µA reference current. The peak current limit of an individual channel will not trigger the converter to shutdown.

Thermal Monitoring (VR_HOT/VR_FAN)

There are two thermal signals to indicate the temperature status of the voltage regulator: VR_HOT and VR_FAN. Both VR_FAN and VR_HOT pins are open-drain outputs, and external pull-up resistors are required. Those signals are valid only after the controller is enabled.

The VR_FAN signal indicates that the temperature of the voltage regulator is high and more cooling airflow is needed. The VR_HOT signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption. The VR_HOT signal may be tied to the CPU's PROC_HOT signal.

The diagram of thermal monitoring function block is shown in Figure 17. One NTC resistor should be placed close to the power stage of the voltage regulator to sense the operational temperature, and one pull-up resistor is needed to form the voltage divider for the TM pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the TM pin. Figure 18 shows the TM voltage over the temperature for a typical design with a recommended 6.8kΩ NTC (P/N: NTHS0805N02N6801 from Vishay) and 1kΩ resistor RTM1. We recommend using those resistors for the accurate temperature compensation.

There are two comparators with hysteresis to compare the TM pin voltage to the fixed thresholds for VR_FAN and VR_HOT signals respectively. The VR_FAN signal is set to high when the TM voltage is lower than 39.1% of VCC voltage, and is pulled to GND when the TM voltage increases to above 45.1% of VCC voltage. The VR_FAN signal is set to high when the TM voltage goes below 33.3% of VCC voltage, and is pulled to GND when the TM voltage goes back to above 39.1% of VCC voltage. Figure 19 shows the operation of those signals.

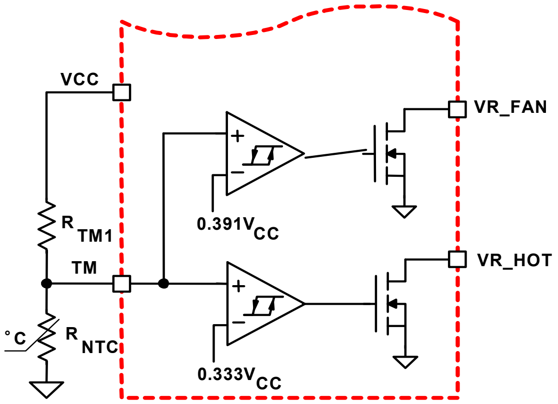


FIGURE 17. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

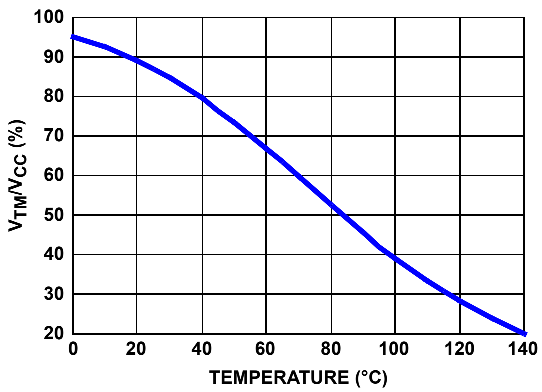


FIGURE 18. THE RATIO OF TM VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PARTS

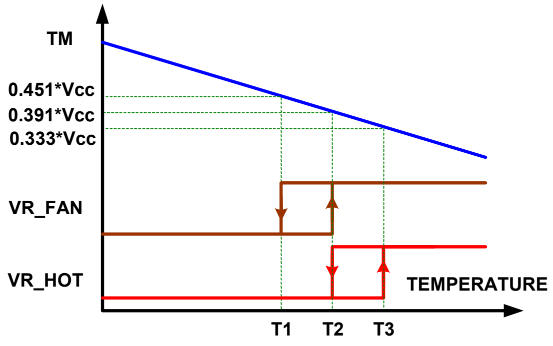


FIGURE 19. VR_HOT AND VR_FAN SIGNAL vs TM VOLTAGE

Based on the NTC temperature characteristics and the desired threshold of the VR_HOT signal, the pull-up resistor RTM1 of TM pin is given by Equation 17:

$$R_{TM1} = 2.75xR_{NTC(T3)} \quad \text{(EQ. 17)}$$

$R_{NTC(T3)}$ is the NTC resistance at the VR_HOT threshold temperature T3.

The NTC resistance at the set point T2 and release point T1 of VR_FAN signal can be calculated as shown in Equations 18 and 19:

$$R_{NTC(T2)} = 1.267xR_{NTC(T3)} \quad \text{(EQ. 18)}$$

$$R_{NTC(T1)} = 1.644xR_{NTC(T3)} \quad \text{(EQ. 19)}$$

With the NTC resistance value obtained from Equations 18 and 19, the temperature value T2 and T1 can be found from the NTC datasheet.

Temperature Compensation

The ISL6336D supports inductor DCR sensing, or resistive sensing techniques. The inductor DCR has a positive temperature coefficient, which is about +0.385%/°C. Since the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

In order to obtain the correct current information, there should be a way to correct the temperature impact on the current sense component. The ISL6336D provides two methods: integrated temperature compensation and external temperature compensation.

Integrated Temperature Compensation

When the TCOMP voltage is equal or greater than VCC/15, ISL6336D will utilize the voltage at TM and TCOMP pins to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 20.

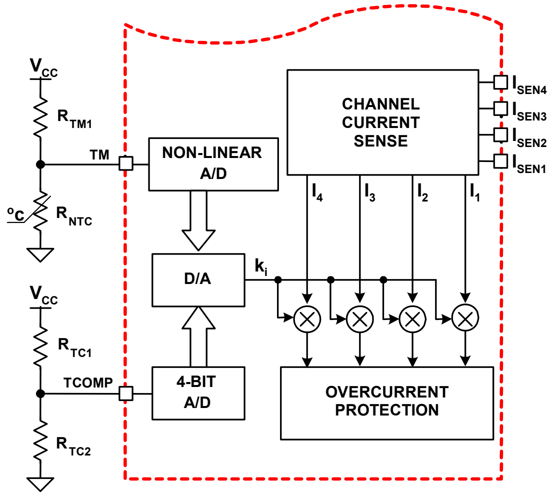


FIGURE 20. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

When the TM NTC is placed close to the current sense component (inductor), the temperature of the NTC will track the temperature of the current sense component. Therefore, the TM voltage can be utilized to obtain the temperature of the current sense component.

Based on VCC voltage, the ISL6336D converts the TM pin voltage to a 6-bit TM digital signal for temperature compensation. With the nonlinear A/D converter of ISL6336D, the TM digital signal is linearly proportional to the NTC temperature. For accurate temperature compensation, the ratio of the TM voltage to the NTC temperature of the practical design should be similar to that in Figure 18.

Depending on the location of the NTC and the airflow, the NTC may be cooler or hotter than the current sense component. The TCOMP pin voltage can be utilized to correct the temperature difference between NTC and the current sense component. When a different NTC type or different voltage divider is used for the TM function, the TCOMP voltage can also be used to compensate for the difference between the recommended TM voltage curve in Figure 19 and that of the actual design. According to the VCC voltage, ISL6336D converts the TCOMP pin voltage to a 4-bit TCOMP digital signal as TCOMP factor N.

The TCOMP factor N is an integer between 0 and 15. The integrated temperature compensation function is disabled for N = 0. For N = 4, the NTC temperature is equal to the temperature of the current sense component. For N < 4, the NTC is hotter than the current sense component. The NTC is cooler than the current sense component for N > 4. When N > 4, the larger TCOMP factor N is, the larger the difference between the NTC temperature and the temperature of the current sense component.

The ISL6336D multiplexes the TCOMP factor N with the TM digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated channel current signal is used for IMON and overcurrent protection functions.

Design Procedure

1. Properly choose the voltage divider for the TM pin to match the TM voltage vs temperature curve with the recommended curve in Figure 18.
2. Run the actual board under the full load and the desired cooling condition.
3. After the board reaches the thermal steady state, record the temperature (T_{CSC}) of the current sense component (inductor or MOSFET) and the voltage at TM and VCC pins.
4. Use Equation 20 to calculate the resistance of the TM NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet.

$$R_{NTC(T_{NTC})} = \frac{V_{TM} x R_{TM1}}{V_{CC} - V_{TM}} \qquad \text{(EQ. 20)}$$

5. Use Equation 21 to calculate the TCOMP factor N:

$$N = \frac{209x(T_{CSC} - T_{NTC})}{3xT_{NTC} + 400} + 4 \qquad \text{(EQ. 21)}$$

6. Choose an integral number close to the above result for the TCOMP factor. If this factor is higher than 15, use N = 15. If it is less than 1, use N = 1.
7. Choose the pull-up resistor R_{TC1} (typical 10kΩ);
8. If N = 15, one does not need the pull-down resistor R_{TC2}. If otherwise, obtain R_{TC2} using Equation 22:

$$R_{TC2} = \frac{N x R_{TC1}}{15 - N} \qquad \text{(EQ. 22)}$$

9. Run the actual board under full load again with the proper resistors connected to the TCOMP pin.
10. Record the output voltage as V1 immediately after the output voltage is stable with the full load. Record the output voltage as V2 after the VR reaches the thermal steady state.
11. If the output voltage increases over 2mV as the temperature increases (i.e., V2 - V1 > 2mV), reduce N and redesign R_{TC2}; if the output voltage decreases over 2mV as the temperature increases (i.e., V1 - V2 > 2mV), increase N and redesign R_{TC2}.

External Temperature Compensation

By pulling the TCOMP pin to GND, the integrated temperature compensation function is disabled. In addition, external temperature compensation network on the IMON pin, shown in Figure 21, can be used to cancel the temperature impact on the IMON voltage.

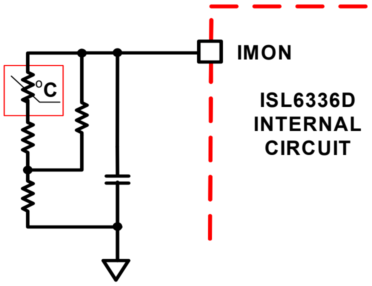


FIGURE 21. EXTERNAL TEMPERATURE COMPENSATION

The sensed current will flow out of the IMON pin and develop a voltage across the resistor equivalent (RIMON). If the resistance on the IMON pin reduces as the temperature increases, the temperature impact on the IMON voltage can be compensated. An NTC resistor can be placed close to the power stage and used to form a RIMON. Due to the nonlinear temperature characteristics of the NTC, a resistor network is needed to make the equivalent resistance on the IMON pin reverse proportional to the temperature.

The external temperature compensation network can only compensate the temperature impact on the IMON voltage, while it has no impact to the sensed current inside ISL6336D. Therefore, this network cannot compensate for the temperature impact on the overcurrent protection function.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 23, I_M is the maximum continuous output current; I_{P-P} is the peak-to-peak inductor current (see Equation 1); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2(1-d) + \frac{I_{L(P-P)}^{\;2}(1-d)}{12}\right] \quad \text{(EQ. 23)}$$

An additional term can be added to the lower MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_{SW}; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_{sw}\left[\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)t_{d2}\right] \quad \text{(EQ. 24)}$$

Thus the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper MOSFET switching times; the lower MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 25, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)\left(\frac{t_1}{2}\right)f_{SW} \quad \text{(EQ. 25)}$$

At turn-on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 26, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)\left(\frac{t_2}{2}\right)f_{SW} \quad \text{(EQ. 26)}$$

A third component involves the lower MOSFET's reverse recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated as a result is $P_{UP,3}$ and is approximated in Equation 27:

$$P_{UP,3} = V_{IN} Q_{rr} f_{SW} \quad \text{(EQ. 27)}$$

Finally, the resistive part of the upper MOSFET's is given in Equation 28 as $P_{UP,4}$.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 25, 26, and 27. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies, as shown in Equation 28.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 d + \frac{I_{P-P}^{\;2}}{12}d\right] \quad \text{(EQ. 28)}$$

Current Sensing Resistor

The resistors connected to the ISEN+ pins determine the gain in the channel-current balance loop and set the overcurrent trip point. Select values for these resistors by using Equation 29:

$$R_{ISEN} = \frac{R_X}{105 \times 10^{-6}}\,\frac{I_{OCP}}{N} \quad \text{(EQ. 29)}$$

where R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method, and I_{OCP} is the desired overcurrent trip point. Typically, I_{OCP} can be chosen to be 1.2x the maximum load current of the specific application.

With integrated temperature compensation, the sensed current signal is independent on the operational temperature of the power stage, i.e., the temperature effect on the current sense element R_X is cancelled by the integrated temperature compensation function. R_X in Equation 29 should be the resistance of the current sense element at the room temperature.

When the integrated temperature compensation function is disabled by pulling the TCOMP pin to GND, the sensed current will be dependent on the operational temperature of the power stage, since the DC resistance of the current sense element may be changed according to the operational temperature. R_X in Equation 29 should be the maximum DC resistance of the current sense element at the all operational temperature.

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistors. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see "Voltage Regulation" on page 16). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase, as shown in Equation 30:

$$R_{ISEN,2} = R_{ISEN}\frac{\Delta T_2}{\Delta T_1} \qquad \text{(EQ. 30)}$$

In Equation 30, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 30 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Compensation

The ISL6336D converter can be accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A type III controller, as shown in Figure 22, provides the necessary compensation.

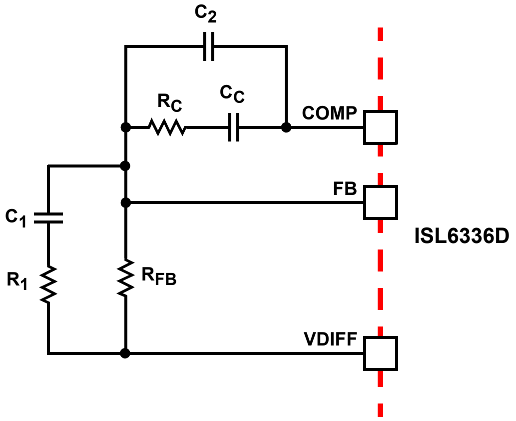


FIGURE 22. COMPENSATION CIRCUIT

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

$$\begin{aligned}
R_1 &= R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR} \\
C_1 &= \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}} \\
C_2 &= \frac{V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P\text{-}P}} \\
R_C &= \frac{V_{PP} \cdot (2\pi)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)} \\
C_C &= \frac{V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{P\text{-}P}}
\end{aligned} \qquad \text{(EQ. 31)}$$

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 31, R_{FB} can be arbitrarily chosen as 1kΩ to 2kΩ. The remaining compensation components are then selected.

In Equation 31, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and $V_{P\text{-}P}$ is the peak-to-peak sawtooth signal amplitude, typically 1.5V.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 32:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \qquad \text{(EQ. 32)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 13 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}$ (ESR). Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance, as shown in Equation 33.

$$L \geq (ESR)\frac{\left(V_{IN} - NV_{OUT}\right)V_{OUT}}{f_{SW}V_{IN}V_{P\text{-}P(MAX)}} \qquad \text{(EQ. 33)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 34 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 35 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2NCV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \qquad \text{(EQ. 34)}$$

$$L \leq \frac{(1.25)NC}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right]\left(V_{IN} - V_O\right) \qquad \text{(EQ. 35)}$$

Switching Frequency Selection

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 25, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in "Output Filter Design" on page 27. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs, which is related to duty cycle and the number of active phases.

For a 2-phase design, use Figure 23 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L(P-P)}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage.

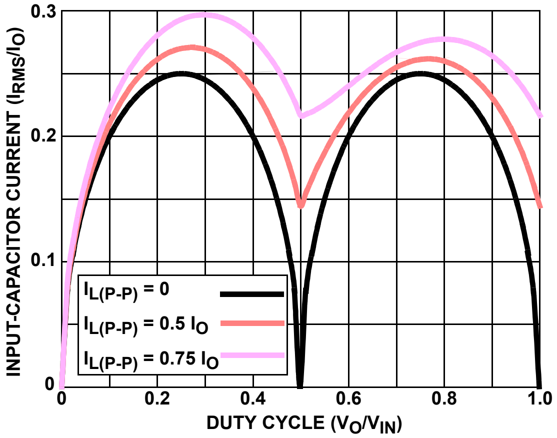


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

Figures 24 and 25 provide the same input RMS current information for 3- and 4-phase designs respectively. Use the same approach to selecting the bulk capacitor type and number, as previously described.

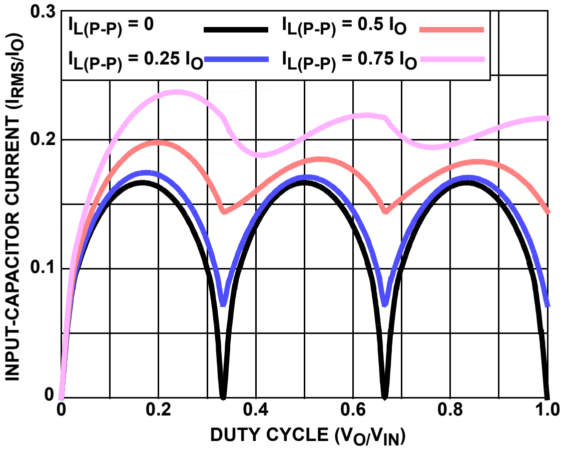


FIGURE 24. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

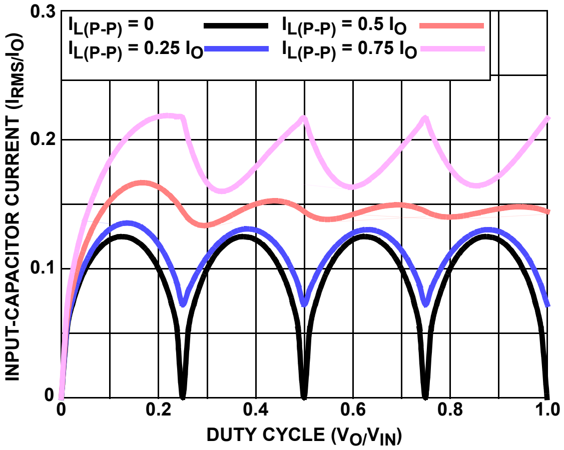


FIGURE 25. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize suppression.

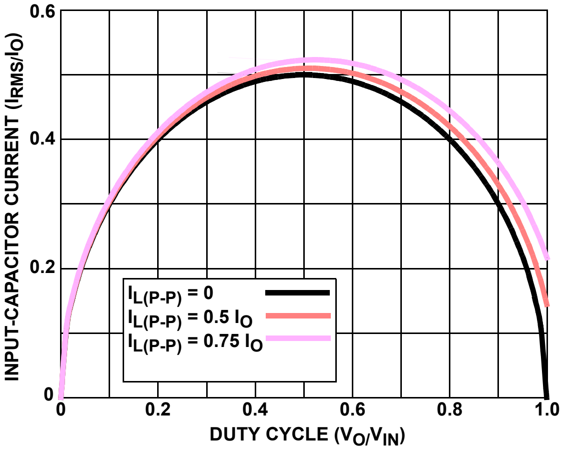


FIGURE 26. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

MULTIPHASE RMS IMPROVEMENT

Figure 26 is provided as a reference to demonstrate the dramatic reductions in input-capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, a maximum sustained output current of 40A, and a ratio of $I_{L(P-P)}$ to I_O of 0.5. The single phase converter would require $17.3A_{RMS}$ current capacity while the two-phase converter would only require $10.9A_{RMS}$. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout Considerations

The following layout strategies are intended to minimize the impact of board parasitic impedances on converter performance and to optimize the heat-dissipating capabilities of the printed-circuit board. These sections highlight some important practices which should not be overlooked during the layout process.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position one high frequency ceramic input capacitor next to each upper MOSFET drain. Place the bulk input capacitors as close to the upper MOSFET drains, as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity to the microprocessor socket.

Voltage-Regulator (VR) Design Materials

Intersil has also developed a set of worksheets to support VR design and layout. Contact Intersil's local office or field support for the latest available information.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 6, 2014	FN8320.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

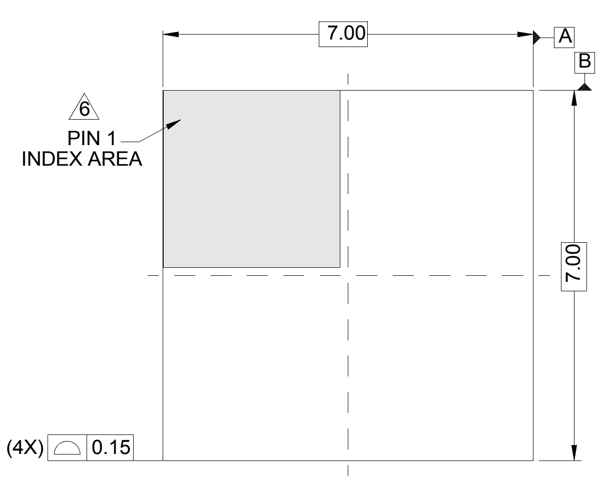
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

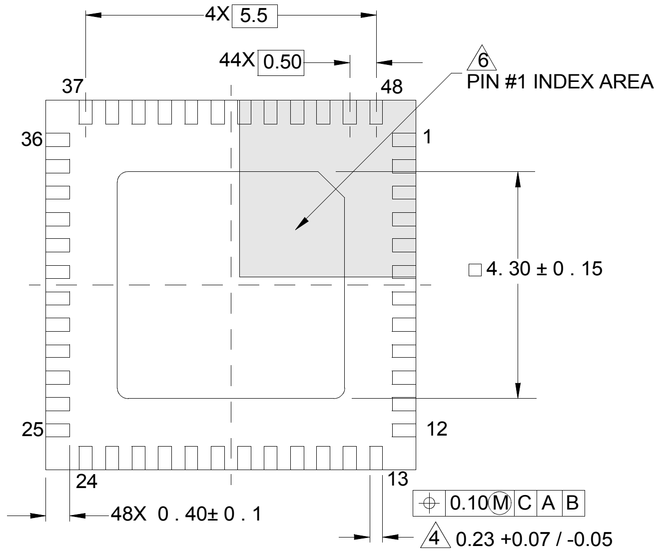
L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

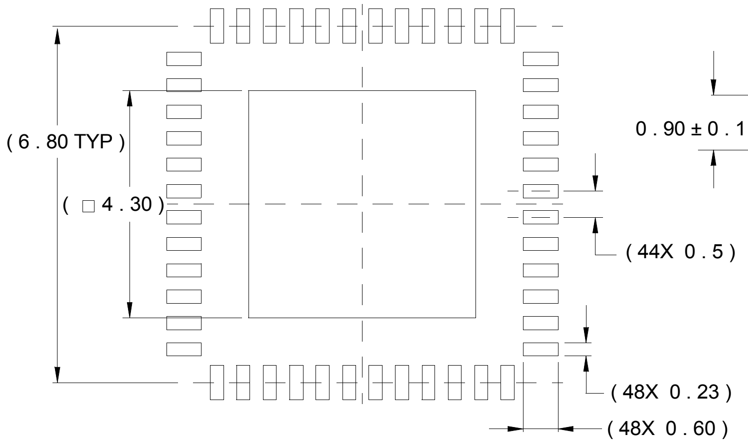
Rev 5, 4/10



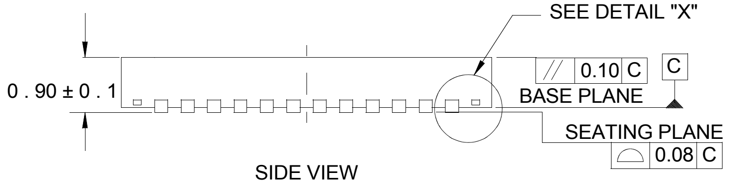
TOP VIEW



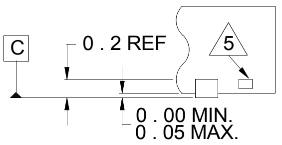
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.