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Flash Memory Datasheet

MONOS eFlash

Overview

This Renesas MONOS_eFlash Technology is realized with TSMC standard CMOS process Technology as N40LP by Open Platform. The IP has the following features – large memory capacity , high performance , high reliability. Therefore it will expand to not only MCU also many applications of SoC field.

Key Features

Code flash memory

- Supports versions with up to 4 Mbytes of ROM
- High Speed Read Operation 50MHz(120MHz option)
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)

Data flash memory

- 64 Kbytes, reprogrammable up to 250,000 times
- Programming/erasing as background operations (BGOs)

SG-MONOS Flash Specification

	Code Flash	**Data Flash**
VCC	**1.62V-3.6V@READ 2.25V-3.6V@P/E (1.62V~ option)**	**1.62V-3.6V@READ 2.25V-3.6V@P/E (1.62V~ option)**
VDD	**1.1V±10%**	**1.1V±10%**
Max capacity	**4MB**	**64KB**
Read speed	**50MHz (120MHz option)**	**10MHz**
Read Bus	**X64/ x128**	**x32**
Block size	**32/16KByte**	**64Byte**
Endurance	**10K**	**125K 250K(@3years)**
Retention	**10years@125'C**	**10 years@125'C**
Tj	**-40'C~125'C**	**-40'C~125'C**

**This IP is contract design IP. Please contact for detail.*

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