

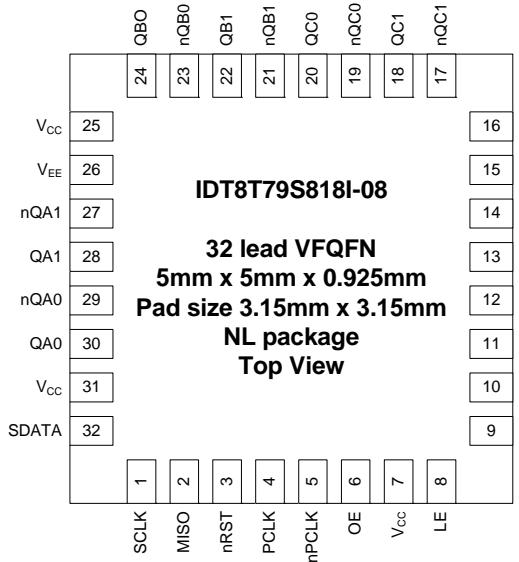
## General Description

The IDT8T79S818I-08 is a high performance, 1-to-8, differential input to universal output clock divider and fanout buffer. The device is designed for frequency-division and signal fanout of high-frequency clock signals in applications requiring four different output frequencies generated simultaneously. Each bank of two outputs has a selectable divider value of  $\div 1$  through  $\div 6$  and  $\div 8$ . The IDT8T79S818I-08 is optimized for 3.3V and 2.5V supply voltages and a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The device is packaged in a space-saving 32 lead VFQFN package.

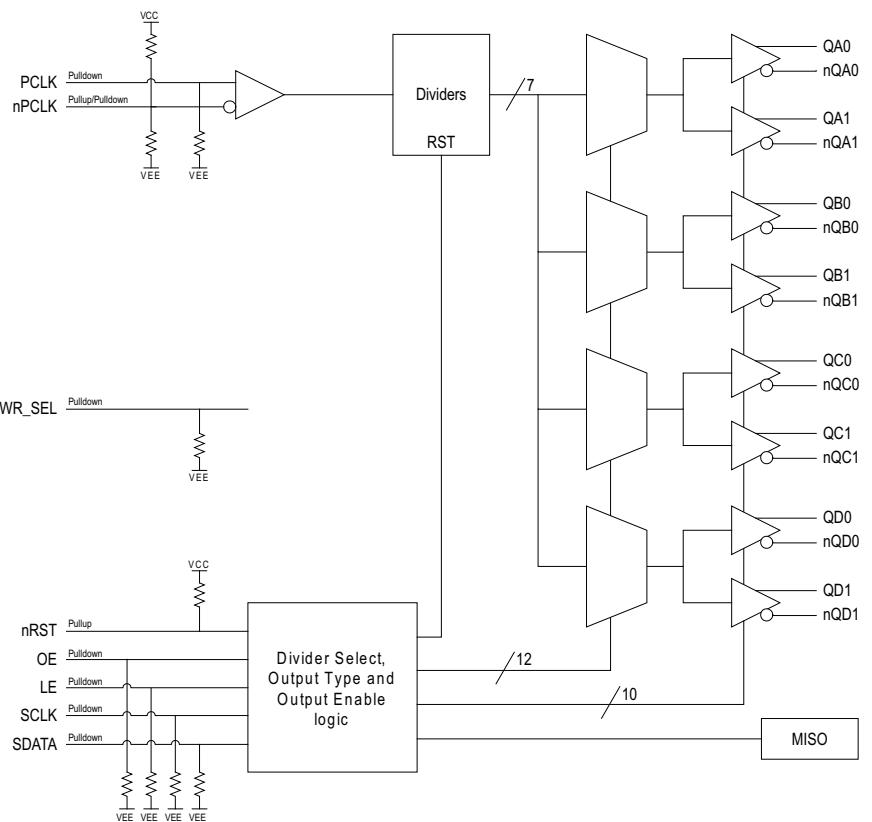
## Features

- Four banks of two low skew outputs
- Selectable bank output divider values:  $\div 1$  through  $\div 6$  and  $\div 8$
- One differential PCLK, nPCLK input
- PCLK, nPCLK input pair can accept the following differential input levels: LVPECL, LVDS levels
- Maximum input frequency: 1.5GHz
- LVCMOS control inputs
- $\text{QXX} \div 1$  edge aligned to  $\text{QXX} \div n$  edge
- Individual output divider control via serial interface
- Individual output enable/disable control via serial interface
- Individual output type control, LVDS or LVPECL, via serial interface
- 2.375V to 3.465V supply voltage operation
- $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  ambient operating temperature
- Lead-free (RoHS 6) packaging

## Pin Assignment



## Block Diagram



## Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	SCLK	Input	Pulldown	Serial Control Port Mode Data Input. LVCMOS/LVTTL interface levels.
2	MISO	Output		Serial Control Port Mode Data Output. LVCMOS/LVTTL interface levels.
3	nRST	Input	Pullup	Frequency Divider Reset. When the nRST is released (rising edge), the divided clock outputs are activated and will transition to a high state simultaneously. See also Timing Diagram. LVCMOS/LVTTL interface levels ( <a href="#">"Figure 1. Timing Diagram"</a> ).
4	PCLK	Input	Pulldown	Non-inverting differential clock input.
5	nPCLK	Input	Pullup / Pulldown	Inverting differential clock input. $V_{CC} / 2$ by default when left floating.
6	OE	Input	Pulldown	Default output disable. LVCMOS/LVTTL interface levels. See <a href="#">"Table 3B. OE Truth Table"</a> .
7, 10, 16, 25, 31	$V_{CC}$	Power		Power supply voltage pin.
8	LE	Input	Pulldown	Serial Control Port Mode Load Enable. Latches data when the pin gets a high level. Outputs are disabled when LE is low. LVCMOS/LVTTL interface levels.
9	PWR_SEL		Pulldown	Power supply selection. See <a href="#">"Table 3A. PWR_SEL Truth Table"</a> .
11, 12	nQD1, QD1	Output		Differential output pair Bank D, output 1. LVPECL or LVDS interface levels.
13, 14	nQD0, QD0	Output		Differential output pair Bank D, output 0. LVPECL or LVDS interface levels.
15, 26	$V_{EE}$	Power		Negative power supply pins.
17, 18	nQC1, QC1	Output		Differential output pair Bank C, output 1. LVPECL or LVDS interface levels.
19, 20	nQC0, QC0	Output		Differential output pair Bank C, output 0. LVPECL or LVDS interface levels.
21, 22	nQB1, QB1	Output		Differential output pair Bank B, output 1. LVPECL or LVDS interface levels.
23, 24	nQB0, QB0	Output		Differential output pair Bank B, output 0. LVPECL or LVDS interface levels.
27, 28	nQA1, QA1	Output		Differential output pair Bank A, output 1. LVPECL or LVDS interface levels.
29, 30	nQA0, QA0	Output		Differential output pair Bank A, output 0. LVPECL or LVDS interface levels.
32	SDATA	Input	Pulldown	Serial Control Port Mode Data Input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See ["Table 2. Pin Characteristics"](#) for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance				2		pF
$R_{PULLUP}$	Input Pullup Resistor				51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor				51		k $\Omega$
$R_{OUT}$	Output Impedance	MISO	$V_{CC} = 3.3V$		125		$\Omega$
			$V_{CC} = 2.5V$		145		$\Omega$

## Function Tables

**Table 3A. PWR\_SEL Truth Table**

PWR_SEL	Function
L (Connect to V <sub>EE</sub> )	2.5V power supply
H (Connect to V <sub>CC</sub> )	3.3V power supply

**Table 3B. OE Truth Table**

OE	Function
L (default)	All outputs disabled (Low/High static mode), regardless of individual OE registers set by Serial Interface.
H	Outputs enabled according to individual OE registers set by Serial Interface (see " <a href="#">Table 3E. Configuration Table</a> ").

## Output Type Control and Start-up Status

Two output types are available: LVDS and LVPECL. The part features four modes of output type controls, see Table 3C.

Disabled outputs are in static Low/High LVDS mode. At start-up, all outputs are disabled (i.e. in static Low/High LVDS mode) until the part has been configured. A global hardware Output Enable (OE pin #6) enables or disables all outputs at once. The global hardware OE has priority over serial interface configuration.

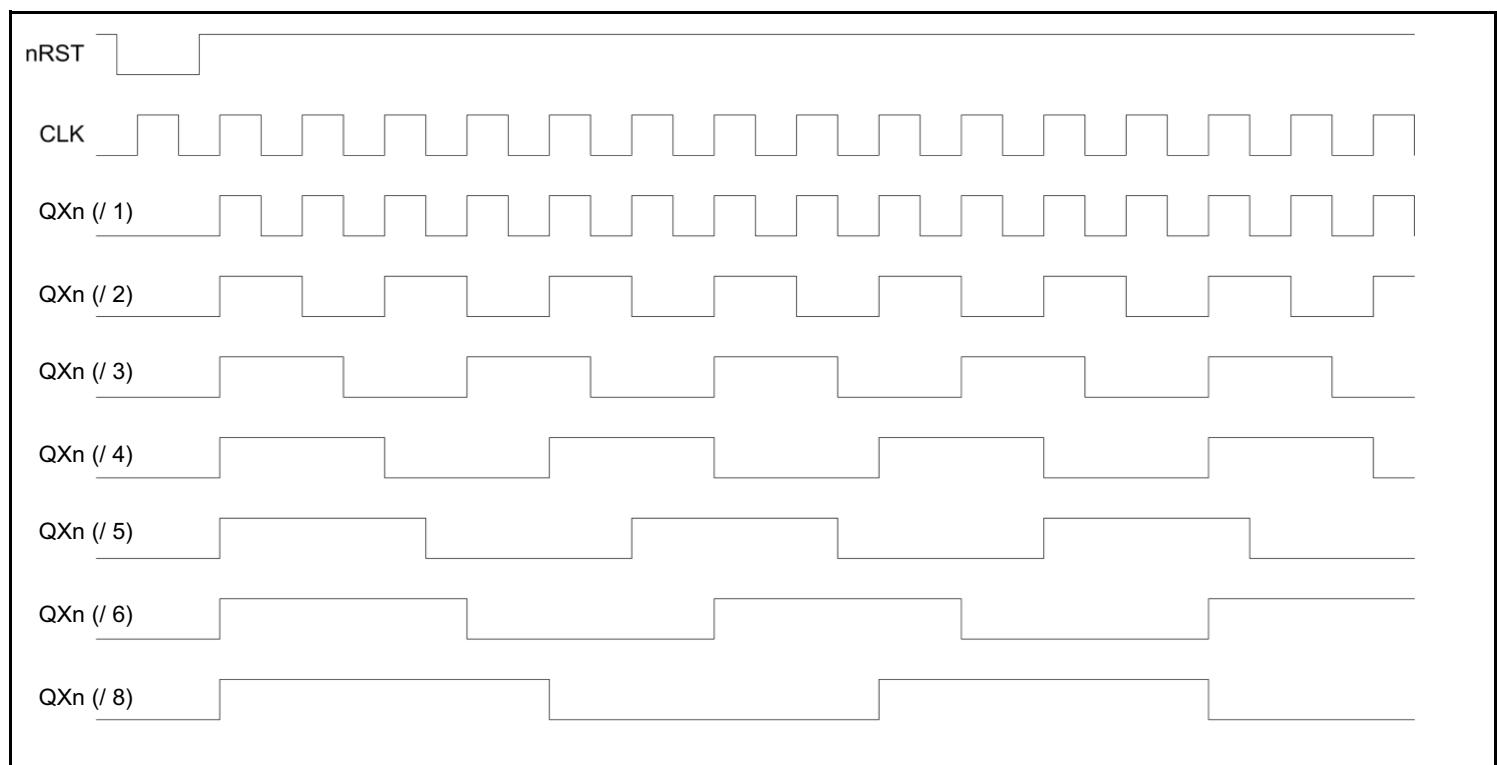
**Table 3C. Output Type Control**

Control Bits		Output Configuration
D2	D1	
LOW	LOW	8 LVDS outputs
HIGH	HIGH	8 LVPECL outputs
HIGH	LOW	2 LVDS (QA <sub>x</sub> ) + 6 LVPECL (QB <sub>x</sub> , QC <sub>x</sub> , QD <sub>x</sub> ) outputs
LOW	HIGH	2 LVPECL (QA <sub>x</sub> ) + 6 LVDS (QB <sub>x</sub> , QC <sub>x</sub> , QD <sub>x</sub> ) outputs

## Frequency Divider

Each output bank can be individually set to output an integer division of the input frequency. Factors of 1, 2, 3, 4, 5, 6 and 8 are available and are programmed by a serial interface.

The nRST pin resets the dividers. When the nRST pin is released, all output dividers are activated and will transition to a high state simultaneously.

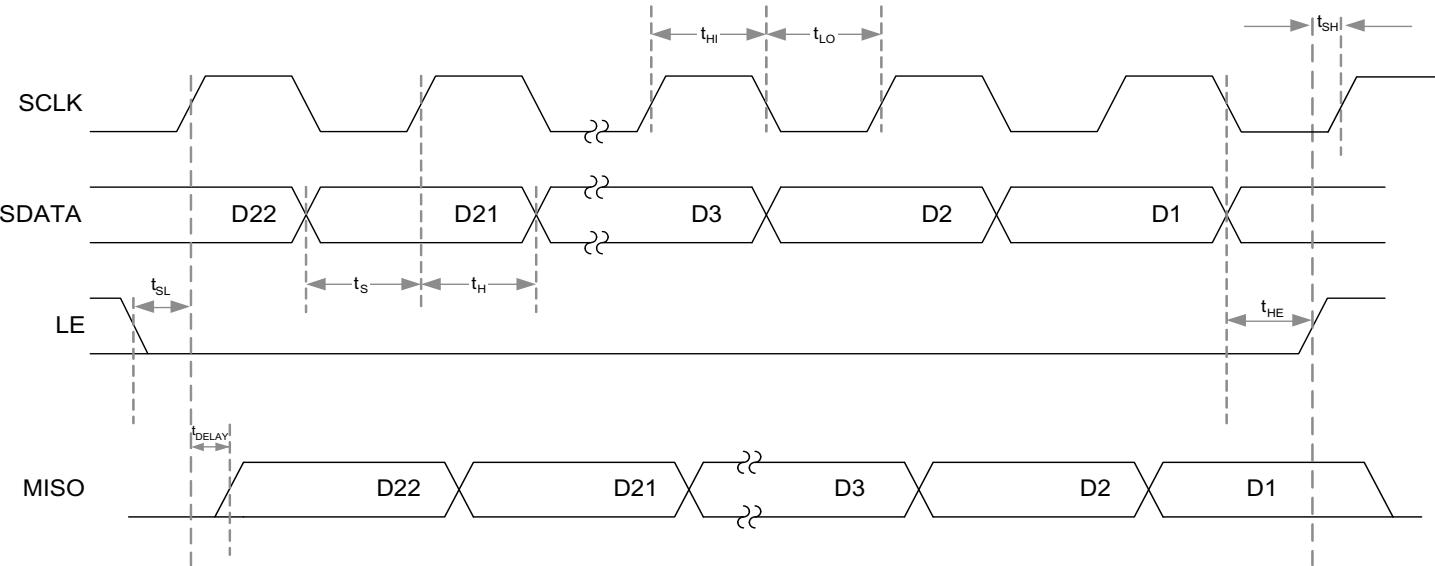


**Figure 1. Timing Diagram**

## Serial Interface

Configuration of the IDT8T79S818I-08 is achieved by writing 22 configuration bits over serial interface. All 22 bits have to be written in sequence.

After writing the 22 configuration bits, the LE pin must remain at high level for outputs to toggle.



**Figure 2. Serial Interface Timing Diagram for Write and Read Access**

**Table 3D. Timing AC Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$t_S$	Data to Clock Setup Time		10			ns
$t_H$	Data to Clock Hold Time		10			ns
$t_{HE}$	Clock to LE Hold Time		10			ns
$t_{HI}$	Clock High Duration		25			ns
$t_{LO}$	Clock Low Duration		25			ns
$t_{SL}$	LE to Clock Setup Time		10			ns
$t_{SH}$	LE to SCLK Setup Time		10			ns
$t_{DELAY}$	Clock to MISO Delay Time				10	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpmin. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 3E. Configuration Table**

Bit	Name	Function	Truth Table
D22	sd0	Output Bank D, Divider Factor Setting bit 0	See "Table 3F. Divider Setting Truth Table"
D21	sd1	Output Bank D, Divider Factor Setting bit 1	
D20	sd2	Output Bank D, Divider Factor Setting bit 2	
D19	sc0	Output Bank C, Divider Factor Setting bit 0	
D18	sc1	Output Bank C, Divider Factor Setting bit 1	
D17	sc2	Output Bank C, Divider Factor Setting bit 2	
D16	sb0	Output Bank B, Divider Factor Setting bit 0	
D15	sb1	Output Bank B, Divider Factor Setting bit 1	
D14	sb2	Output Bank B, Divider Factor Setting bit 2	
D13	sa0	Output Bank A, Divider Factor Setting bit 0	
D12	sa1	Output Bank A, Divider Factor Setting bit 1	
D11	sa2	Output Bank A, Divider Factor Setting bit 2	
D10	oed1	Output Enable QD1	Low: Disabled High: Enabled
D9	oedo	Output Enable QD0	
D8	oec1	Output Enable QC1	
D7	oec0	Output Enable QC0	
D6	oeb1	Output Enable QB1	
D5	oeb0	Output Enable QB0	
D4	oea1	Output Enable QA1	
D3	oea0	Output Enable QA0	
D2	ot1	Banks QB, QC, QD Output Type	Low: LVDS High: LVPECL
D1	ot0	Bank QA Output Type	

**Table 3F. Divider Setting Truth Table**

sd2	sd1	sd0	sc2	sc1	sc0	sb2	sb1	sb0	sa2	sa1	sa0	Divide Ratio
L	L	L										1
L	L	H										2
L	H	L										3
L	H	H										4
H	L	L										5
H	L	H										6
H	H	L										Reserved
H	H	H										8

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$ (LVCMOS)	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	48.9°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics**,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current	LVPECL		147	175	mA
$I_{CC}$	Power Supply Current	LVDS		237	284	mA

**Table 4B. Power Supply DC Characteristics**,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current	LVPECL		130	165	mA
$I_{CC}$	Power Supply Current	LVDS		230	272	mA

**Table 4C. LVC MOS/LV TTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$		2.2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$		1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$		-0.3		0.8	V
		$V_{CC} = 2.5V$		-0.3		0.7	V
$I_{IH}$	Input High Current	nRST	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			10	$\mu A$
		OE, LE, PWR_SEL, SCLK, SDATA	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	nRST	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-150		$\mu A$
		OE, LE, PWR_SEL, SCLK, SDATA	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-10		$\mu A$
$V_{OH}$	Output High Voltage	MISO	$V_{CC} = 3.465V$ $I_{OH} = -1mA$		2.6		V
			$V_{CC} = 2.625V$ $I_{OH} = -1mA$		1.8		V
$V_{OL}$	Output Low Voltage	MISO	$V_{CC} = 3.465V$ or $2.625V$ $I_{OL} = 1mA$			0.5	V

**Table 4D. Differential Input DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK, nPCLK	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-10		$\mu A$
		nPCLK	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-150		$\mu A$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1				0.15		1.3
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2				$V_{EE} + 1$	$V_{CC} - 0.5$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as crosspoint.

**Table 4E. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow**

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1			$V_{CC} - 1.3$		$V_{CC} - 0.75$	V
$V_{OL}$	Output Low Voltage; NOTE 1			$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 4F. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.3$		$V_{CC} - 0.75$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

**Table 4G. LVDS DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{os}$	Offset Voltage		1.125		1.45	V
$\Delta V_{os}$	$V_{os}$ Magnitude Change				50	mV

**Table 4H. LVDS DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247		454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{os}$	Offset Voltage		1.125		1.45	V
$\Delta V_{os}$	$V_{os}$ Magnitude Change				50	mV

## AC Electrical Characteristics

Table 5. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  with airflow

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	PCLK, nPCLK				1.5	GHz
$f_{OUT}$	Output Frequency	$f_{IN} = 1500MHz$ , $Qx = \div 1$		1500			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 2$		750			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 3$		500			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 4$		375			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 5$		300			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 6$		250			MHz
		$f_{IN} = 1500MHz$ , $Qx = \div 8$		187.5			MHz
$t_{PD}$	Propagation Delay; NOTE 5	All outputs operating at the same frequency		0.57	0.8	1	ns
$tsk(o)$	Output Skew; NOTE 1, 2	All outputs operating at the same frequency				80	ps
$tsk(b)$	Bank Skew; NOTE 1, 3	Outputs within each bank operating at the same frequency				55	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 1, 4					450	ps
$t_R / t_F$	Output Rise/Fall Time	LVPECL	20% to 80%	50		300	ps
		LVDS	20% to 80%	50		300	ps
$odc$	Output Duty Cycle			40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

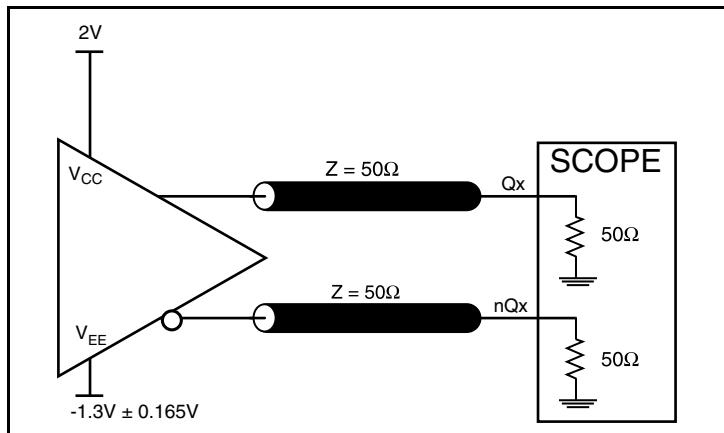
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 3: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

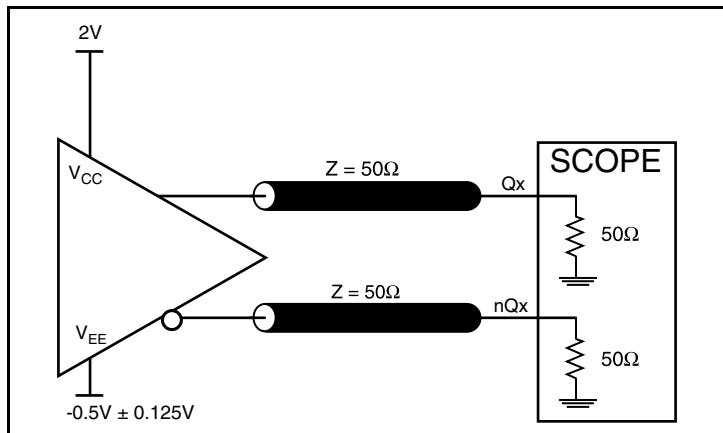
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Measured from the differential input crossing point to the differential output crossing point.

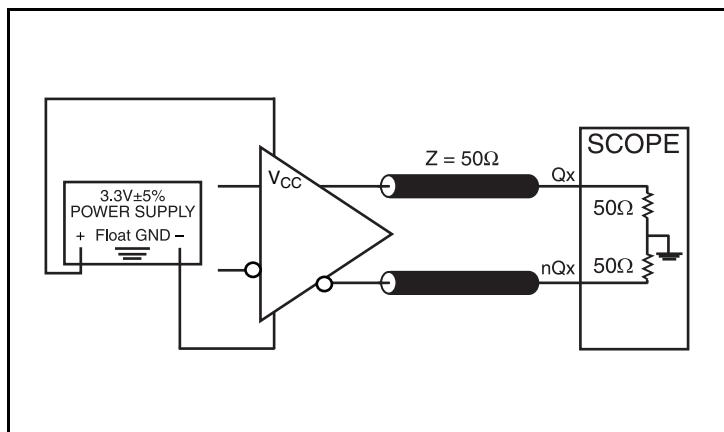
## Parameter Measurement Information



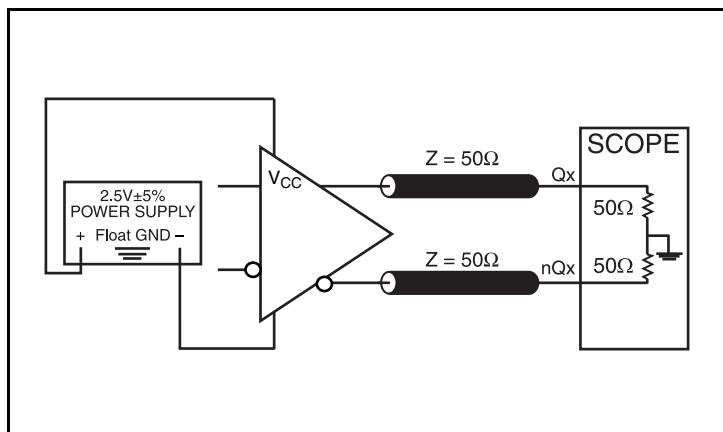
3.3V LVPECL Output Load Test Circuit



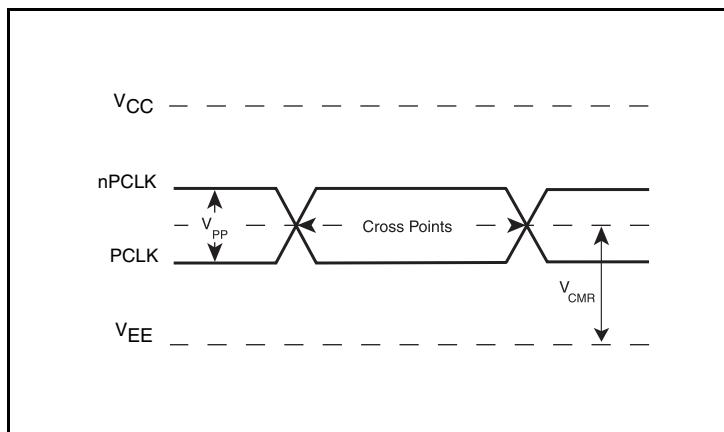
2.5V LVPECL Output Load Test Circuit



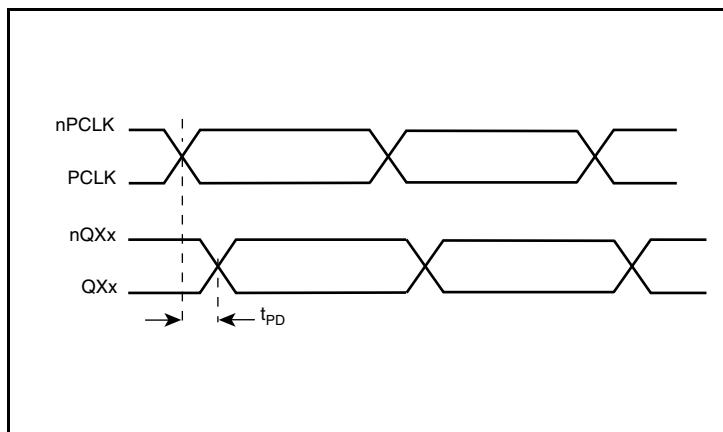
3.3V LVDS Output Load Test Circuit



2.5V LVDS Output Load Test Circuit

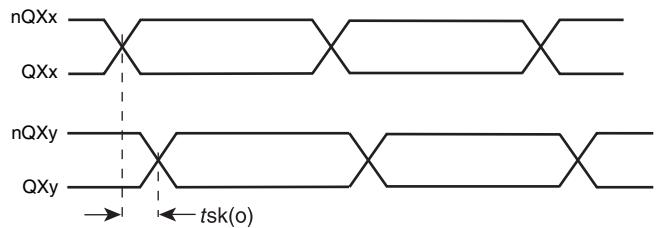


Differential Input Levels



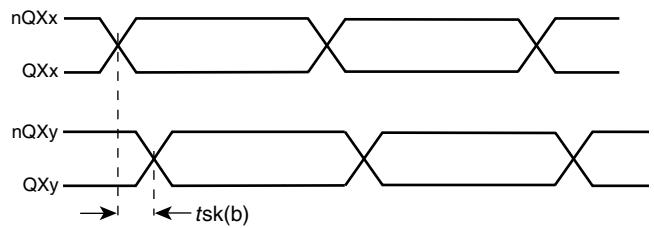
Propagation Delay

## Parameter Measurement Information, continued



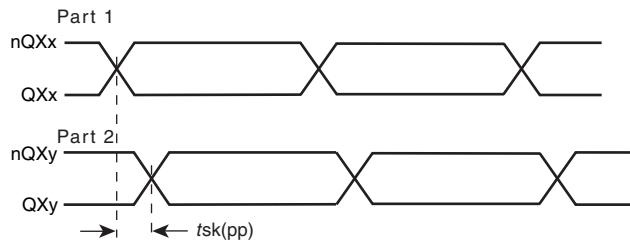
Where X = Bank A, B, C or D

**Output Skew**



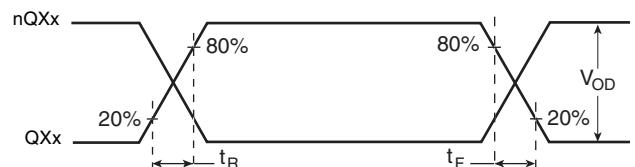
Where X = Bank A, B, C or D

**Bank Skew**



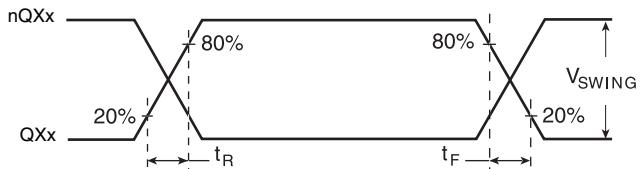
Where X = Bank A, B, C or D

**Part-to-Part Skew**



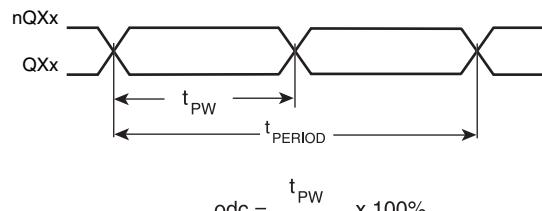
Where X = Bank A, B, C or D

**LVDS Output Rise/Fall Time**



Where X = Bank A, B, C or D

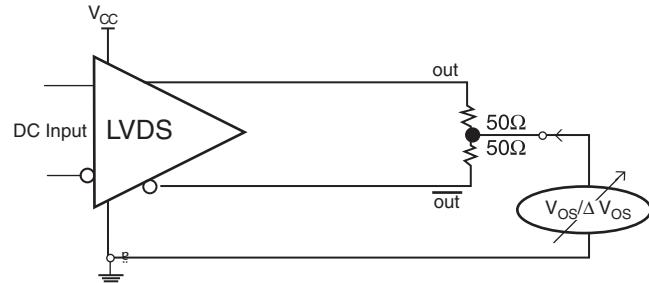
**LVPECL Output Rise/Fall Time**



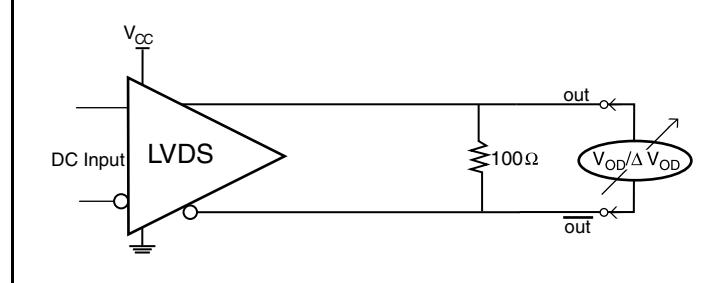
Where X = Bank A, B, C or D

**Output Duty Cycle/Pulse Width/Period**

## Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

##### LVC MOS Outputs

The unused LVC MOS output can be left floating. There should be no trace attached.

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line

impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

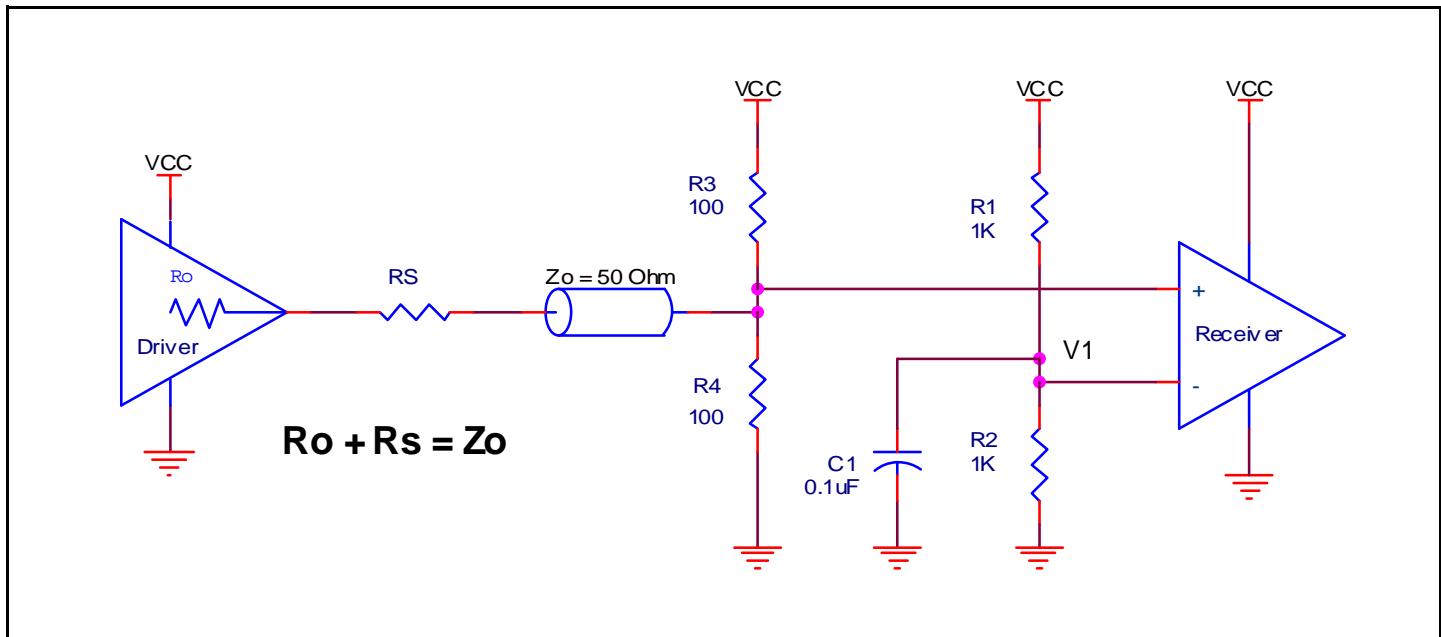
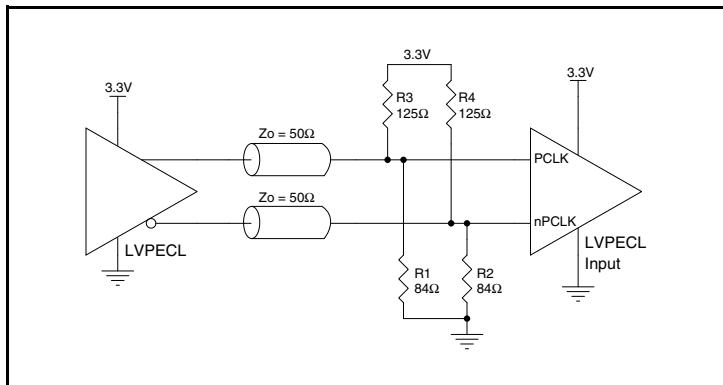


Figure 3. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

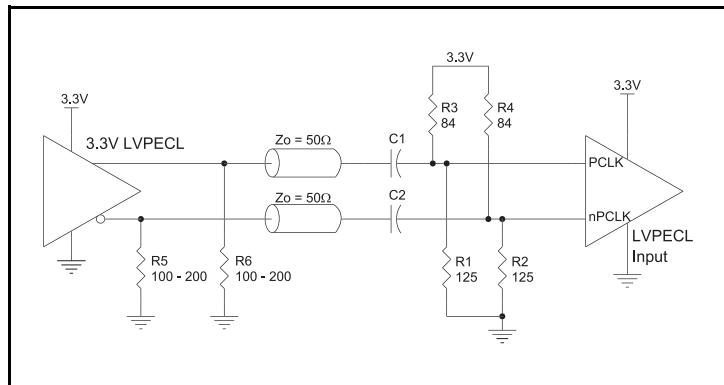
### 3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 4A to 4C show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

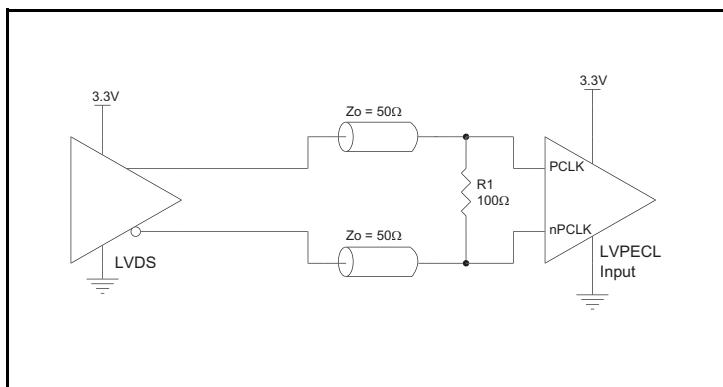
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 4A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 4B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

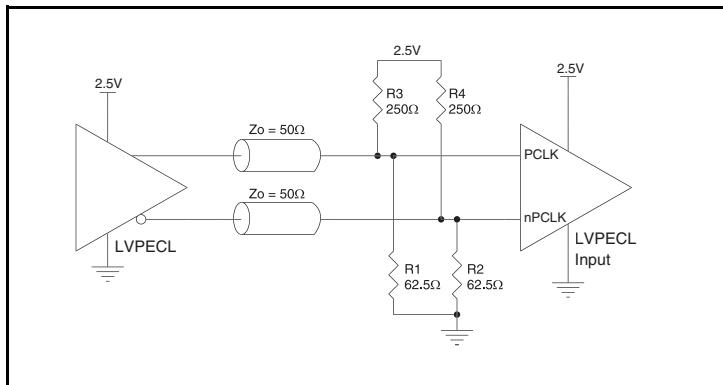


**Figure 4C. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

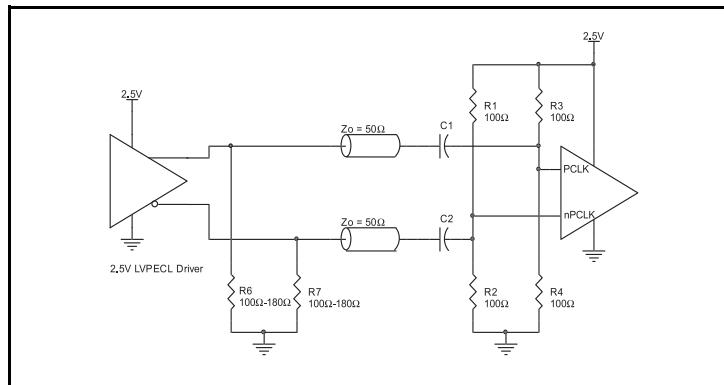
## 2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 5A to 5C show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

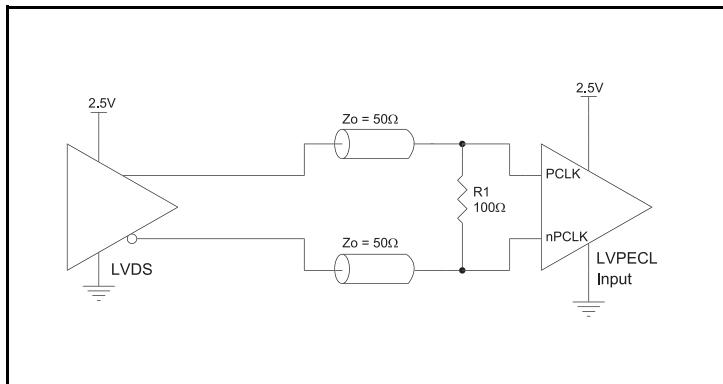
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 5A. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 5B. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple**

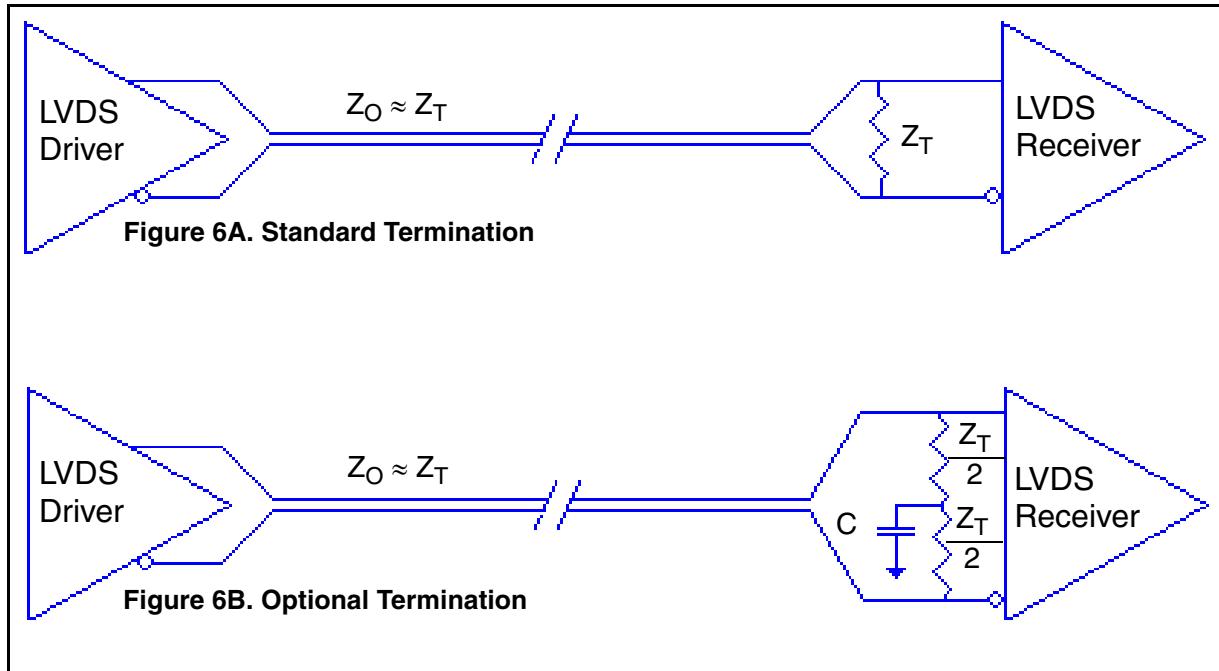


**Figure 5C. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver**

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



## LVDS Termination

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

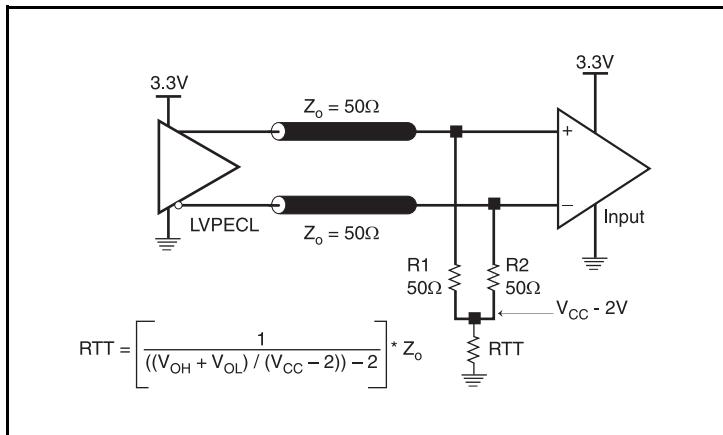


Figure 7A. 3.3V LVPECL Output Termination

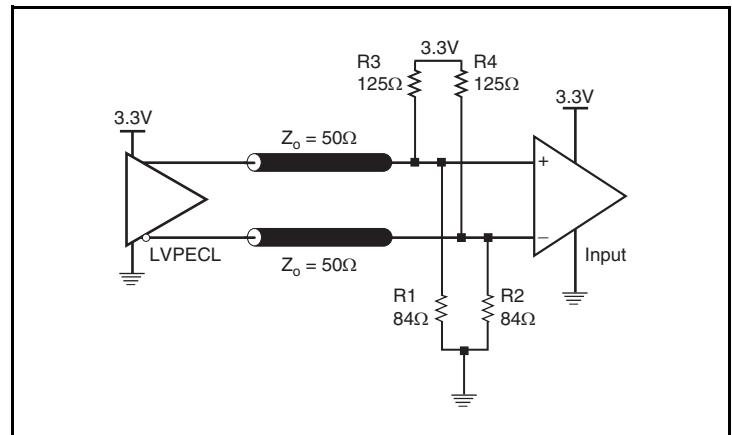


Figure 7B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 8A and Figure 8B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The  $R3$  in Figure 8B can be eliminated and the termination is shown in Figure 8C.

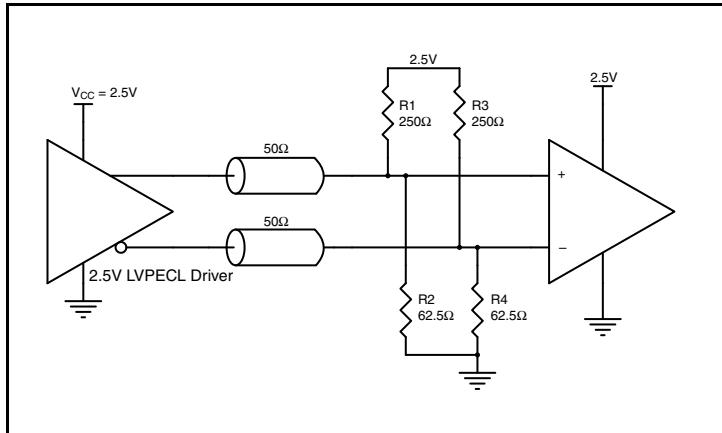


Figure 8A. 2.5V LVPECL Driver Termination Example

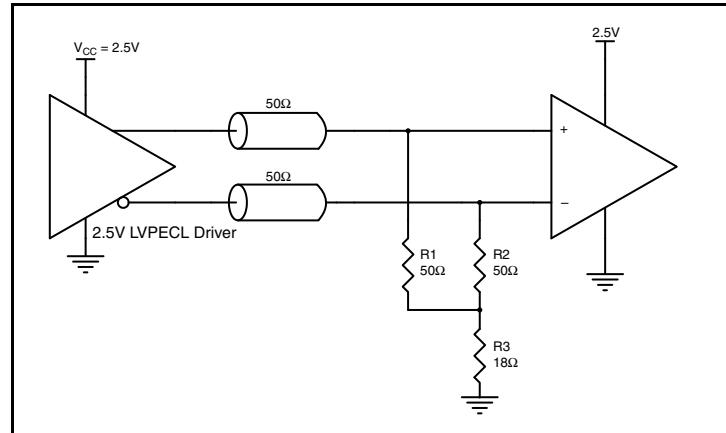


Figure 8B. 2.5V LVPECL Driver Termination Example

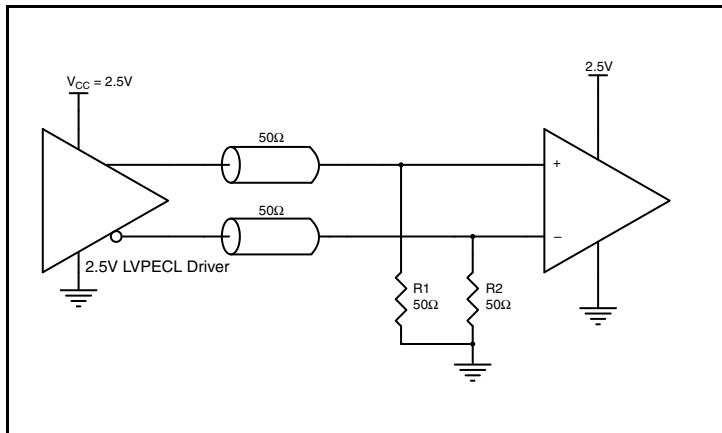


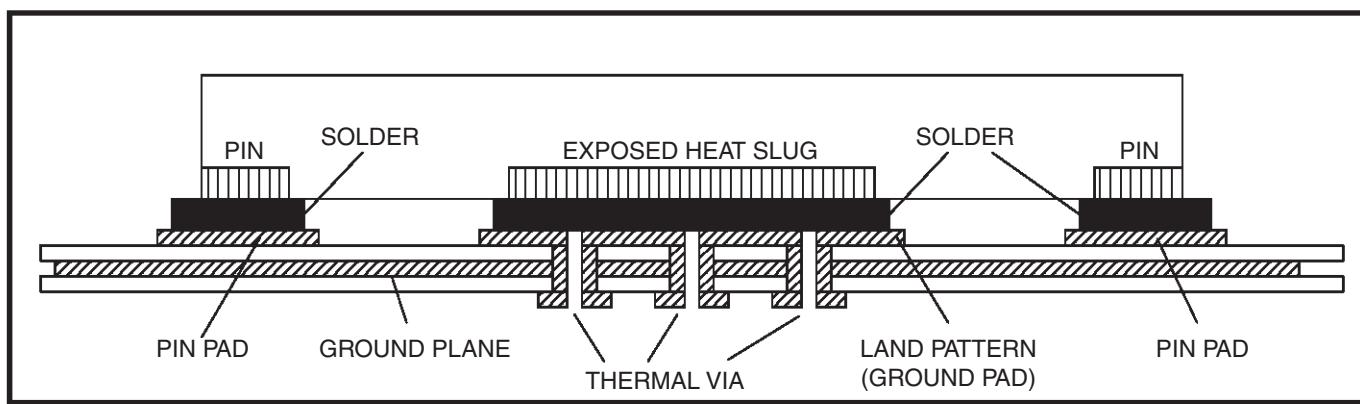
Figure 8C. 2.5V LVPECL Driver Termination Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 9*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 9. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

A forced airflow has to be guaranteed in order to meet the thermal requirements of the part at  $3.3V \pm 5\%$ . No flow is required at  $2.5V \pm 5\%$ .

**Table 6. Minimum recommended air flow conditions**

Power Supply Voltage ( $V_{CC}$ , Volts)			Minimum Airflow
Minimum	Typical	Maximum	Meters per Second
2.375	2.5	2.625	0
3.135	3.3	3.465	1

## LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T79S818I-08. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T79S818I-08 is the sum of the core power plus the power dissipated into the load. The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: The maximum  $I_{CC}$  current at  $85^\circ C$  is 269mA.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{CC\_MAX} = 3.465V * 269mA = 932.1mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ C$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ C$  ensures that the bond wire and bond pad temperature remains below  $125^\circ C$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming 1m/s air flow and a multi-layer board, the appropriate value is  $42^\circ C/W$  per Table 7A below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ C$  with all outputs switching is:

$$85^\circ C + 0.9321W * 42^\circ C/W = 124.2^\circ C. This is below the limit of 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7A. Thermal Resistance  $\theta_{JA}$  for 32-lead VFQFN Package**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42°C/W	39.4°C/W

## LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T79S818I-08, for all outputs that are configured to LVPECL. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8T79S818I-08 is the sum of the core power plus the power dissipated due to the load. The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{EE\_MAX} = 3.465V * 175mA = 606.4\text{mW}$
- Power (outputs)<sub>MAX</sub> = **31.6mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $8 * 31.6\text{mW} = 253\text{mW}$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $606.4\text{mW} + 253\text{mW} = 860\text{mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming one meter per second and a multi-layer board, the appropriate value is 42°C/W per Table 7B below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ\text{C} + 0.860\text{W} * 42^\circ\text{C/W} = 121.2^\circ\text{C}$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

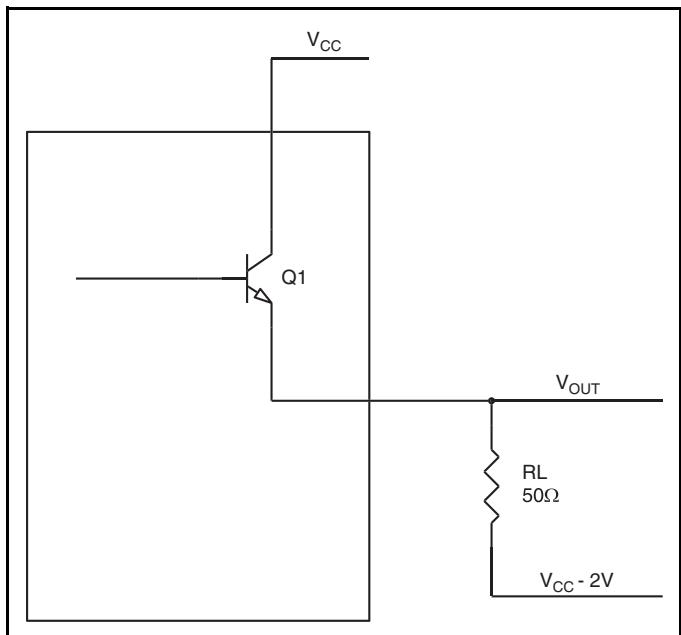
**Table 7B. Thermal Resistance  $\theta_{JA}$  for 32-lead VFQFN Package**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42°C/W	39.4°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 11*.



**Figure 11. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.75V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.75V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.6V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.6V$

$P_{d\_H}$  is power dissipation when the output drives high.

$P_{d\_L}$  is the power dissipation when the output drives low.

$$P_{d\_H} = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX})) / 50\Omega] * 0.75V = 18.8\text{mW}$$

$$P_{d\_L} = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX})) / 50\Omega] * 1.6V = 12.8\text{mW}$$

$$\text{Total Power Dissipation per output pair} = P_{d\_H} + P_{d\_L} = 31.6\text{mW}$$

## Reliability Information

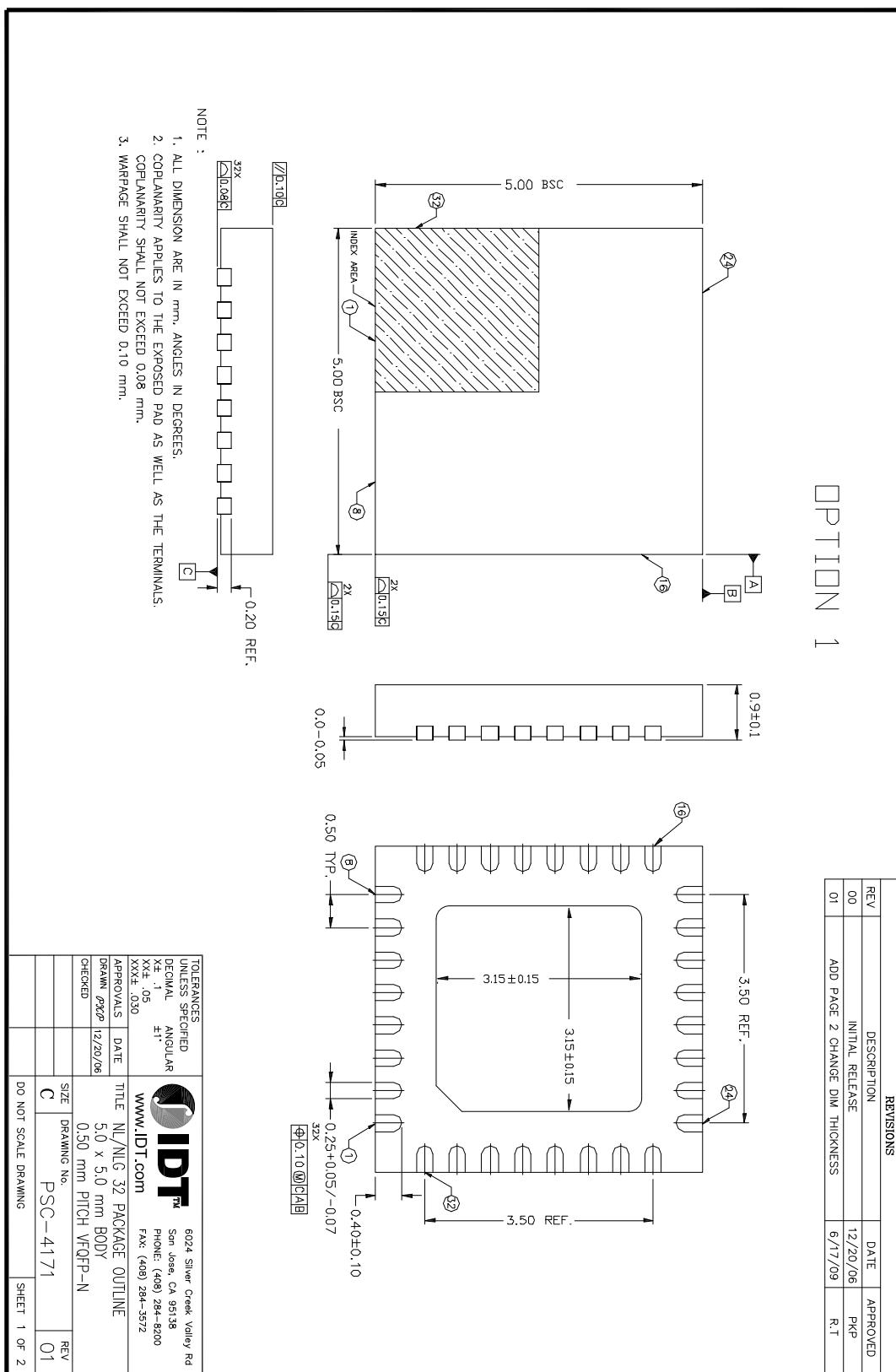
**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32-lead VFQFN Package**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42.0°C/W	39.4°C/W

## Transistor Count

The transistor count for IDT8T79S818I-08 is: 2618

## 32 Lead VFQFN Package Outline and Package Dimensions



## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T79S818A-08NLGI	IDT8T79S818A-08NLGI	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8T79S818A-08NLGI8	IDT8T79S818A-08NLGI	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1 15 16	Features Section - deleted CML levles from the PCLK bullet. 3.3V LVPECL Clock Input Interface Application Note - deleted CML references. 2.5V LVPECL Clock Input Interface Application Note - deleted CML references.	7/11/13



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).