EBU WAN PLL

IDT82V32021

Version 3
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Table of Contents

List of Tables

List of Figures

FEATURES

HIGHLIGHTS

- The first single PLL chip:
  - Features 1.2 Hz to 560 Hz bandwidth
  - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-16/ Option I) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including 4E and 4 clocks
- Employs DPLL and APLL to feature excellent jitter performance and minimize the number of the external components
- Supports Forced or Automatic operating mode switch controlled by an internal state machine; the primary operating modes are Free-Run, Locked and Holdover
- Supports programmable DPLL bandwidth (1.2 Hz to 560 Hz in 8 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports PBO to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Limits the phase and frequency offset of the output
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides two 2 kHz, 4 kHz or 8 kHz frame sync input signals, and an 8 kHz frame sync output signal
- Provides two input clocks whose frequency cover from 2 kHz to 155.52 MHz
- Provides one output clock whose frequency covers from 1Hz to 155.52 MHz
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports CMOS input/output
- Supports master clock calibration
- Supports Line Card application
- Meets Telcordia GR-1244-CORE, GR-253-CORE, ITU-T G.812, ITU-T G.813 and ITU-T G.783 criteria

OTHER FEATURES

- I^2C programming interface
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 68-pin VFQFPN package, Green package options available

APPLICATIONS

- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V32021 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for 4E and 4 clocks in SONET / SDH equipments, DWDM and Wireless base station, such as GSM, 3G, DSL concentrator, Router and Access Network applications.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

An input clock is automatically or manually selected for DPLL locking. The DPLL supports three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0 APLL, the outputs of the device will be in a better jitter/wander performance.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed only through an I^2C programming interface.

The device can be used typically in Line Card application.

FUNCTIONAL BLOCK DIAGRAM

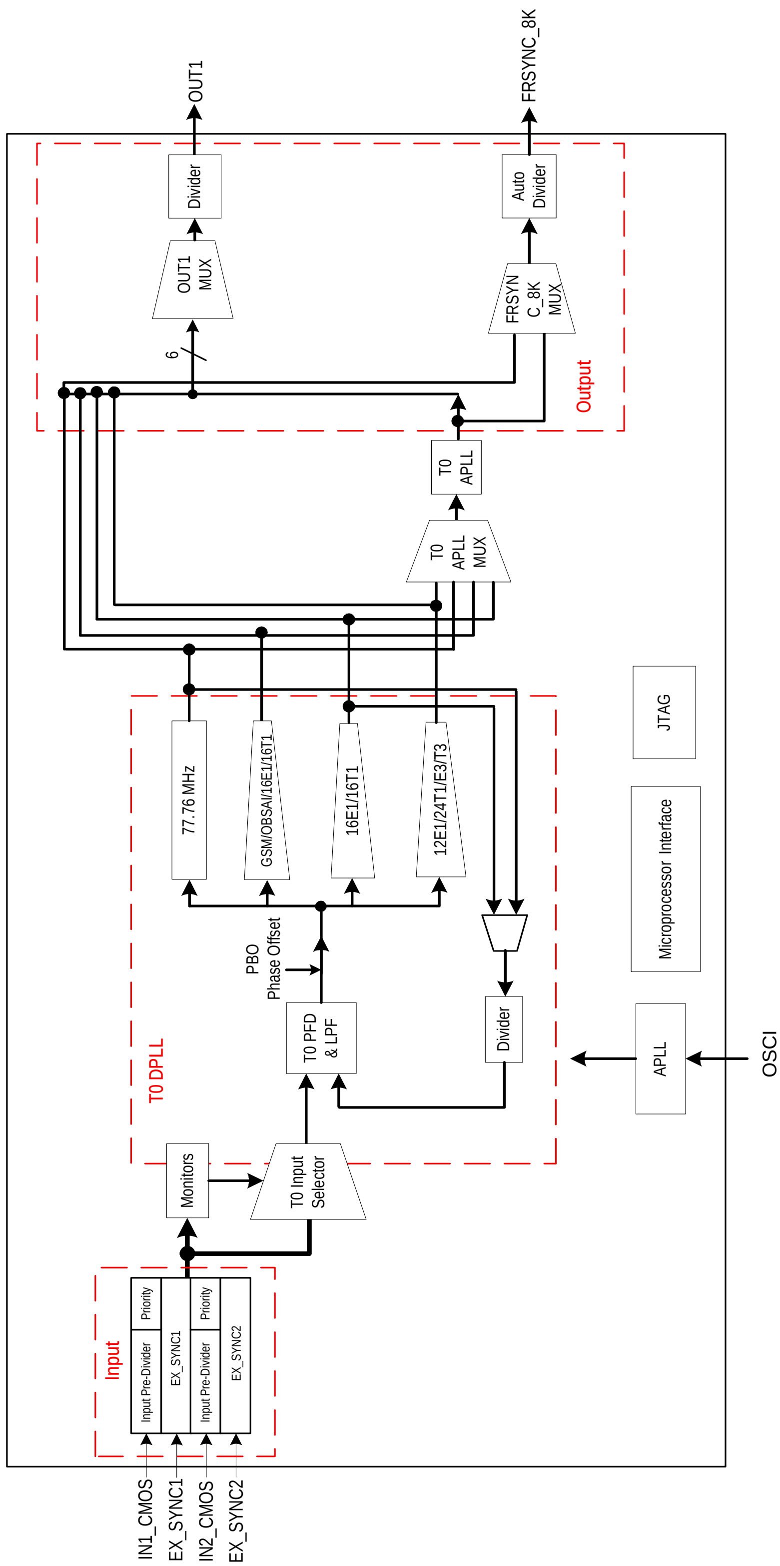


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

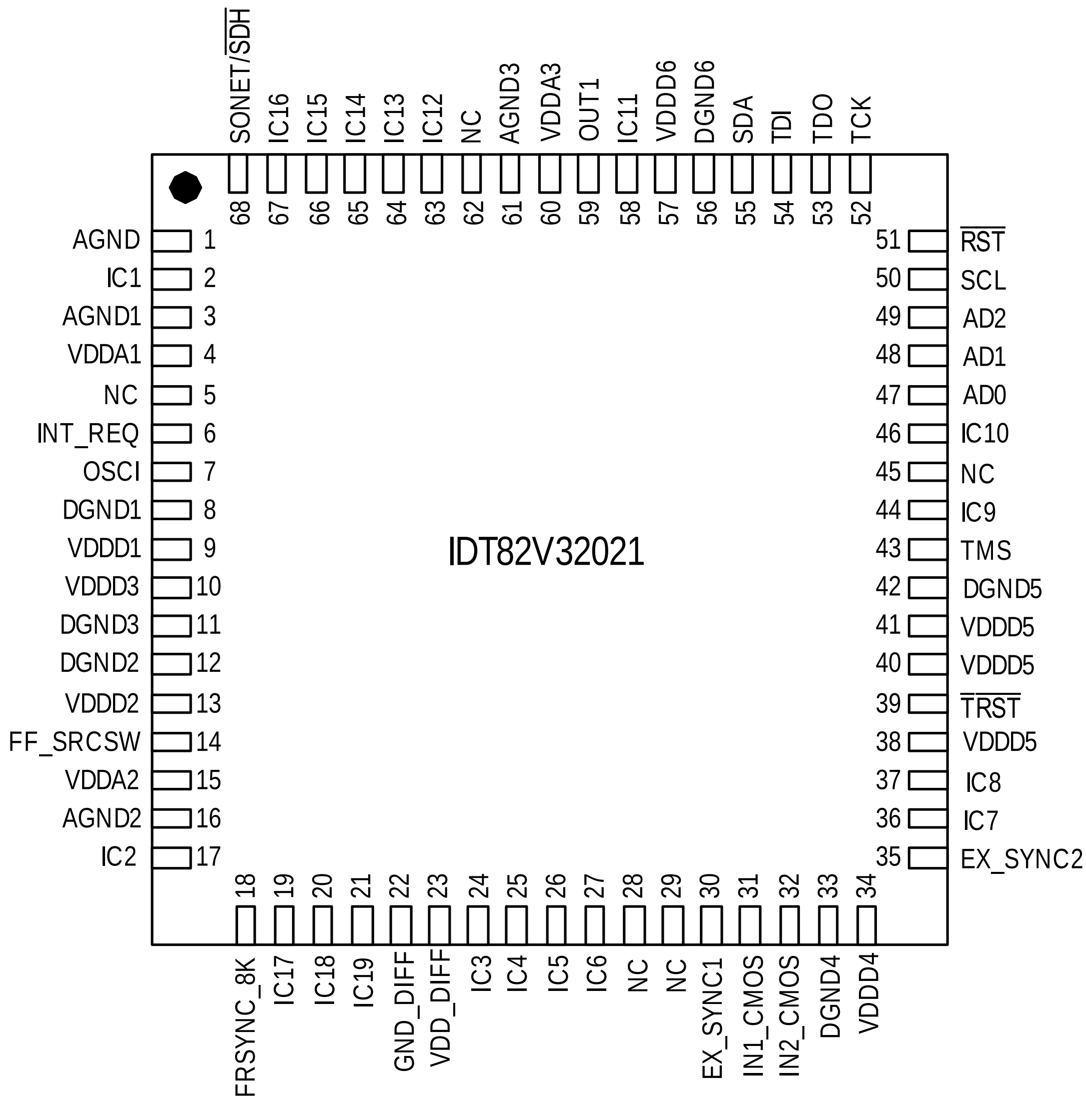


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description [1]
				Global Control Signal
OSCI	7	I	CMOS	**OSCI: Crystal Oscillator Master Clock** A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
FF_SRCSW	14	I pull-down	CMOS	**FF_SRCSW: External Fast Selection Enable** During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) [2]. The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is '1' (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is '0' (External Fast selection is disabled). After reset, this pin selects an input clock for the T0 DPLL if the External Fast selection is enabled: High: IN1_CMOS is selected. Low: IN2_CMOS is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled.
SONET/$\overline{\text{SDH}}$	68	I pull-down	CMOS	**SONET/$\overline{\text{SDH}}$: SONET / SDH Frequency Selection** During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect.
$\overline{\text{RST}}$	51	I pull-up	CMOS	**$\overline{\text{RST}}$: Reset** A low pulse of at least 50 µs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
				Frame Synchronization Input Signal
EX_SYNC1	30	I pull-down	CMOS	**EX_SYNC1: External Sync Input 1** A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
EX_SYNC2	35	I pull-down	CMOS	**EX_SYNC2: External Sync Input 2** A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
				Input Clock
IN1_CMOS	31	I pull-down	CMOS	**IN1_CMOS: Input Clock 1** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN2_CMOS	32	I pull-down	CMOS	**IN2_CMOS: Input Clock 2** A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
				Output Frame Synchronization Signal
FRSYNC_8K	18	O	CMOS	**FRSYNC_8K: 8 kHz Frame Sync Output** An 8 kHz signal is output on this pin.
				Output Clock
OUT1	59	O	CMOS	**OUT1: Output Clock 1** A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 (includes 65.536 MHz) [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
I^2C Programming Interface				
INT_REQ	6	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
AD0 AD1 AD2	47 48 49	I	CMOS	AD[2:0]: Address Input 2 to 0 The address is input on these pins.
SCL	50	I	CMOS	SCL: Serial Clock Line The serial clock is input on this pin. The clock is 100 kbit/s in Standard mode and 400 kbit/s in Fast mode. Should be pulled high via a 10 kΩ resistor.
SDA	55	I/O	CMOS	SDA: Serial Data Input/Output This pin is used as the input/output for the serial data. Should be pulled high via a 10 kΩ resistor.
JTAG (per IEEE 1149.1)				
$\overline{TRST}$	39	I pull-down	CMOS	$\overline{TRST}$: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	43	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	52	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	54	I pull-up	CMOS	TDI: JTAG Test Data Input The test data is input on this pin. It is clocked into the device on the rising edge of TCK.
TDO	53	O	CMOS	TDO: JTAG Test Data Output The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_-FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.
Power & Ground				
VDDD1 VDDD2 VDDD3 VDDD4 VDDD5 VDDD6	9 13 10 34 38, 40, 41 57	Power	-	VDDDn: 3.3 V Digital Power Supply Each VDDDn should be paralleled with ground through a 0.1 µF capacitor.
VDDA1 VDDA2 VDDA3	4 15 60	Power	-	VDDAn: 3.3 V Analog Power Supply Each VDDAn should be paralleled with ground through a 0.1 µF capacitor.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
VDD_DIFF	23	Power	-	VDD_DIFF: 3.3 V Power Supply
DGND1 DGND2 DGND3 DGND4 DGND5 DGND6	8 12 11 33 42 56	Ground	-	DGNDn: Digital Ground
AGND1 AGND2 AGND3	3 16 61	Ground	-	AGNDn: Analog Ground
GND_DIFF	22	Ground	-	GND_DIFF: Ground
AGND	1	Ground	-	AGND: Analog Ground

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
Others				
IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC9 IC10 IC11 IC12 IC13 IC14 IC15 IC16 IC17 IC18 IC19	2 17 24 25 26 27 36 37 44 46 58 63 64 65 66 67 19 20 21	-	-	IC: internally connected Internal Use. These pins should be left open for normal operation.
NC	5, 28, 29, 45, 62	-	-	NC: Not Connected

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \leq N \leq 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64.
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96.
6. N x 13.0 MHz: N = 1, 2, 4.
7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40.

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the $\overline{RST}$ pin must be asserted low for at least 50 µs. After the $\overline{RST}$ pin is pulled high, the device will still be in reset state for 500 ms (typical). If the $\overline{RST}$ pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSCI pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may input on the OSCI pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The performance of the master clock should meet GR-1244-CORE, GR-253-CORE, ITU-T G.812 and G.813 criteria.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	OSCI_CNFG	0A

3.3 INPUT CLOCKS & FRAME SYNC SIGNALS

Altogether two clocks and two frame sync signals are input to the device.

3.3.1 INPUT CLOCKS

The device provides two CMOS input clock ports: IN1_CMOS and IN2_CMOS.

According to the input clock source, the following clock sources are supported:

- T1: Recovered clock from STM-N or OC-n
- T2: PDH network synchronization timing
- T3: External synchronization reference timing

The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is determined by the SONET/$\overline{\text{SDH}}$ pin: high for SONET and low for SDH. After reset, the input signal on the SONET/$\overline{\text{SDH}}$ pin takes no effect.

3.3.2 FRAME SYNC INPUT SIGNALS

Two 2 kHz, 4 kHz or 8 kHz frame sync signals are input on the EX_SYNC1 and EX_SYNC2 pins respectively. They are CMOS inputs. The input frequency should match the setting in the SYNC_FREQ[1:0] bits. The frame sync signals are only valid for the OC-n clock (6.48 MHz, 19.44 MHz, 38.88 MHz and 77.76 MHz) input.

Only one of the two frame sync input signals is used for frame sync output signal synchronization. Refer to Chapter 3.13.2 Frame SYNC Output Signal for details.

Table 3: Related Bit / Register in Chapter 3.3

Bit	Register	Address (Hex)
IN_SONET_SDH	INPUT_MODE_CNFG	09
SYNC_FREQ[1:0]		

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the DPLL required frequency, which is no more than 38.88 MHz. For each input clock, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

If the input clock is of 2 kHz, 4 kHz or 8 kHz, the Pre-Divider is bypassed automatically and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency; the input clock can be inverted, as determined by the IN_2K_4K_8K_INV bit.

Each Pre-Divider consists of a DivN Divider and a Lock 8k Divider, as shown in Figure 3.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used, the division factor setting should observe the following order:

1. *Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;*
2. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
3. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN Divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The DivN Divider can only divide the input clock whose frequency is lower than (<) 155.52 MHz.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz automatically.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the clock input pin and the DPLL required clock. Here is an example:

The input clock on the IN2_CMOS pin is 155.52 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN2_CMOS_CNFG to ‘0010’. Do the following to divide the input clock:

Use the DivN Divider to divide the clock down to 6.48 MHz:
Set the PRE_DIV_CH_VALUE[3:0] bits to ‘0011’;
Set the DIRECT_DIV bit in Register IN2_CMOS_CNFG to ‘1’ and the LOCK_8K bit in Register IN2_CMOS_CNFG to ‘0’;
155.52 ÷ 6.48 = 24; 24 - 1 = 23, so set the PRE_DIVN_VALUE[14:0] bits to ‘10111’.

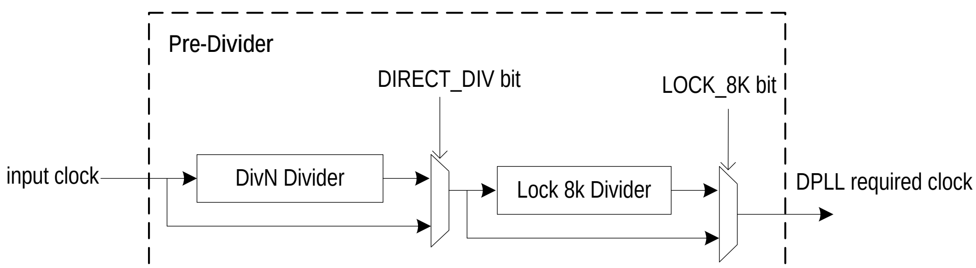


Figure 3. Pre-Divider for An Input Clock

Table 4: Related Bit / Register in Chapter 3.4

Bit	Register	Address (Hex)
IN_FREQ[3:0]	IN1_CMOS_CNFG, IN2_CMOS_CNFG	16, 17
DIRECT_DIV		
LOCK_8K		
IN_2K_4K_8K_INV	FR_SYNC_CNFG	74
PRE_DIV_CH_VALUE[3:0]	PRE_DIV_CH_CNFG	23
PRE_DIVN_VALUE[14:0]	PRE_DIVN[14:8]_CNFG, PRE_DIVN[7:0]_CNFG	25, 24

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of the input clocks are always monitored in the following aspects:

- Activity
- Frequency

The qualified clocks are available for T0 DPLL selection. The T0 selected input clock has to be monitored further. Refer to Chapter 3.7 Selected Input Clock Monitoring for details.

3.5.1 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 4.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_CMOS_NO_ACTIVITY_ALARM bit (n = 1 or 2).

The input clock with a no-activity alarm is disqualified for clock selection for T0 DPLL.

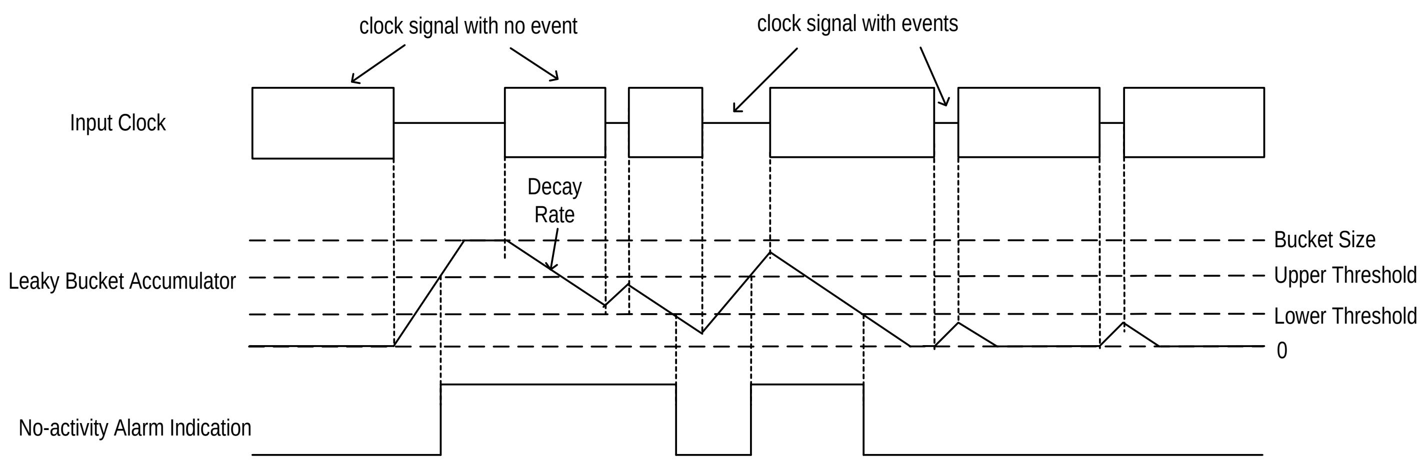


Figure 4. Input Clock Activity Monitoring

3.5.2 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the FREQ_MON_CLK bit.

A frequency hard alarm threshold is set for frequency monitoring. If the FREQ_MON_HARD_EN bit is ‘1’, a frequency hard alarm is raised when the frequency of the input clock with respect to the reference clock is above the threshold; the alarm is cleared when the frequency is below the threshold.

The frequency hard alarm threshold can be calculated as follows:

Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0]

If the FREQ_MON_HARD_EN bit is ‘1’, the frequency hard alarm status of the input clock is indicated by the INn_CMOS_FREQ_HARD_ALARM bit (n = 1 or 2). When the FREQ_MON_HARD_EN bit is ‘0’, no frequency hard alarm is raised even if the input clock is above the frequency hard alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside ±5%, the input clock is disqualified for clock selection for T0 DPLL. The input clock is qualified if any edge drifts inside ±5%. This function is supported only when the IN_NOISE_WINDOW bit is ‘1’.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. *Select an input clock by setting the IN_FREQ_READ_CH[3:0] bits;*
2. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] X FREQ_MON_FACTOR[3:0]

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

Table 5: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
BUCKET_SIZE_n_DATA[7:0] (3 ≥ n ≥ 0)	BUCKET_SIZE_0_CNFG ~ BUCKET_SIZE_3_CNFG	33, 37, 3B, 3F
UPPER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	UPPER_THRESHOLD_0_CNFG ~ UPPER_THRESHOLD_3_CNFG	31, 35, 39, 3D
LOWER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	LOWER_THRESHOLD_0_CNFG ~ LOWER_THRESHOLD_3_CNFG	32, 36, 3A, 3E
DECAY_RATE_n_DATA[1:0] (3 ≥ n ≥ 0)	DECAY_RATE_0_CNFG ~ DECAY_RATE_3_CNFG	34, 38, 3C, 40
BUCKET_SEL[1:0]	IN1_CMOS_CNFG, IN2_CMOS_CNFG	16, 17
INn_CMOS_NO_ACTIVITY_ALARM (n = 1 or 2)	IN1_IN2_CMOS_STS	44
INn_CMOS_FREQ_HARD_ALARM (n = 1 or 2)		
FREQ_MON_CLK	MON_SW_PBO_CNFG	0B
FREQ_MON_HARD_EN		
ALL_FREQ_HARD_THRESHOLD[3:0]	ALL_FREQ_MON_THRESHOLD_CNFG	2F
FREQ_MON_FACTOR[3:0]	FREQ_MON_FACTOR_CNFG	2E
IN_NOISE_WINDOW	PHASE_MON_PBO_CNFG	78
IN_FREQ_READ_CH[3:0]	IN_FREQ_READ_CH_CNFG	41
IN_FREQ_VALUE[7:0]	IN_FREQ_READ_STS	42

3.6 DPLL INPUT CLOCK SELECTION

The EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in Table 6:

Table 6: Input Clock Selection

Control Bits		Input Clock Selection
EXT_SW	T0_INPUT_SEL[3:0]	
1	don't-care	External Fast selection
0	other than 0000	Forced selection
	0000	Automatic selection

External Fast selection is done between IN1_CMOS and IN2_CMOS.

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

The selected input clock is attempted to be locked by T0 DPLL.

3.6.1 EXTERNAL FAST SELECTION

In External Fast selection, only IN1_CMOS and IN2_CMOS are available for selection. Refer to Figure 5. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRCSW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to Chapter 2 Pin Description), the IN1_CMOS_SEL_PRIORITY[3:0] bits and the IN2_CMOS_SEL_PRIORITY[3:0] bits, as shown in Figure 5 and Table 7:

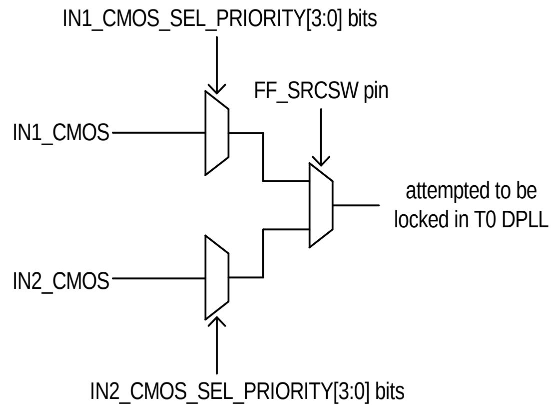


Figure 5. External Fast Selection

Table 7: External Fast Selection

Control Pin & Bits			the Selected Input Clock
FF_SRCSW (after reset)	IN1_CMOS_SEL_PRIORITY[3:0]	IN2_CMOS_SEL_PRIORITY[3:0]	
high	other than 0000	don't-care	IN1_CMOS
low	don't-care	other than 0000	IN2_CMOS

3.6.2 FORCED SELECTION

In Forced selection, the selected input clock is set by the T0_INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect the input clock selection.

3.6.3 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity and priority. The validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring).

In the qualified input clocks, the one with the higher priority is selected. The priority is configured by the corresponding INn_CMOS_SEL_PRIORITY[3:0] bits (n = 1 or 2). If more than one qualified input clock is available and has the same priority, the input clock with the smaller 'n' is selected. See Table 8 for the 'n' assigned to the input clock.

Table 8: 'n' Assigned to the Input Clock

Input Clock	'n' Assigned to the Input Clock
IN1_CMOS	1
IN2_CMOS	3

Table 9: Related Bit / Register in Chapter 3.6

Bit	Register	Address (Hex)
EXT_SW	MON_SW_PBO_CNFG	0B
T0_INPUT_SEL[3:0]	T0_INPUT_SEL_CNFG	50
INn_CMOS_SEL_PRIORITY[3:0] (n = 1 or 2)	IN1_IN2_CMOS_SEL_PRIORITY_CNFG	27

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to Chapter 3.5 Input Clock Quality Monitoring) and the DPLL locking status is always monitored.

3.7.1 DPLL LOCKING DETECTION

The following events is always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

The occurrence of the fast loss will result in T0 DPLL unlocked if the FAST_LOS_SW bit is '1'.

3.7.1.2 Coarse Phase Loss

The T0 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 10. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 11.

Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
0	don't-care	±1 UI
1	0	±1 UI
	1	set by the PH_LOS_COARSE_LIMT[3:0] bits

Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

WIDE_EN	Coarse Phase Limit
0	±1 UI
1	set by the PH_LOS_COARSE_LIMT[3:0] bits

The occurrence of the coarse phase loss will result in T0 DPLL unlocked if the COARSE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.3 Fine Phase Loss

The T0 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in T0 DPLL unlocked if the FINE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the T0 DPLL locking status. The DPLL soft alarm is indicated by the corresponding T0_DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in T0 DPLL unlocked if the FREQ_LIMT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

DPLL Soft Limit (ppm) = DPLL_FREQ_SOFT_LIMT[6:0] X 0.724

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

DPLL Hard Limit (ppm) = DPLL_FREQ_HARD_LIMT[15:0] X 0.0014

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Coarse Phase Loss (the COARSE_PH_LOS_LIMT_EN bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the T0_DPLL_LOCK bit.

3.7.3 PHASE LOCK ALARM

A phase lock alarm will be raised when the selected input clock can not be locked in T0 DPLL within a certain period. This period can be calculated as follows:

Period (sec.) = TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0]

The phase lock alarm is indicated by the corresponding INn_CMOS_PH_LOCK_ALARM bit (n = 1 or 2).

The phase lock alarm can be cleared by the following two ways, as selected by the PH_ALARM_TIMEOUT bit:

- Be cleared when a '1' is written to the corresponding INn_CMOS_PH_LOCK_ALARM bit;
- Be cleared after the period (= *TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0] in second*) which starts from when the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for T0 DPLL locking.

Table 12: Related Bit / Register in Chapter 3.7

Bit	Register	Address (Hex)
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B
PH_LOS_FINE_LIMT[2:0]		
FINE_PH_LOS_LIMT_EN		
MULTI_PH_8K_4K_2K_EN	PHASE_LOSS_COARSE_LIMIT_CNFG	5A
WIDE_EN		
PH_LOS_COARSE_LIMT[3:0]		
COARSE_PH_LOS_LIMT_EN		
T0_DPLL_SOFT_FREQ_ALARM	OPERATING_STS	52
T0_DPLL_LOCK		
DPLL_FREQ_SOFT_LIMT[6:0]	DPLL_FREQ_SOFT_LIMIT_CNFG	65
FREQ_LIMT_PH_LOS		
DPLL_FREQ_HARD_LIMT[15:0]	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG, DPLL_FREQ_HARD_LIMIT[7:0]_CNFG	67, 66
TIME_OUT_VALUE[5:0]	PHASE_ALARM_TIME_OUT_CNFG	08
MULTI_FACTOR[1:0]		
INn_CMOS_PH_LOCK_ALARM (n = 1 or 2)	IN1_IN2_CMOS_STS	44
PH_ALARM_TIMEOUT	INPUT_MODE_CNFG	09

3.8 SELECTED INPUT CLOCK SWITCH

If the input clock is selected by External Fast selection or by Forced selection, it can be switched by setting the related registers (refer to Chapter 3.6.1 External Fast Selection & Chapter 3.6.2 Forced Selection) any time. In this case, whether the input clock is qualified for DPLL locking does not affect the clock switch.

When the input clock is selected by Automatic selection, the input clock switch depends on its validity and priority. If the current selected input clock is disqualified, a new qualified input clock may be switched to.

3.8.1 INPUT CLOCK VALIDITY

For the input clocks, the validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). When all of the following conditions are satisfied, the input clock is valid; otherwise, it is invalid.

- No no-activity alarm (the INn_CMOS_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_CMOS_FREQ_HARD_ALARM bit is '0');
- If the IN_NOISE_WINDOW bit is '1', all the edges of the input clock of 2 kHz, 4 kHz or 8 kHz drift inside ±5%; if the IN_NOISE_WINDOW bit is '0', this condition is ignored.
- No phase lock alarm, i.e., the INn_CMOS_PH_LOCK_ALARM bit is '0';
- If the ULTR_FAST_SW bit is '1', the T0 selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored.

The validities of the input clocks are indicated by the INn_CMOS [1] bit (n = 1 or 2). When the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), the INn_CMOS [2] bit will be set. If the INn_CMOS [3] bit is '1', an interrupt will be generated.

When the T0 selected input clock has failed, i.e., the validity of the T0 selected input clock changes from 'valid' to 'invalid', the T0_MAIN_REF_FAILED [1] bit will be set. If the T0_MAIN_REF_FAILED [2] bit is '1', an interrupt will be generated. This interrupt can also be indicated by hardware - the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. When the TDO pin is used to indicate this interrupt, it will be set high when this interrupt is generated and will remain high until this interrupt is cleared.

3.8.2 SELECTED INPUT CLOCK SWITCH

Revertive and Non-Revertive switches are supported, as selected by the REVERTIVE_MODE bit.

The difference between Revertive and Non-Revertive switches is that whether the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available for selection. In Non-Revertive switch, input clock switch is minimized.

Conditions of the qualified input clocks available for T0 selection are as the following:

- Valid, i.e., the INn_CMOS [1] bit is '1';
- Priority enabled, i.e., the corresponding INn_CMOS_SEL _PRIORITY[3:0] bits are not '0000'.

The input clock is disqualified if any of the above conditions is not satisfied.

In summary, the selected input clock can be switched by:

- External Fast selection;
- Forced selection;
- Revertive switch;
- Non-Revertive switch.

3.8.2.1 Revertive Switch

In Revertive switch, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available.

The selected input clock is switched if any of the following is satisfied:

- The selected input clock is disqualified;
- Another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the higher priority is selected by revertive switch. If more than one qualified input clock is available and has the same priority, the input clock with the smaller 'n' is selected. See Table 8 for the 'n' assigned to each input clock.

3.8.2.2 Non-Revertive Switch

In Non-Revertive switch, the T0 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock is available. In this case, the selected input clock is switched and a qualified input clock with the higher priority is selected only when the T0 selected input clock is disqualified. If more than one qualified input clock is available and has the same priority, the input clock with the smaller 'n' is selected. See Table 8 for the 'n' assigned to each input clock.

3.8.3 SELECTED / QUALIFIED INPUT CLOCKS INDICATION

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits.

The qualified input clocks with the two highest priorities are indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits and the SECOND_HIGHEST_PRIORITY_VALIDATED[3:0] bits respectively. If more than one input clock has the same priority, the input clock with the smaller 'n' is indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits. See Table 8 for the 'n' assigned to the input clock.

When the device is configured in Automatic selection and Revertive switch is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits; otherwise, they are not the same.

Table 13: Related Bit / Register in Chapter 3.8

Bit	Register	Address (Hex)
INn_CMOS [1] (n = 1 or 2)	INPUT_VALID1_STS	4A
INn_CMOS [2] (n = 1 or 2)	INTERRUPTS1_STS, INTERRUPTS2_STS	0D, 0E
INn_CMOS [3] (n = 1 or 2)	INTERRUPTS1_ENABLE_CNFG, INTERRUPTS2_ENABLE_CNFG	10, 11
INn_CMOS_NO_ACTIVITY_ALARM (n = 1 or 2)	IN1_IN2_CMOS_STS	44
INn_CMOS_FREQ_HARD_ALARM (n = 1 or 2)		
INn_CMOS_PH_LOCK_ALARM (n = 1 or 2)		
IN_NOISE_WINDOW	PHASE_MON_PBO_CNFG	78
ULTR_FAST_SW	MON_SW_PBO_CNFG	0B
LOS_FLAG_TO_TDO		
T0_MAIN_REF_FAILED [1]	INTERRUPTS2_STS	0E
T0_MAIN_REF_FAILED [2]	INTERRUPTS2_ENABLE_CNFG	11
REVERTIVE_MODE	INPUT_MODE_CNFG	09
INn_CMOS_SEL_PRIORITY[3:0] (n = 1 or 2)	IN1_IN2_CMOS_SEL_PRIORITY_CNFG	27
CURRENTLY_SELECTED_INPUT[3:0]	PRIORITY_TABLE1_STS	4E
HIGHEST_PRIORITY_VALIDATED[3:0]		
SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]	PRIORITY_TABLE2_STS	4F

3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE

T0 DPLL supports three primary operating modes: Free-Run, Locked and Holdover, and three secondary, temporary operating modes: Pre-Locked, Pre-Locked2 and Lost-Phase. The operating mode of T0 DPLL can be switched automatically or by force, as controlled by the T0_OPERATING_MODE[2:0] bits.

When the operating mode is switched by force, the operating mode switch is under external control and the status of the selected input clock takes no effect to the operating mode selection. The forced operating mode switch is applicable for special cases, such as testing.

When the operating mode is switched automatically, the internal state machine for T0 automatically determine the operating mode.

The T0 DPLL operating mode is controlled by the T0_OPERATING_MODE[2:0] bits, as shown in Table 14:

Table 14: T0 DPLL Operating Mode Control

T0_OPERATING_MODE[2:0]	T0 DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked
101	Forced - Pre-Locked2
110	Forced - Pre-Locked
111	Forced - Lost-Phase

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 6.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the T0_DPLL_OPERATING_MODE[2:0] bits. When the operating mode switches, the T0_OPERATING_MODE [1] bit will be set. If the T0_OPERATING_MODE [2] bit is '1', an interrupt will be generated.

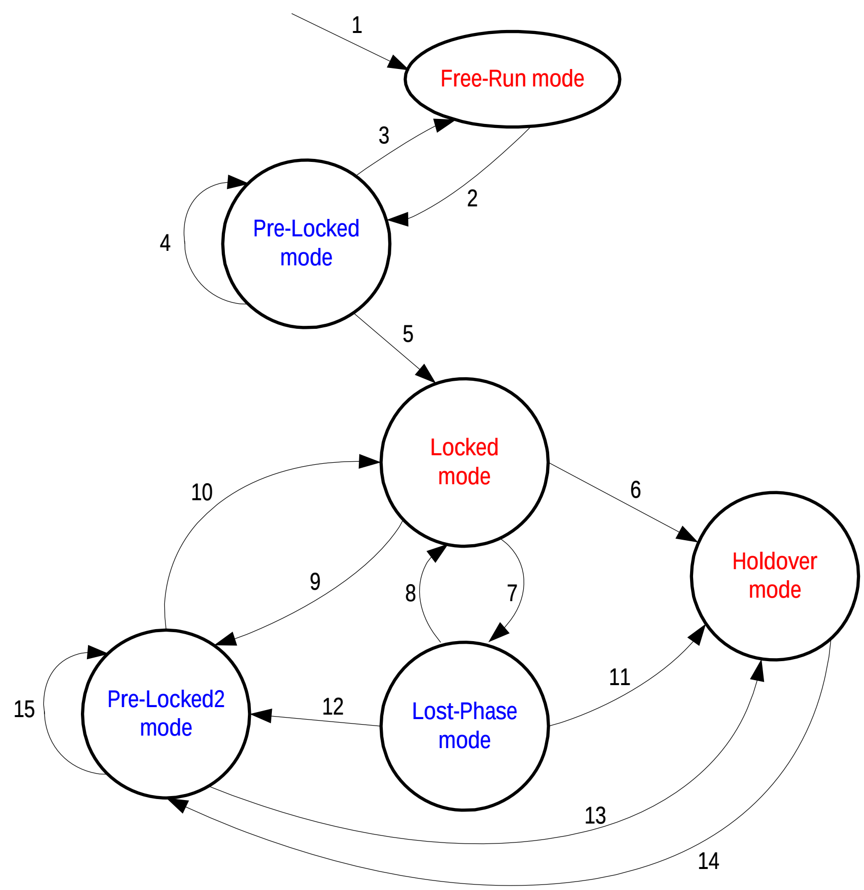


Figure 6. T0 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 6:

1. Reset.

2. An input clock is selected.

3. The T0 selected input clock is disqualified AND No qualified input clock is available.

4. The T0 selected input clock is switched to another one.

5. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').

6. The T0 selected input clock is disqualified AND No qualified input clock is available.

7. The T0 selected input clock is unlocked (the T0_DPLL_LOCK bit is '0').

8. The T0 selected input clock is locked again (the T0_DPLL_LOCK bit is '1').

9. The T0 selected input clock is switched to another one.

10. The T0 selected input clock is locked (the T0_DPLL_LOCK bit is '1').

11. The T0 selected input clock is disqualified AND No qualified input clock is available.

12. The T0 selected input clock is switched to another one.

13. The T0 selected input clock is disqualified AND No qualified input clock is available.

14. An input clock is selected.

15. The T0 selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the T0 selected input clock is switched to another one' - are: (The T0 selected input clock is disqualified AND Another input clock is switched to) OR (In Revertive switch, a qualified input clock with a higher priority is switched to) OR (The T0 selected input clock is switched to another one by External Fast selection or Forced selection).

Refer to Chapter 3.8.2 Selected Input Clock Switch for details about T0 input clock qualification.

Table 15: Related Bit / Register in Chapter 3.9

Bit	Register	Address (Hex)
T0_OPERATING_MODE[2:0]	T0_OPERATING_MODE_CNFG	53
T0_DPLL_OPERATING_MODE[2:0]	OPERATING_STS	52
T0_DPLL_LOCK		
T0_OPERATING_MODE [1]	INTERRUPTS2_STS	0E
T0_OPERATING_MODE [2]	INTERRUPTS2_ENABLE_CNFG	11

3.10 DPLL OPERATING MODE

The T0 DPLL gives a stable performance in different applications without being affected by operating conditions or silicon process variations. It integrates a PFD (Phase & Frequency Detector), a LPF (Low Pass Filter) and a DCO (Digital Controlled Oscillator), which forms a closed loop. If no input clock is selected, the loop is not closed, and the PFD and LPF do not function.

The PFD detects the phase error, including the fast loss, coarse phase loss and fine phase loss (refer to Chapter 3.7.1.1 Fast Loss to Chapter 3.7.1.3 Fine Phase Loss). The averaged phase error of the T0 DPLL feedback with respect to the selected input clock is indicated by the CURRENT_PH_DATA[15:0] bits. It can be calculated as follows:

Averaged Phase Error (ns) = CURRENT_PH_DATA[15:0] X 0.61

The LPF filters jitters. Its 3 dB bandwidth and damping factor are programmable. A range of bandwidths and damping factors can be set to meet different application requirements. Generally, the lower the damping factor is, the longer the locking time is and the more the gain is.

The DCO controls the DPLL output. The frequency of the DPLL output is always multiplied on the basis of the master clock. The phase and frequency offset of the DPLL output may be locked to those of the selected input clock. The current frequency offset with respect to the master clock is indicated by the CURRENT_DPLL_FREQ[23:0] bits, and can be calculated as follows:

Current Frequency Offset (ppm) = CURRENT_DPLL_FREQ[23:0] X 0.000011

3.10.1 SIX OPERATING MODES

The T0 DPLL loop is closed except in Free-Run mode and Holdover mode.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the T0 DPLL attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the T0_DPLL_START_BW[4:0] bits and the T0_DPLL_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the T0_DPLL_ACQ_BW[4:0] bits and the T0_DPLL_ACQ_DAMPING[2:0] bits respectively.

When the T0 selected input clock is locked, the locked bandwidth and damping factor are used. They are set by the T0_DPLL_LOCKED_BW[4:0] bits and the T0_DPLL_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the T0 DPLL operates in different DPLL locking stages: starting, acquisition and locked, as controlled by the device automatically.

Only the locked bandwidth and damping factor can be used regardless of the T0 DPLL locking stage, as controlled by the AUTO_BW_SEL bit.

3.10.1.1 Free-Run Mode

In Free-Run mode, the T0 DPLL output refers to the master clock and is not affected by any input clock. The accuracy of the T0 DPLL output is equal to that of the master clock.

3.10.1.2 Pre-Locked Mode

In Pre-Locked mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.10.1.3 Locked Mode

In Locked mode, the T0 selected input clock is locked. The phase and frequency offset of the T0 DPLL output track those of the T0 selected input clock.

In this mode, if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is ‘1’, the T0 DPLL is unlocked (refer to Chapter 3.7.1.1 Fast Loss) and will enter Lost-Phase mode when the operating mode is switched automatically; if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is ‘0’, the T0 DPLL locking status is not affected and the T0 DPLL will enter Temp-Holdover mode automatically.

3.10.1.3.1 Temp-Holdover Mode

The T0 DPLL will automatically enter Temp-Holdover mode with a selected input clock switch or no qualified input clock available when the operating mode switch is under external control.

In Temp-Holdover mode, the T0 DPLL has temporarily lost the selected input clock. The T0 DPLL operation in Temp-Holdover mode and that in Holdover mode are alike (refer to Chapter 3.10.1.5 Holdover Mode) except the frequency offset acquiring methods. See Chapter 3.10.1.5 Holdover Mode for details about the methods. The method is selected by the TEMP_HOLDOVER_MODE[1:0] bits, as shown in Table 16:

Table 16: Frequency Offset Control in Temp-Holdover Mode

TEMP_HOLDOVER_MODE[1:0]	Frequency Offset Acquiring Method
00	the same as that used in Holdover mode
01	Automatic Instantaneous
10	Automatic Fast Averaged
11	Automatic Slow Averaged

The device automatically controls the T0 DPLL to exit from Temp-Holdover mode.

3.10.1.4 Lost-Phase Mode

In Lost-Phase mode, the T0 DPLL output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.10.1.5 Holdover Mode

In Holdover mode, the T0 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T0 DPLL output is not phase locked to any input clock. The frequency offset acquiring method is selected by the MAN_HOLDOVER bit, the AUTO_AVG bit and the FAST_AVG bit, as shown in Table 17:

Table 17: Frequency Offset Control in Holdover Mode

MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged
		1	Automatic Fast Averaged
1	don't-care		Manual

3.10.1.5.1 Automatic Instantaneous

By this method, the T0 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is $4.4X10^{-8}$ ppm.

3.10.1.5.2 Automatic Slow Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 110 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.5.3 Automatic Fast Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 8 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.5.4 Manual

By this method, the frequency offset is set by the T0_HOLDOVER_FREQ[23:0] bits. The accuracy is $1.1X10^{-5}$ ppm.

The frequency offset of the T0 DPLL output is indicated by the CURRENT_DPLL_FREQ[23:0] bits.

The device provides a reference for the value to be written to the T0_HOLDOVER_FREQ[23:0] bits. The value to be written can refer to the value read from the CURRENT_DPLL_FREQ[23:0] bits or the T0_HOLDOVER_FREQ[23:0] bits (refer to Chapter 3.10.1.5.5 Holdover Frequency Offset Read); or then be processed by external software filtering.

3.10.1.5.5 Holdover Frequency Offset Read

The offset value, which is acquired by Automatic Slow Averaged, Automatic Fast Averaged and is set by related register bits, can be read from the T0_HOLDOVER_FREQ[23:0] bits by setting the READ_AVG bit and the FAST_AVG bit, as shown in Table 18.

Table 18: Holdover Frequency Offset Read

READ_AVG	FAST_AVG	Offset Value Read from T0_HOLDOVER_FREQ[23:0]
0	don't-care	The value is equal to the one written to.
1	0	The value is acquired by Automatic Slow Averaged method, not equal to the one written to.
	1	The value is acquired by Automatic Fast Averaged method, not equal to the one written to.

The frequency offset in ppm is calculated as follows:

Holdover Frequency Offset (ppm) = T0_HOLDOVER_FREQ[23:0] X 0.000011

3.10.1.6 Pre-Locked2 Mode

In Pre-Locked2 mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

Table 19: Related Bit / Register in Chapter 3.10

Bit	Register	Address (Hex)
CURRENT_PH_DATA[15:0]	CURRENT_DPLL_PHASE[15:8]_STS, CURRENT_DPLL_PHASE[7:0]_STS	69, 68
CURRENT_DPLL_FREQ[23:0]	CURRENT_DPLL_FREQ[23:16]_STS, CURRENT_DPLL_FREQ[15:8]_STS, CURRENT_DPLL_-FREQ[7:0]_STS	64, 63, 62
T0_DPLL_START_BW[4:0]	T0_DPLL_START_BW_DAMPING_CNFG	56
T0_DPLL_START_DAMPING[2:0]		
T0_DPLL_ACQ_BW[4:0]	T0_DPLL_ACQ_BW_DAMPING_CNFG	57
T0_DPLL_ACQ_DAMPING[2:0]		
T0_DPLL_LOCKED_BW[4:0]	T0_DPLL_LOCKED_BW_DAMPING_CNFG	58
T0_DPLL_LOCKED_DAMPING[2:0]		
AUTO_BW_SEL	T0_BW_OVERSHOOT_CNFG	59
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B
TEMP_HOLDOVER_MODE[1:0]	T0_HOLDOVER_MODE_CNFG	5C
MAN_HOLDOVER		
AUTO_AVG		
FAST_AVG		
READ_AVG		
T0_HOLDOVER_FREQ[23:0]	T0_HOLDOVER_FREQ[23:16]_CNFG, T0_HOLDOVER_FREQ[15:8]_CNFG, T0_HOLDOVER_-FREQ[7:0]_CNFG	5F, 5E, 5D

3.11 DPLL OUTPUT

The DPLL output is locked to the selected input clock. According to the phase-compared result of the feedback and the selected input clock, and the DPLL output frequency offset, the PFD output is limited and the DPLL output is frequency offset limited.

3.11.1 PFD OUTPUT LIMIT

The PFD output is limited to be within ±1 UI or within the coarse phase limit (refer to Chapter 3.7.1.2 Coarse Phase Loss), as determined by the MULTI_PH_APP bit.

3.11.2 FREQUENCY OFFSET LIMIT

The DPLL output is limited to be within the DPLL hard limit (refer to Chapter 3.7.1.4 Hard Limit Exceeding).

The integral path value can be frozen when the DPLL hard limit is reached. This function, enabled by the T0_LIMT bit, will minimize the subsequent overshoot when T0 DPLL is pulling in.

3.11.3 PBO

When a PBO event is triggered, the phase offset of the selected input clock with respect to the T0 DPLL output is measured. The device then automatically accounts for the measured phase offset and compensates an appropriate phase offset into the DPLL output so that the phase transients on the T0 DPLL output are minimized.

A PBO event is triggered if any one of the following conditions occurs:

- T0 selected input clock switches (the PBO_EN bit is ‘1’);
- T0 DPLL exits from Holdover mode or Free-Run mode (the PBO_EN bit is ‘1’);
- Phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds (the PH_MON_PBO_EN bit is ‘1’).

For the first two conditions, the phase transients on the T0 DPLL output are minimized to be no more than 0.61 ns with PBO. The PBO can also be frozen at the current phase offset by setting the PBO_FREZ bit. When the PBO is frozen, the device will ignore any further PBO events triggered by the above two conditions, and maintain the current phase offset. When the PBO is disabled, there may be a phase shift on the T0 DPLL output and the T0 DPLL output tracks back to 0 degree phase offset with respect to the T0 selected input clock.

The last condition is specially for stratum 2 and 3E clocks. The PBO requirement specified in the Telcordia GR-1244-CORE is: ‘Input phase-time changes of 3.5 µs or greater over an interval of less than 0.1 seconds or less shall be built-out by stratum 2 and 3E clocks to reduce the resulting clock phase-time change to less than 50 ns. Phase-time changes of 1.0 µs or less over an interval of 0.1 seconds shall not be built-out.’ Based on this requirement, phase-time changes of more than 1.0 µs but less than 3.5 µs that occur over an interval of less than 0.1 seconds may or may not be built-out.

An integrated Phase Transient Monitor can be enabled by the PH_MON_EN bit to monitor the phase-time changes on the T0 selected input clock. When the phase-time changes are greater than a limit over an interval of less than 0.1 seconds, a PBO event is triggered and the phase transients on the DPLL output are absorbed. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits, and can be calculated as follows:

Limit (ns) = (PH_TR_MON_LIMT[3:0] + 7) X 156

The phase offset induced by PBO will never result in a coarse or fine phase loss.

3.11.4 FOUR PATHS OF T0 DPLL OUTPUT

The T0 DPLL output is phase aligned with the T0 selected input clock every 125 µs period. T0 DPLL has four output paths as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/OBSAI/16E1/16T1 path - outputs a GSM, OBSAI, 16E1 or 16T1 clock, as selected by the T0_GSM_OBSAI_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T0_12E1_24T1_E3_T3_SEL[1:0] bits.

T0 selected input clock is compared with a T0 DPLL output for DPLL locking. The output can only be derived from the 77.76 MHz path or the 16E1/16T1 path. The output path is automatically selected and the output is automatically divided to get the same frequency as the T0 selected input clock.

T0 DPLL outputs are provided for T0 APLL or device output process.

Table 20: Related Bit / Register in Chapter 3.11

Bit	Register	Address (Hex)
MULTI_PH_APP	PHASE_LOSS_COARSE_LIMIT_CNFG	5A
T0_LIMT	T0_BW_OVERSHOOT_CNFG	59
PBO_EN	MON_SW_PBO_CNFG	0B
PBO_FREZ		
PH_MON_PBO_EN	PHASE_MON_PBO_CNFG	78
PH_MON_EN		
PH_TR_MON_LIMT[3:0]		
PH_OFFSET_EN	PHASE_OFFSET[9:8]_CNFG	7B
IN_SONET_SDH	INPUT_MODE_CNFG	09
T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	T0_DPLL_APLL_PATH_CNFG	55
T0_12E1_24T1_E3_T3_SEL[1:0]		

3.12 T0 APLL

A T0 APLL is provided for a better jitter and wander performance of the device output clock.

The bandwidth of the T0 APLL is set by the T0_APLL_BW[1:0] bits. The lower the bandwidth is, the better the jitter and wander performance of the T0 APLL output are.

The input of the T0 APLL can be derived from T0 DPLL output, as selected by the T0_APLL_PATH[3:0] bits.

Both the APLL and DPLL outputs are provided for selection for the device output.

Table 21: Related Bit / Register in Chapter 3.12

Bit	Register	Address (Hex)
T0_APLL_BW[1:0]	T0_APLL_BW_CNFG	6A
T0_APLL_PATH[3:0]	T0_DPLL_APLL_PATH_CNFG	55

3.13 OUTPUT CLOCK & FRAME SYNC SIGNALS

The device supports 1 output clock and 1 frame sync output signal altogether.

3.13.1 OUTPUT CLOCK

The device provides 1 output clock.

The output on OUT1 is variable, depending on the signals derived from the T0 DPLL and T0 APLL outputs, and the corresponding OUT1_PATH_SEL[3:0] bits. The derived signal can be from the T0 DPLL and T0 APLL outputs, as selected by the corresponding OUT1_PATH_SEL[3:0] bits. If the signal is derived from the T0 DPLL output, please refer to Table 22 for the output frequency. If the signal is derived from the T0 APLL output, please refer to Table 23 for the output frequency.

The output on OUT1 can be inverted, as determined by the corresponding OUT1_INV bit.

The output clock derived from T0 selected input clock is aligned with the T0 selected input clock every 125 µs period.

Table 22: Output on OUT1 if Derived from T0 DPLL Output

OUT1_DIVIDER[3:0] (Output Divider)	output on OUT1 if derived from T0 DPLL output [1]								
	77.76 MHz	12E1	16E1	24T1	16T1	E3	T3	GSM (26 MHz)	OBSAI (30.72 MHz)
0000	Output is disabled (output low).								
0001									
0010		12E1	16E1	24T1	16T1	E3	T3		
0011		6E1	8E1	12T1	8T1			13 MHz	15.36 MHz
0100		3E1	4E1	6T1	4T1				
0101		2E1		4T1					
0110			2E1	3T1	2T1				
0111		E1		2T1					
1000			E1		T1				
1001				T1					
1010	64 kHz								
1011	8 kHz								
1100	2 kHz								
1101	400 Hz								
1110	1Hz								
1111	Output is disabled (output high).								

Note:
1. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.

Table 23: Output on OUT1 if Derived from T0 APLL

OUT1_DIVIDER[3:0] (Output Divider)	output on OUT1 if derived from T0 APLL output [1]								
	77.76 MHz X 4	12E1 X 4	16E1 X 4	24T1 X 4	16T1 X 4	E3	T3	GSM (26 MHz X 2)	OBSAI (30.72 MHz X 10)
0000	Output is disabled (output low).								
0001									
0010		48E1	64E1	96T1	64T1	E3	T3	52 MHz	
0011	155.52 MHz	24E1	32E1	48T1	32T1			26 MHz	153.6 MHz
0100	77.76 MHz	12E1	16E1	24T1	16T1			13 MHz	76.8 MHz
0101	51.84 MHz	8E1		16T1					
0110	38.88 MHz	6E1	8E1	12T1	8T1				38.4 MHz
0111	25.92 MHz	4E1		8T1					
1000	19.44 MHz	3E1	4E1	6T1	4T1				
1001		2E1		4T1					61.44 MHz [2]
1010			2E1	3T1	2T1				30.72 MHz [2]
1011	6.48 MHz	E1		2T1					15.36 MHz [2]
1100			E1		T1				7.68 MHz [2]
1101				T1					3.84 MHz [2]
1110									
1111	Output is disabled (output high).								

Note:
1. In the APLL, the selected T0 DPLL output may be multiplied. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.
2. The 61.44 MHz, 30.72 MHz, 15.36 MHz, 7.68 MHz and 3.84 MHz outputs are only derived from T0 APLL.

3.13.2 FRAME SYNC OUTPUT SIGNAL

An 8 kHz frame sync signal is output on the FRSYNC_8K pin if enabled by the 8K_EN bit. It is a CMOS output.

The frame sync signal is derived from the T0 APLL output and are aligned with the output clock. It can be synchronized to one of the two frame sync input signals.

One of the two frame sync input signals is selected, as determined by the SYNC_BYPASS bit and the T0 selected input clock, as shown in Table 24:

Table 24: Frame Sync Input Signal Selection

SYNC_BYPASS	T0 Selected Input Clock	Selected Frame Sync Input Signal
0	don't-care	EX_SYNC1
1	IN1_CMOS	EX_SYNC1
	IN2_CMOS	EX_SYNC2
	none	none

If the selected frame sync input signal with respect to the T0 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and the selected frame sync input signal is disabled to synchronize the frame sync output signal. The external sync alarm is cleared once the selected frame sync input signal with respect to the T0 selected input clock is within the limit. If it is within the limit, whether the selected frame sync input signal is enabled to synchronize the frame sync output signal is determined by the SYNC_BYPASS bit, the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit. Refer to Table 25 for details.

When the selected frame sync input signal is enabled to synchronize the frame sync output signal, it should be adjusted to align itself with the T0 selected input clock. Nominally, the falling edge of the selected frame sync input signal is aligned with the rising edge of the T0 selected input clock. The selected frame sync input signal may be 0.5 UI early/late or 1 UI late due to the circuit and board wiring delays. Setting the sampling of the selected frame sync input signal by the SYNC_PHn[1:0] bits (n = 1 or 2 corresponding to EX_SYNC1 or EX_SYNC2 respectively) will compensate this early/late. Refer to Figure 7 to Figure 10.

The EX_SYNC_ALARM_MON bit indicates whether the selected frame sync input signal is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM [1] bit. If the EX_SYNC_ALARM [2] bit is '1', the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz frame sync output signal can be inverted by setting the 8K_INV bit. The frame sync output can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL bit. When they are pulsed, the pulse width is defined by the period of OUT1; and they are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 8K_PUL_POSITION bit.

Table 25: Synchronization Control

SYNC_BYPASS	AUTO_EXT_SYNC_EN	EXT_SYNC_EN	Synchronization
0	don't-care	0	Disabled
	0	1	Enabled
	1	1	Disabled
1	don't-care		Enabled

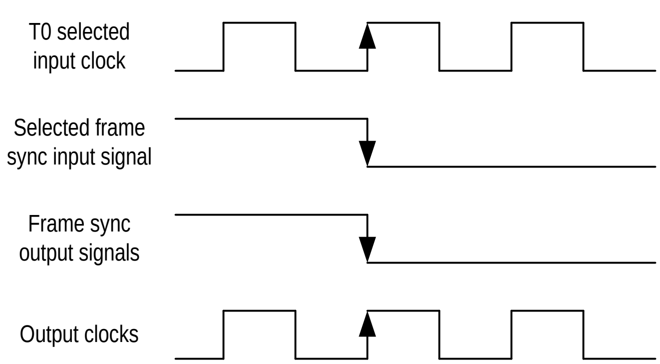


Figure 7. On Target Frame Sync Input Signal Timing

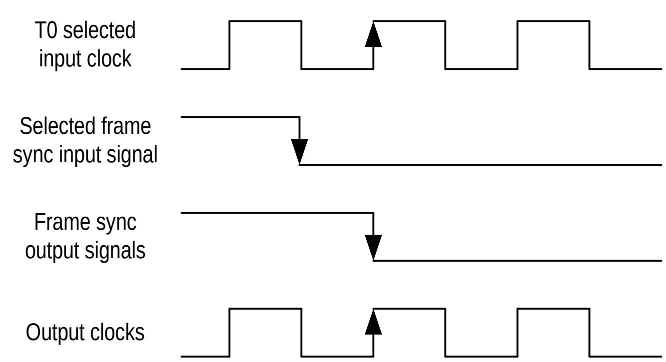


Figure 8. 0.5 UI Early Frame Sync Input Signal Timing

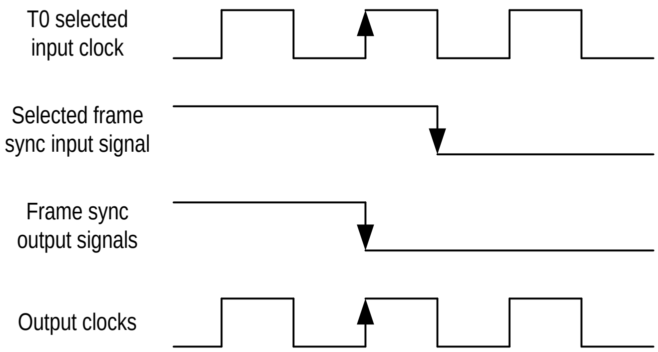


Figure 9. 0.5 UI Late Frame Sync Input Signal Timing

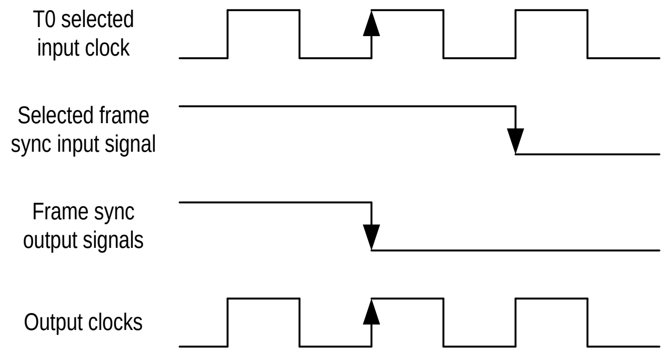


Figure 10. 1 UI Late Frame Sync Input Signal Timing

Table 26: Related Bit / Register in Chapter 3.13

Bit	Register	Address (Hex)
OUT1_PATH_SEL[3:0]	OUT1_FREQ_CNFG	6D
OUT1_DIVIDER[3:0]		
IN_SONET_SDH	INPUT_MODE_CNFG	09
AUTO_EXT_SYNC_EN		
EXT_SYNC_EN		
OUT1_INV	OUT1_INV_CNFG	73
8K_EN	FR_SYNC_CNFG	74
8K_INV		
8K_PUL		
8K_PUL_POSITION		
SYNC_BYPASS	SYNC_MONITOR_CNFG	7C
SYNC_MON_LIMT[2:0]		
SYNC_PHn[1:0] (n = 1 or 2)	SYNC_PHASE_CNFG	7D
EX_SYNC_ALARM_MON	OPERATING_STS	52
EX_SYNC_ALARM [1]	INTERRUPTS3_STS	0F
EX_SYNC_ALARM [2]	INTERRUPTS3_ENABLE_CNFG	12

3.14 INTERRUPT SUMMARY

The interrupt sources of the device are as follows:

- T0 Input clocks validity change
- T0 selected input clock fail
- T0 DPLL operating mode switch
- External sync alarm

All of the above interrupt events are indicated by the corresponding interrupt status bit. If the corresponding interrupt enable bit is set, any of the interrupts can be reported by the INT_REQ pin. The output characteristics on the INT_REQ pin are determined by the HZ_EN bit and the INT_POL bit.

Interrupt events are cleared by writing a '1' to the corresponding interrupt status bit. The INT_REQ pin will be inactive only when all the pending enabled interrupts are cleared.

In addition, the interrupt of T0 selected input clock fail can be reported by the TDO pin, as determined by the LOS_FLAG_TO_TDO bit.

Table 27: Related Bit / Register in Chapter 3.14

Bit	Register	Address (Hex)
HZ_EN	INTERRUPT_CNFG	0C
INT_POL		
LOS_FLAG_TO_TDO	MON_SW_PBO_CNFG	0B

3.15 T0 SUMMARY

The main features supported by the T0 path are as follows:

- Phase lock alarm;
- Forced or Automatic input clock selection/switch;
- 3 primary and 3 secondary, temporary DPLL operating modes, switched automatically or under external control;
- Automatic switch between starting, acquisition and locked bandwidths/damping factors;
- Programmable DPLL bandwidths from 1.2 Hz to 560 Hz in 8 steps;
- Programmable damping factors: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous, Automatic Slow Averaged, Automatic Fast Averaged or Manual holdover frequency offset acquiring;
- PBO to minimize output phase transients;
- Programmable output phase offset;
- Low jitter multiple clock outputs with programmable polarity;
- Low jitter 8 kHz frame sync signal output with programmable pulse width and polarity;

3.16 LINE CARD APPLICATION

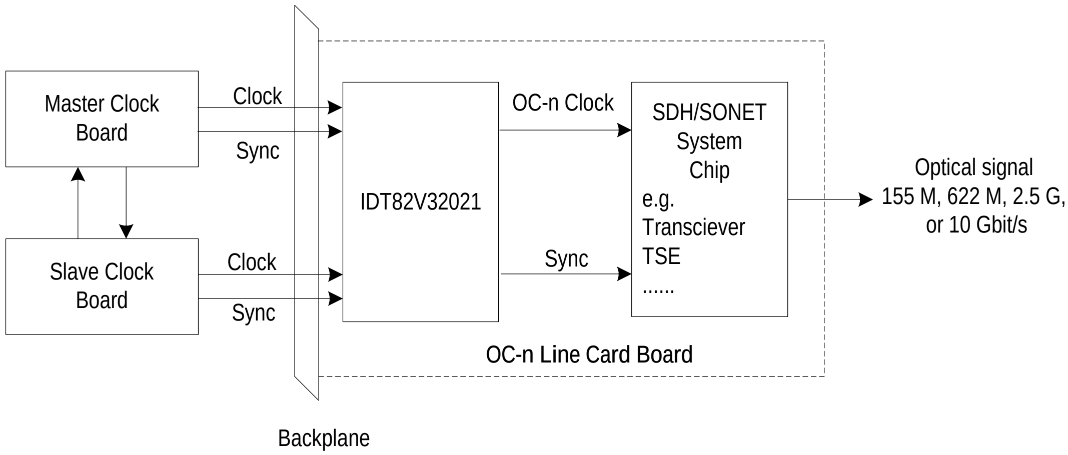


Figure 11. Line Card Application

4 I²C PROGRAMMING INTERFACE

The I²C bus interface provides access to read and write the registers in the IDT82V32021.

4.1 FUNCTION DESCRIPTION

The timing of a complete data transfer is shown in Figure 12.

The transfer process can be divided into three phases:

- START (S) or repeated START (Sr) condition;
- Byte data transfer condition;
- STOP (P) condition.

The definitions of S/Sr and P conditions are shown in Table 28:

Table 28: Definition of S/Sr and P Conditions

Condition	Definition
S/Sr	A high to low transition on the SDA pin while the SCL pin is high.
P	A low to high transition on the SDA pin while the SCL pin is high.

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted in theory. Each byte has to be followed by an acknowledge bit (ACK). So the whole data transfer needs a period of 9 clock cycles. The data is transferred with the most significant bit (MSB) first. The input SCL signal for the IDT82V32021 is from the master device.

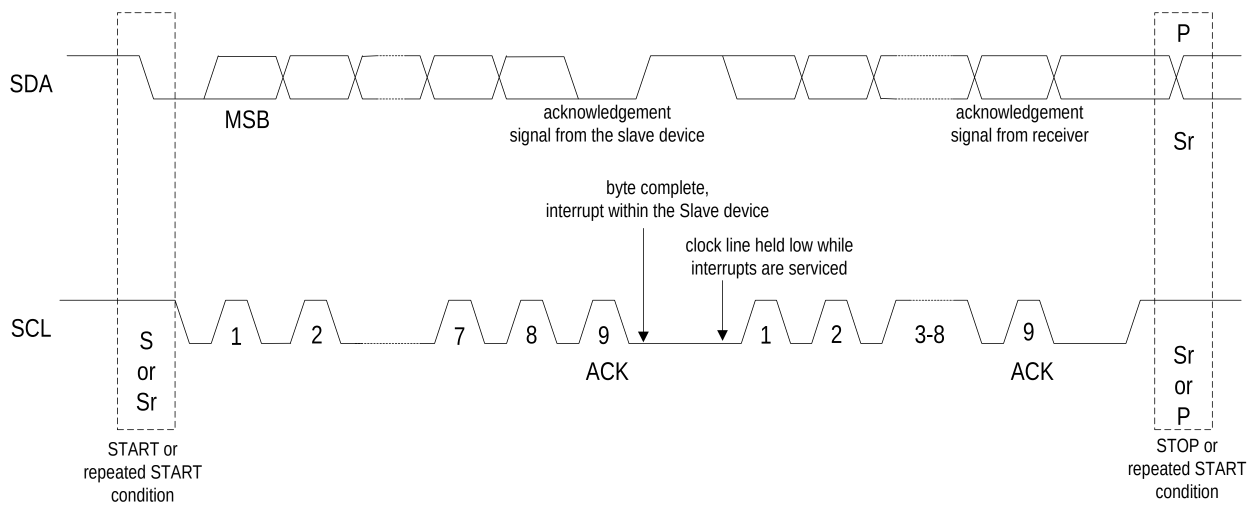


Figure 12. Data Transfer on the I²C-bus

4.1.1 DATA TRANSFER FORMAT

Two kinds of data transfer formats are supported by the IDT82V32021:

- Slave-receiver mode (Write);
- Slave-transmitter mode (Read);

4.1.1.1 Slave-receiver Mode (Write)

The Slave-receiver mode is as shown in Figure 13.

The Master device asserts the slave address followed by the Write bit. The Slave device acknowledges and the Master device delivers the address byte. The Slave device again acknowledges before the Master device sends the data byte. The Slave device acknowledges each byte, and the entire transaction is finished with a STOP condition.

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Address Byte	A	Data Byte	A	P

S Start Condition

Wr Write (bit value of 0)

P Stop Condition

A Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)

White box: Master-to-Slave

Grey box: Slave-to-Master

Figure 13. Slave-receiver Mode

4.1.1.2 Slave-transmitter Mode (Read)

The Slave-transmitter mode is as shown in Figure 14.

First the Master device must write an address byte to the slave device. Then it must follow that address byte with a repeated START condition to denote a read from that device's address. The Slave device then returns one byte data corresponding the address. Note that there is no STOP condition before the repeated STRAT condition, and that a no-acknowledge (NACK) signifies the end of the read transfer.

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Address Byte	A	S	Slave Address	Rd	A	Data Byte	A	P

S Start Condition

P Stop Condition

Rd Read (bit value of 1)

Wr Write (bit value of 0)

White box: Master-to-Slave

Grey box: Slave-to-Master

A Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)

Figure 14. Slave-transmitter Mode

4.1.2 ADDRESS ASSIGNMENT

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	0	AD2	AD1	AD0	1/0

Figure 15. Address Assignment

Each device is recognized by a unique slave address. The slave addressing procedure for the I^2C-bus is such that the first byte after the START condition usually determines which slave device will be selected by the Master device. In this specification, the 4 MSB bits of the address byte are fixed and the 3 LSB bits are decided by address input pins AD[2:0], as shown in Figure 15.

The R/$\overline{W}$ bit is used as a data transfer direction bit which is determined by the Master device. A '0' on this bit indicates a transmission (Write) to registers and a '1' indicates a request for data (Read) from the registers.

The device will acknowledge (ACK) the first byte which is received after the Start Condition even though it is other device's address. If the slave address of the device matches the address input pins AD[2:0], the device will process the normal read/write operation; otherwise the device will release the data line with the right pin address for other chip operation.

4.2 TIMING DEFINITION

The timing of I^2C-bus is as shown in Figure 16.

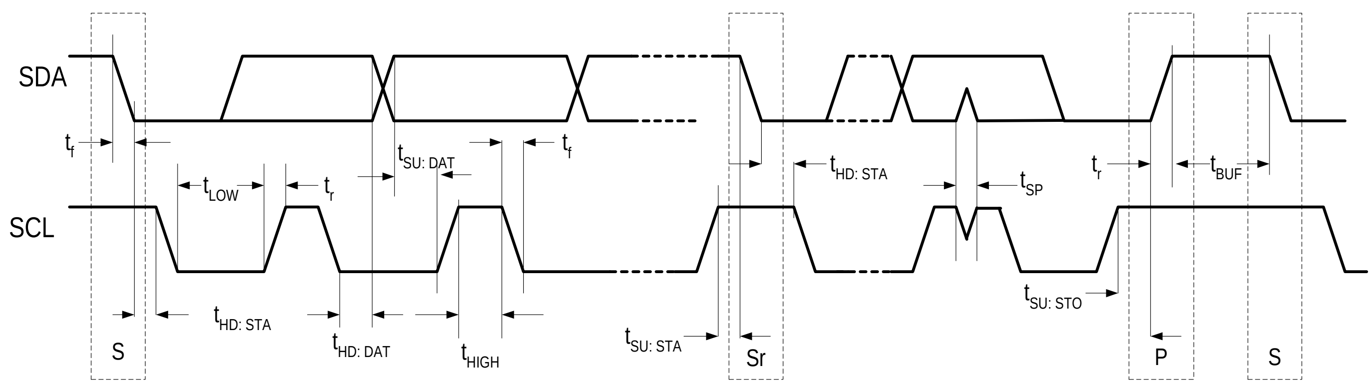


Figure 16. Timing Definition of I^2C-bus

Table 29: Timing Definition for Standard Mode and Fast Mode(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL	Serial clock frequency	0	100	0	400	KHz
$t_{HD; STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.5	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU; STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD; DAT}$	Data hold time: for CBUS compatible masters for I^2C-bus devices	5.0 0(2)	- 3.45(3)	- 0(2)	- 0.9(3)	µs
$t_{SU; DAT}$	Data set-up time	250	-	100(4)	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20 + 0.1Cb(5)	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	20 + 0.1Cb(5)	300	ns
$t_{SU; STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (Including hysteresis)	0.1VDD	-	0.1VDD	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (Including hysteresis)	0.2VDD	-	0.2VDD	-	V
t_{sp}	Pulse width of spikes which must be suppressed by the input filter	0	50	0	50	ns

Note:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 37)
2. A device must Internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD; DAT}$ has only to be met if the device does not strech the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU; DAT} \geqslant 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode device, faster fall-times according to Table 39 allowed.

n/a = not applicable

5 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The $\overline{TRST}$ pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in Figure 17.

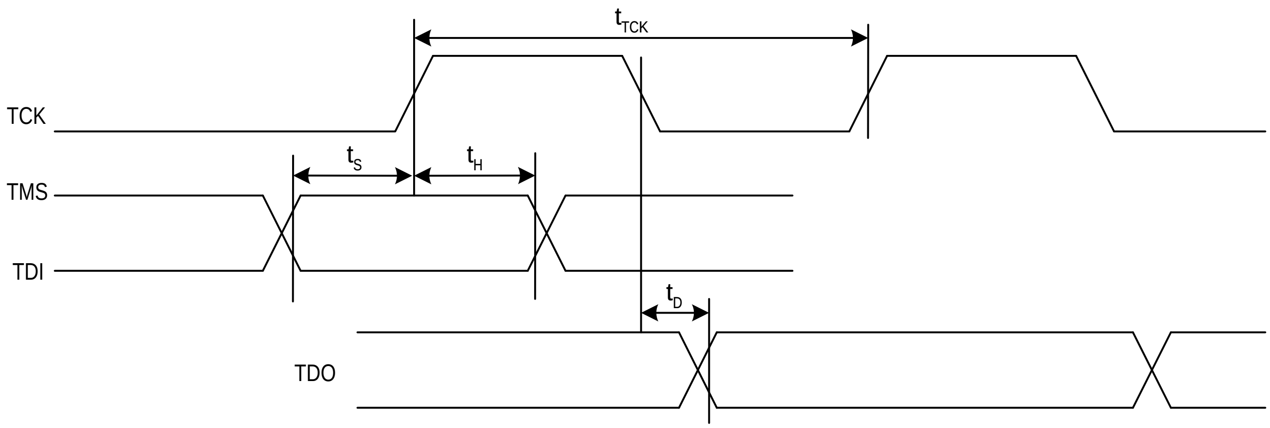


Figure 17. JTAG Interface Timing Diagram

Table 30: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_S	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

6 PROGRAMMING INFORMATION

After reset, all the registers are set to their default values. The registers are read or written via the microprocessor interface.

Before any write operation, the value in register PROTECTION_CNFG is recommended to be confirmed to make sure whether the write operation is enabled. The device provides 3 register protection modes:

- Protected mode: no other registers can be written except register PROTECTION_CNFG itself;
- Fully Unprotected mode: all the writable registers can be written;
- Single Unprotected mode: one more register can be written besides register PROTECTION_CNFG. After write operation (not including writing a ‘1’ to clear a bit to ‘0’), the device automatically switches to Protected mode.

Writing ‘0’ to the registers will take no effect if the registers are cleared by writing ‘1’.

The access of the Multi-word Registers is different from that of the Single-word Registers. Take the registers (04H, 05H and 06H) for an example, the write operation for the Multi-word Registers follows a fixed sequence. The register (04H) is configured first and the register (06H) is configured last. The three registers are configured continuously and should not be interrupted by any operation. The crystal calibration configuration will take effect after all the three registers are configured. During read operation, the register (04H) is read first and the register (06H) is read last. The crystal calibration reading should be continuous and not be interrupted by any operation.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved should not be written by the users. In addition, their value should be masked out from any testing or error detection methods that are implemented.

6.1 REGISTER MAP

Table 31 is the map of all the registers, sorted in an ascending order of their addresses.

Table 31: Register List and Map

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
Global Control Registers										
00	ID[7:0] - Device ID 1	ID[7:0]								P 49
01	ID[15:8] - Device ID 2	ID[15:8]								P 49
04	NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1	NOMINAL_FREQ_VALUE[7:0]								P 50
05	NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2	NOMINAL_FREQ_VALUE[15:8]								P 50
06	NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3	NOMINAL_FREQ_VALUE[23:16]								P 50
08	PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration	MULTI_FACTOR[1:0]		TIME_OUT_VALUE[5:0]						P 51
09	INPUT_MODE_CNFG - Input Mode Configuration	AUTO_EXT_SYNC_EN	EXT_SYNC_EN	PH_ALARM_TIMEOUT	SYNC_FREQ[1:0]		IN_SONET_SDH	-	REVERTIVE_MODE	P 52
0A	OSCI_CNFG - Master Clock Configuration	-	-	-	-	-	OSC_EDGE	-	-	P 53
0B	MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control	FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	PBO_FREZ	PBO_EN	-	FREQ_MON_HARD_EN	P 54
7E	PROTECTION_CNFG - Register Protection Mode Configuration	PROTECTION_DATA[7:0]								P 55
Interrupt Registers										
0C	INTERRUPT_CNFG - Interrupt Configuration	-	-	-	-	-	-	HZ_EN	INT_POL	P 56

Table 31: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
0D	INTERRUPTS1_STS - Interrupt Status 1	-	-	-	-	IN2_CMOS	IN1_CMOS	-	-	P 56
0E	INTERRUPTS2_STS - Interrupt Status 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	-	-	-	-	-	-	P 57
0F	INTERRUPTS3_STS - Interrupt Status 3	EX_SYNC_ALARM	-	-	-	-	-	-	-	P 57
10	INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1	-	-	-	-	IN2_CMOS	IN1_CMOS	-	-	P 58
11	INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	-	-	-	-	-	-	P 58
12	INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3	EX_SYNC_ALARM	-	-	-	-	-	-	-	P 59
Input Clock Frequency & Priority Configuration Registers										
16	IN1_CMOS_CNFG - CMOS Input Clock 1 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 60
17	IN2_CMOS_CNFG - CMOS Input Clock 2 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 61
23	PRE_DIV_CH_CNFG - DivN Divider Channel Selection	-	-	-	-	PRE_DIV_CH_VALUE[3:0]				P 62
24	PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1	PRE_DIVN_VALUE[7:0]								P 62
25	PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2	-	PRE_DIVN_VALUE[14:8]							P 63
27	IN1_IN2_CMOS_SEL_PRIORITY_CNFG - CMOS Input Clock 1 & 2 Priority Configuration	IN2_CMOS_SEL_PRIORITY[3:0]				IN1_CMOS_SEL_PRIORITY[3:0]				P 64
Input Clock Quality Monitoring Configuration & Status Registers										
2E	FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration	-	-	-	-	FREQ_MON_FACTOR[3:0]				P 65
2F	ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration	-	-	-	-	ALL_FREQ_HARD_THRESHOLD[3:0]				P 65
31	UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0	UPPER_THRESHOLD_0_DATA[7:0]								P 66
32	LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0	LOWER_THRESHOLD_0_DATA[7:0]								P 66
33	BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0	BUCKET_SIZE_0_DATA[7:0]								P 66
34	DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0	-	-	-	-	-	-	DECAY_RATE_0_DATA[1:0]		P 67
35	UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1	UPPER_THRESHOLD_1_DATA[7:0]								P 67

Table 31: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
36	LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1	LOWER_THRESHOLD_1_DATA[7:0]								P 67
37	BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1	BUCKET_SIZE_1_DATA[7:0]								P 68
38	DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1	-	-	-	-	-	-	DECAY_RATE_1_DATA[1:0]		P 68
39	UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2	UPPER_THRESHOLD_2_DATA[7:0]								P 68
3A	LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2	LOWER_THRESHOLD_2_DATA[7:0]								P 69
3B	BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2	BUCKET_SIZE_2_DATA[7:0]								P 69
3C	DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2	-	-	-	-	-	-	DECAY_RATE_2_DATA[1:0]		P 69
3D	UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3	UPPER_THRESHOLD_3_DATA[7:0]								P 70
3E	LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3	LOWER_THRESHOLD_3_DATA[7:0]								P 70
3F	BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3	BUCKET_SIZE_3_DATA[7:0]								P 70
40	DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3	-	-	-	-	-	-	DECAY_RATE_3_DATA[1:0]		P 71
41	IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection	-	-	-	-	IN_FREQ_READ_CH[3:0]				P 71
42	IN_FREQ_READ_STS - Input Clock Frequency Read Value	IN_FREQ_VALUE[7:0]								P 71
44	IN1_IN2_CMOS_STS - CMOS Input Clock 1 & 2 Status	-	IN2_CMOS_FREQ_HARD_ALARM	IN2_CMOS_NO_ACTIVITY_ALARM	IN2_CMOS_PH_LOCK_ALARM	-	IN1_CMOS_FREQ_HARD_ALARM	IN1_CMOS_NO_ACTIVITY_ALARM	IN1_CMOS_PH_LOCK_ALARM	P 72
T0 DPLL Input Clock Selection Registers										
4A	INPUT_VALID1_STS - Input Clocks Validity 1	-	-	-	-	IN2_CMOS	IN1_CMOS	-	-	P 73
4E	PRIORITY_TABLE1_STS - Priority Status 1	HIGHEST_PRIORITY_VALIDATED[3:0]				CURRENTLY_SELECTED_INPUT[3:0]				P 73
4F	PRIORITY_TABLE2_STS - Priority Status 2	-	-	-	-	SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]				P 74
50	T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration	-	-	-	-	T0_INPUT_SEL[3:0]				P 74
T0 DPLL State Machine Control Registers										
52	OPERATING_STS - DPLL Operating Status	EX_SYNC_ALARM_MON	-	T0_DPLL_SOFT_FREQ_ALARM	-	T0_DPLL_LOCK	T0_DPLL_OPERATING_MODE[2:0]			P 75

Table 31: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
53	T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration	-	-	-	-	-	T0_OPERATING_MODE[2:0]			P 76
T0 DPLL & T0 APLL Configuration Registers										
55	T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration	T0_APLL_PATH[3:0]				T0_GSM_OBSAI_16E1_16T1_SEL[1:0]		T0_12E1_24T1_E3_T3_SEL[1:0]		P 77
56	T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration	T0_DPLL_START_DAMPING[2:0]			T0_DPLL_START_BW[4:0]					P 78
57	T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration	T0_DPLL_ACQ_DAMPING[2:0]			T0_DPLL_ACQ_BW[4:0]					P 79
58	T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration	T0_DPLL_LOCKED_DAMPING[2:0]			T0_DPLL_LOCKED_BW[4:0]					P 80
59	T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration	AUTO_BW_SEL	-	-	-	T0_LIMT	-	-	-	P 80
5A	PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration	COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT[3:0]				P 81
5B	PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration	FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT[2:0]			P 82
5C	T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration	MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLDOVER_MODE[1:0]		-	-	P 83
5D	T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1	T0_HOLDOVER_FREQ[7:0]								P 83
5E	T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2	T0_HOLDOVER_FREQ[15:8]								P 84
5F	T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3	T0_HOLDOVER_FREQ[23:16]								P 84
62	CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1	CURRENT_DPLL_FREQ[7:0]								P 84
63	CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2	CURRENT_DPLL_FREQ[15:8]								P 85
64	CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3	CURRENT_DPLL_FREQ[23:16]								P 85
65	DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration	FREQ_LIMT_PH_LOS	DPLL_FREQ_SOFT_LIMT[6:0]							P 85
66	DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1	DPLL_FREQ_HARD_LIMT[7:0]								P 86
67	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2	DPLL_FREQ_HARD_LIMT[15:8]								P 86

Table 31: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
68	CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1	CURRENT_PH_DATA[7:0]								P 86
69	CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2	CURRENT_PH_DATA[15:8]								P 87
6A	T0_APLL_BW_CNFG - T0 APLL Bandwidth Configuration	-	-	T0_APLL_BW[1:0]		-	-	-	-	P 87
Output Configuration Registers										
6D	OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration	OUT1_PATH_SEL[3:0]				OUT1_DIVIDER[3:0]				P 88
73	OUT1_INV_CNFG - Output Clock 1 Invert Configuration	-	-	-	-	-	OUT1_INV	-	-	P 88
74	FR_SYNC_CNFG - Frame Sync Output Configuration	IN_2K_4K_8K_INV	8K_EN	-	8K_PUL_POSITION	8K_INV	8K_PUL	-	-	P 89
PBO & Phase Offset Control Registers										
78	PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration	IN_NOISE_WINDOW	-	PH_MON_EN	PH_MON_PBO_EN	PH_TR_MON_LIMT[3:0]				P 90
Synchronization Configuration Registers										
7C	SYNC_MONITOR_CNFG - Sync Monitor Configuration	SYNC_BYPASS	SYNC_MON_LIMT[2:0]			-	-	-	-	P 91
7D	SYNC_PHASE_CNFG - Sync Phase Configuration	-	-	-		SYNC_PH2[1:0]		SYNC_PH1[1:0]		P 91

6.2 REGISTER DESCRIPTION

6.2.1 GLOBAL CONTROL REGISTERS

ID[7:0] - Device ID 1

Address: 00H
Type: Read
Default Value: 10001000

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7 - 0	ID[7:0]	Refer to the description of the ID[15:8] bits (b7~0, 01H).

ID[15:8] - Device ID 2

Address: 01H Type: Read Default Value: 00010001							
7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit	Name	Description
7 - 0	ID[15:8]	The value in the ID[15:0] bits are pre-set, representing the identification number for the IDT82V32021.

NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1

Address: 04H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VALUE7	NOMINAL_-FREQ_VALUE6	NOMINAL_-FREQ_VALUE5	NOMINAL_-FREQ_VALUE4	NOMINAL_-FREQ_VALUE3	NOMINAL_-FREQ_VALUE2	NOMINAL_-FREQ_VALUE1	NOMINAL_-FREQ_VALUE0

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[7:0]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2

Address: 05H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VAL-UE15	NOMINAL_-FREQ_VAL-UE14	NOMINAL_-FREQ_VAL-UE13	NOMINAL_-FREQ_VAL-UE12	NOMINAL_-FREQ_VAL-UE11	NOMINAL_-FREQ_VAL-UE10	NOMINAL_-FREQ_VALUE9	NOMINAL_-FREQ_VALUE8

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[15:8]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3

Address: 06H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VAL-UE23	NOMINAL_-FREQ_VAL-UE22	NOMINAL_-FREQ_VAL-UE21	NOMINAL_-FREQ_VAL-UE20	NOMINAL_-FREQ_VAL-UE19	NOMINAL_-FREQ_VAL-UE18	NOMINAL_-FREQ_VAL-UE17	NOMINAL_-FREQ_VAL-UE16

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[23:16]	The NOMINAL_FREQ_VALUE[23:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.0000884, the calibration value for the master clock in ppm will be gotten. For example, the frequency offset on OSCI is +3 ppm. Though -3 ppm should be compensated, the calibration value is calculated as +3 ppm: 3 ÷ 0.0000884 = 33937 (Dec.) = 8490 (Hex); So '008490' should be written into these bits. The calibration range is within ±741 ppm.

PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration

Address: 08H
Type: Read / Write
Default Value: 00110010

7	6	5	4	3	2	1	0
MULTI_FAC-TOR1	MULTI_FAC-TOR0	TIME_OUT_VALUE5	TIME_OUT_VALUE4	TIME_OUT_VALUE3	TIME_OUT_VALUE2	TIME_OUT_VALUE1	TIME_OUT_VALUE0

Bit	Name	Description
7 - 6	MULTI_FACTOR[1:0]	These bits determine a factor which has a relationship with a period in seconds. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised). Refer to the description of the TIME_OUT_VALUE[5:0] bits (b5~0, 08H). 00: 2 (default) 01: 4 10: 8 11: 16
5 - 0	TIME_OUT_VALUE[5:0]	These bits represent an unsigned integer. If the value in these bits is multiplied by the value in the MULTI_FACTOR[1:0] bits (b7~6, 08H), a period in seconds will be gotten. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised).

INPUT_MODE_CNFG - Input Mode Configuration

Address: 09H
Type: Read / Write
Default Value: 10100X10

7	6	5	4	3	2	1	0
AUTO_EX-T_SYNC_EN	EXT_SYNC_EN	PH_ALARM_-TIMEOUT	SYNC_FREQ1	SYNC_FREQ0	IN_SON-ET_SDH	-	REVERTIVE_-MODE

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>AUTO_EXT_SYNC_EN</td><td>This bit is valid only when the SYNC_BYPASS bit (b7, 7CH) is ‘0’.
Refer to the description of the EXT_SYNC_EN bit (b6, 09H).</td></tr>
<tr><td>6</td><td>EXT_SYNC_EN</td><td>This bit is valid only when the SYNC_BYPASS bit (b7, 7CH) is ‘0’.
This bit, together with the AUTO_EXT_SYNC_EN bit (b7, 09H), determines whether the selected frame sync input signal is enabled to synchronize the frame sync output signals.
<table><tr><th>AUTO_EXT_SYNC_EN</th><th>EXT_SYNC_EN</th><th>Synchronization</th></tr><tr><td>don’t-care</td><td>0</td><td>Disabled (default)</td></tr><tr><td>0</td><td>1</td><td>Enabled</td></tr><tr><td>1</td><td>1</td><td>Disabled</td></tr></table></td></tr>
<tr><td>5</td><td>PH_ALARM_TIMEOUT</td><td>This bit determines how to clear the phase lock alarm.
0: The phase lock alarm will be cleared when a ‘1’ is written to the corresponding INn_CMOS_PH_LOCK_ALARM bit (n = 1 or 2) (b4/0, 44H).
1: The phase lock alarm will be cleared after a period (= TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second) which starts from when the alarm is raised. (default)</td></tr>
<tr><td>4 - 3</td><td>SYNC_FREQ[1:0]</td><td>These bits set the frequency of the frame sync signals input on the EX_SYNC1 ~ EX_SYNC2 pins.
00: 8 kHz (default)
01: 8 kHz.
10: 4 kHz.
11: 2 kHz.</td></tr>
<tr><td>2</td><td>IN_SONET_SDH</td><td>This bit selects the SDH or SONET network type.
0: SDH. The DPLL required clock is 2.048 MHz when the IN_FREQ[3:0] bits (b3~0, 16H, 17H) are ‘0001’ and the T0 DPLL output from the 16E1/16T1 path is 16E1.
1: SONET. The DPLL required clock is 1.544 MHz when the IN_FREQ[3:0] bits (b3~0, 16H, 17H) are ‘0001’ and the T0 DPLL output from the 16E1/16T1 path is 16T1.
The default value of this bit is determined by the SONET/$\overline{SDH}$ pin during reset.</td></tr>
<tr><td>1</td><td>-</td><td>Reserved.</td></tr>
<tr><td>0</td><td>REVERTIVE_MODE</td><td>This bit selects Revertive or Non-Revertive switch.
0: Non-Revertive switch. (default)
1: Revertive switch.</td></tr>
</table>

OSCI_CNFG - Master Clock Configuration

Address: 0AH Type: Read / Write Default Value: XXXXX00X							
7	6	5	4	3	2	1	0
-	-	-	-	-	OSC_EDGE	-	-

Bit	Name	Description
7 - 3	-	Reserved.
2	OSC_EDGE	This bit selects a better active edge of the master clock. 0: The rising edge. (default) 1: The falling edge.
1 - 0	-	Reserved

MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control

Address: 0BH
Type: Read / Write
Default Value: 100X01X1

7	6	5	4	3	2	1	0
FREQ_MON_-CLK	LOS_-FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	PBO_FREZ	PBO_EN	-	FRE-Q_MON_HARD_EN

Bit	Name	Description
7	FREQ_MON_CLK	The bit selects a reference clock for input clock frequency monitoring. 0: The output of T0 DPLL. 1: The master clock. (default)
6	LOS_FLAG_TO_TDO	The bit determines whether the interrupt of T0 selected input clock fail - is reported by the TDO pin. 0: Not reported. TDO pin is used as JTAG test data output which complies with IEEE 1149.1. (default) 1: Reported. TDO pin mimics the state of the T0_MAIN_REF_FAILED bit (b6, 0EH) and does not strictly comply with IEEE 1149.1.
5	ULTR_FAST_SW	This bit determines whether the T0 selected input clock is valid when missing 2 consecutive clock cycles or more. 0: Valid. (default) 1: Invalid.
4	EXT_SW	This bit determines the T0 input clock selection. 0: Forced selection or Automatic selection, as controlled by the T0_INPUT_SEL[3:0] bits (b3~0, 50H). 1: External Fast selection. The default value of this bit is determined by the FF_SRCSW pin during reset.
3	PBO_FREZ	This bit is valid only when the PBO is enabled by the PBO_EN bit (b2, 0BH). It determines whether PBO is frozen at the current phase offset when a PBO event is triggered. 0: Not frozen. (default) 1: Frozen. Further PBO events are ignored and the current phase offset is maintained.
2	PBO_EN	This bit determines whether PBO is enabled when the T0 selected input clock switch or the T0 DPLL exiting from Holdover mode or Free-Run mode occurs. 0: Disabled. 1: Enabled. (default)
1	-	Reserved.
0	FREQ_MON_HARD_EN	This bit determines whether the frequency hard alarm is enabled when the frequency of the input clock with respect to the reference clock is above the frequency hard alarm threshold. The reference clock can be the output of T0 DPLL or the master clock, as determined by the FREQ_MON_CLK bit (b7, 0BH). 0: Disabled. 1: Enabled. (default)

PROTECTION_CNFG - Register Protection Mode Configuration

Address: 7EH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
PROTECTION_DATA7	PROTECTION_DATA6	PROTECTION_DATA5	PROTECTION_DATA4	PROTECTION_DATA3	PROTECTION_DATA2	PROTECTION_DATA1	PROTECTION_DATA0

Bit	Name	Description
7 - 0	PROTECTION_DATA[7:0]	These bits select a register write protection mode. 00000000 - 10000100, 10000111 - 11111111: Protected mode. No other registers can be written except this register. 10000101: Fully Unprotected mode. All the writable registers can be written. (default) 10000110: Single Unprotected mode. One more register can be written besides this register. After write operation (not including writing a ‘1’ to clear the bit to ‘0’), the device automatically switches to Protected mode.

6.2.2 INTERRUPT REGISTERS

INTERRUPT_CNFG - Interrupt Configuration

Address: 0CH
Type: Read / Write
Default Value: XXXXXX10

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HZ_EN	INT_POL

Bit	Name	Description
7 - 2	-	Reserved.
1	HZ_EN	This bit determines the output characteristics of the INT_REQ pin. 0: The output on the INT_REQ pin is high/low when the interrupt is active; the output is the opposite when the interrupt is inactive. 1: The output on the INT_REQ pin is high/low when the interrupt is active; the output is in high impedance state when the interrupt is inactive. (default)
0	INT_POL	This bit determines the active level on the INT_REQ pin for an active interrupt indication. 0: Active low. (default) 1: Active high.

INTERRUPTS1_STS - Interrupt Status 1

Address: 0DH
Type: Read / Write
Default Value: XXXX11XX

7	6	5	4	3	2	1	0
-	-	-	-	IN2_CMOS	IN1_CMOS	-	-

Bit	Name	Description
7 - 4	-	Reserved.
3 - 2	INn_CMOS	This bit indicates the validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’) for the corresponding INn_CMOS; i.e., whether there is a transition (from ‘0’ to ‘1’ or from ‘1’ to ‘0’) on the corresponding INn_CMOS bit (b3/2, 4AH). Here n is 2 or 1. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a ‘1’.
1 - 0	-	Reserved.

INTERRUPTS2_STS - Interrupt Status 2

Address: 0EH
Type: Read / Write
Default Value: 00XXXXXX

7	6	5	4	3	2	1	0
T0_OPERAT-ING_MODE	T0_MAIN_REF_-FAILED	-	-	-	-	-	-

Bit	Name	Description
7	T0_OPERATING_MODE	This bit indicates the operating mode switch for T0 DPLL; i.e., whether the value in the T0_DPLL_OPERATING_-MODE[2:0] bits (b2~0, 52H) changes. 0: Has not switched. (default) 1: Has switched. This bit is cleared by writing a ‘1’.
6	T0_MAIN_REF_FAILED	This bit indicates whether the T0 selected input clock has failed. The T0 selected input clock fails when its validity changes from ‘valid’ to ‘invalid’; i.e., when there is a transition from ‘1’ to ‘0’ on the corresponding INn_CMOS bit (4AH). 0: Has not failed. (default) 1: Has failed. This bit is cleared by writing a ‘1’.
5 - 0	-	Reserved.

INTERRUPTS3_STS - Interrupt Status 3

Address: 0FH
Type: Read / Write
Default Value: 1XXXXXXX

7	6	5	4	3	2	1	0
EX_SYNC_ALARM	-	-	-	-	-	-	-

Bit	Name	Description
7	EX_SYNC_ALARM	This bit indicates whether an external sync alarm is raised; i.e., whether there is a transition from ‘0’ to ‘1’ on the EX_SYN-C_ALARM_MON bit (b7, 52H). 0: Has not occurred. 1: Has occurred. (default) This bit is cleared by writing a ‘1’.
6 - 0	-	Reserved.

INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1

Address: 10H
Type: Read / Write
Default Value: XXXX00XX

7	6	5	4	3	2	1	0
-	-	-	-	IN2_CMOS	IN1_CMOS	-	-

Bit	Name	Description
7 - 4	-	Reserved.
3 - 2	INn_CMOS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’), i.e., when the corresponding INn_CMOS bit (b3/2, 0DH) is ‘1’. Here n is 2 or 1. 0: Disabled. (default) 1: Enabled.
1 - 0	-	Reserved.

INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2

Address: 11H
Type: Read / Write
Default Value: 00XXXXXX

7	6	5	4	3	2	1	0
T0_OPERAT-ING_MODE	T0_MAIN_REF_-FAILED	-	-	-	-	-	-

Bit	Name	Description
7	T0_OPERATING_MODE	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 DPLL operating mode switches, i.e., when the T0_OPERATING_MODE bit (b7, 0EH) is ‘1’. 0: Disabled. (default) 1: Enabled.
6	T0_MAIN_REF_FAILED	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 selected input clock has failed; i.e., when the T0_MAIN_REF_FAILED bit (b6, 0EH) is ‘1’. 0: Disabled. (default) 1: Enabled.
5 - 0	-	Reserved.

INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3

Address: 12H Type: Read / Write Default Value: 0XXXXXXX							
7	6	5	4	3	2	1	0
EX_SYNC_ALARM	-	-	-	-	-	-	-

Bit	Name	Description
7	EX_SYNC_ALARM	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when an external sync alarm has occurred, i.e., when the EX_SYNC_ALARM bit (b7, 0FH) is ‘1’. 0: Disabled. (default) 1: Enabled.
6 - 0	-	Reserved.

6.2.3 INPUT CLOCK FREQUENCY & PRIORITY CONFIGURATION REGISTERS

IN1_CMOS_CNFG - CMOS Input Clock 1 Configuration

Address: 16H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 16H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 16H), determines whether the DivN Divider or the Lock 8k Divider is used for IN1_CMOS: DIRECT_DIV bit / LOCK_8K bit / Used Divider: 0 / 0 / Both bypassed (default) 0 / 1 / Lock 8k Divider 1 / 0 / DivN Divider 1 / 1 / Reserved
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN1_CMOS: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN1_CMOS: 0000: 8 kHz. (default) 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN1_CMOS, the required frequency should not be set higher than that of the input clock.

IN2_CMOS_CNFG - CMOS Input Clock 2 Configuration

Address: 17H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 17H).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 17H), determines whether the DivN Divider or the Lock 8k Divider is used for IN2_CMOS:
<table><tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr><tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr><tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr><tr><td>1</td><td>0</td><td>DivN Divider</td></tr><tr><td>1</td><td>1</td><td>Reserved</td></tr></table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN2_CMOS:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN2_CMOS:
0000: 8 kHz. (default)
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz.
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For the IN2_CMOS, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

PRE_DIV_CH_CNFG - DivN Divider Channel Selection

Address: 23H Type: Read / Write Default Value: XXXX0000							
7	6	5	4	3	2	1	0
-	-	-	-	PRE_DIV_CH_VALUE3	PRE_DIV_CH_VALUE2	PRE_DIV_CH_VALUE1	PRE_DIV_CH_VALUE0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	PRE_DIV_CH_VALUE[3:0]	This register is an indirect address register for Register 24H and 25H. These bits select an input clock. The value set in the PRE_DIVN_VALUE[14:0] bits (25H, 24H) is available for the selected input clock. 0000: Reserved. (default) 0001, 0010: Reserved. 0011: IN1_CMOS. 0100: IN2_CMOS. 0101 ~ 1111: Reserved.

PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1

Address: 24H Type: Read / Write Default Value: 00000000							
7	6	5	4	3	2	1	0
PRE_DIVN_VALUE7	PRE_DIVN_VALUE6	PRE_DIVN_VALUE5	PRE_DIVN_VALUE4	PRE_DIVN_VALUE3	PRE_DIVN_VALUE2	PRE_DIVN_VALUE1	PRE_DIVN_VALUE0

Bit	Name	Description
7 - 0	PRE_DIVN_VALUE[7:0]	Refer to the description of the PRE_DIVN_VALUE[14:8] bits (b6~0, 25H).

PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2

Address: 25H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	PRE_DIVN_VALUE14	PRE_DIVN_VALUE13	PRE_DIVN_VALUE12	PRE_DIVN_VALUE11	PRE_DIVN_VALUE10	PRE_DIVN_VALUE9	PRE_DIVN_VALUE8

Bit	Name	Description
7	-	Reserved.
6 - 0	PRE_DIVN_VALUE[14:8]	If the value in the PRE_DIVN_VALUE[14:0] bits is plus 1, the division factor for an input clock will be gotten. The input clock is selected by the PRE_DIV_CH_VALUE[3:0] bits (b3~0, 23H). A value from ‘0’ to ‘4BEF’ (Hex) can be written into, corresponding to a division factor from 1 to 19440. The others are reserved. So the DivN Divider only supports an input clock whose frequency is lower than (<) 155.52 MHz. The division factor setting should observe the following order: 1. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits; 2. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

IN1_IN2_CMOS_SEL_PRIORITY_CNFG - CMOS Input Clock 1 & 2 Priority Configuration

Address: 27H
Type: Read / Write
Default Value: 00110010

7	6	5	4	3	2	1	0
IN2_CMOS_SEL_PRIORITY3	IN2_CMOS_SEL_PRIORITY2	IN2_CMOS_SEL_PRIORITY1	IN2_CMOS_SEL_PRIORITY0	IN1_CMOS_SEL_PRIORITY3	IN1_CMOS_SEL_PRIORITY2	IN1_CMOS_SEL_PRIORITY1	IN1_CMOS_SEL_PRIORITY0

Bit	Name	Description
7 - 4	IN2_CMOS_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding IN2_CMOS. 0000: Disable IN2_CMOS for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. (default) 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	IN1_CMOS_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding IN1_CMOS. 0000: Disable IN1_CMOS for automatic selection. 0001: Priority 1. 0010: Priority 2. (default) 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

6.2.4 INPUT CLOCK QUALITY MONITORING CONFIGURATION & STATUS REGISTERS

FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration

Address: 2EH
Type: Read / Write
Default Value: XXXX1011

7	6	5	4	3	2	1	0
-	-	-	-	FREQ_MON_-FACTOR3	FREQ_MON_-FACTOR2	FREQ_MON_-FACTOR1	FREQ_MON_-FACTOR0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	FREQ_MON_FACTOR[3:0]	These bits determine a factor. The factor has a relationship with the frequency hard alarm threshold in ppm (refer to the description of the ALL_FREQ_HARD_THRESHOLD[3:0] bits (b3~0, 2FH)) and with the frequency of the input clock with respect to the master clock in ppm (refer to the description of the IN_FREQ_VALUE[7:0] bits (b7~0, 42H)). The factor represents the accuracy of the frequency monitor and should be set according to the requirements of different applications. 0000: 0.0032. 0001: 0.0064. 0010: 0.0127. 0011: 0.0257. 0100: 0.0514. 0101: 0.103. 0110: 0.206. 0111: 0.412. 1000: 0.823. 1001: 1.646. 1010: 3.292. 1011: 3.81. (default) 1100 - 1111: 4.6.

ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration

Address: 2FH
Type: Read / Write
Default Value: XXXX0011

7	6	5	4	3	2	1	0
-	-	-	-	ALL_FRE-Q_HARD_-THRESHOLD3	ALL_FRE-Q_HARD_-THRESHOLD2	ALL_FRE-Q_HARD_-THRESHOLD1	ALL_FRE-Q_HARD_-THRESHOLD0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	ALL_FREQ_HARD_THRESHOLD[3:0]	These bits represent an unsigned integer. The frequency hard alarm threshold in ppm can be calculated as follows: *Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.

UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0

Address: 31H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_0_DATA7	UPPER_-THRESH-OLD_0_DATA6	UPPER_-THRESH-OLD_0_DATA5	UPPER_-THRESH-OLD_0_DATA4	UPPER_-THRESH-OLD_0_DATA3	UPPER_-THRESH-OLD_0_DATA2	UPPER_-THRESH-OLD_0_DATA1	UPPER_-THRESH-OLD_0_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_0_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0

Address: 32H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_0_DATA7	LOWER_-THRESH-OLD_0_DATA6	LOWER_-THRESH-OLD_0_DATA5	LOWER_-THRESH-OLD_0_DATA4	LOWER_-THRESH-OLD_0_DATA3	LOWER_-THRESH-OLD_0_DATA2	LOWER_-THRESH-OLD_0_DATA1	LOWER_-THRESH-OLD_0_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_0_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0

Address: 33H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_0_DATA7	BUCKET_-SIZE_0_DATA6	BUCKET_-SIZE_0_DATA5	BUCKET_-SIZE_0_DATA4	BUCKET_-SIZE_0_DATA3	BUCKET_-SIZE_0_DATA2	BUCKET_-SIZE_0_DATA1	BUCKET_-SIZE_0_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_0_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0

Address: 34H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_0_DATA1	DECAY_RATE_0_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_0_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1

Address: 35H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_1_DATA7	UPPER_-THRESH-OLD_1_DATA6	UPPER_-THRESH-OLD_1_DATA5	UPPER_-THRESH-OLD_1_DATA4	UPPER_-THRESH-OLD_1_DATA3	UPPER_-THRESH-OLD_1_DATA2	UPPER_-THRESH-OLD_1_DATA1	UPPER_-THRESH-OLD_1_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_1_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1

Address: 36H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_1_DATA7	LOWER_-THRESH-OLD_1_DATA6	LOWER_-THRESH-OLD_1_DATA5	LOWER_-THRESH-OLD_1_DATA4	LOWER_-THRESH-OLD_1_DATA3	LOWER_-THRESH-OLD_1_DATA2	LOWER_-THRESH-OLD_1_DATA1	LOWER_-THRESH-OLD_1_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_1_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1

Address: 37H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_1_DATA7	BUCKET_-SIZE_1_DATA6	BUCKET_-SIZE_1_DATA5	BUCKET_-SIZE_1_DATA4	BUCKET_-SIZE_1_DATA3	BUCKET_-SIZE_1_DATA2	BUCKET_-SIZE_1_DATA1	BUCKET_-SIZE_1_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_1_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1

Address: 38H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_1_DATA1	DECAY_RATE_1_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_1_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2

Address: 39H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_2_DATA7	UPPER_-THRESH-OLD_2_DATA6	UPPER_-THRESH-OLD_2_DATA5	UPPER_-THRESH-OLD_2_DATA4	UPPER_-THRESH-OLD_2_DATA3	UPPER_-THRESH-OLD_2_DATA2	UPPER_-THRESH-OLD_2_DATA1	UPPER_-THRESH-OLD_2_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_2_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2

Address: 3AH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_2_DATA7	LOWER_-THRESH-OLD_2_DATA6	LOWER_-THRESH-OLD_2_DATA5	LOWER_-THRESH-OLD_2_DATA4	LOWER_-THRESH-OLD_2_DATA3	LOWER_-THRESH-OLD_2_DATA2	LOWER_-THRESH-OLD_2_DATA1	LOWER_-THRESH-OLD_2_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_2_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2

Address: 3BH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_2_DATA7	BUCKET_-SIZE_2_DATA6	BUCKET_-SIZE_2_DATA5	BUCKET_-SIZE_2_DATA4	BUCKET_-SIZE_2_DATA3	BUCKET_-SIZE_2_DATA2	BUCKET_-SIZE_2_DATA1	BUCKET_-SIZE_2_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_2_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2

Address: 3CH
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_2_DATA1	DECAY_RATE_2_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_2_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3

Address: 3DH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_3_DATA7	UPPER_-THRESH-OLD_3_DATA6	UPPER_-THRESH-OLD_3_DATA5	UPPER_-THRESH-OLD_3_DATA4	UPPER_-THRESH-OLD_3_DATA3	UPPER_-THRESH-OLD_3_DATA2	UPPER_-THRESH-OLD_3_DATA1	UPPER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_3_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3

Address: 3EH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_3_DATA7	LOWER_-THRESH-OLD_3_DATA6	LOWER_-THRESH-OLD_3_DATA5	LOWER_-THRESH-OLD_3_DATA4	LOWER_-THRESH-OLD_3_DATA3	LOWER_-THRESH-OLD_3_DATA2	LOWER_-THRESH-OLD_3_DATA1	LOWER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_3_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3

Address: 3FH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_3_DATA7	BUCKET_-SIZE_3_DATA6	BUCKET_-SIZE_3_DATA5	BUCKET_-SIZE_3_DATA4	BUCKET_-SIZE_3_DATA3	BUCKET_-SIZE_3_DATA2	BUCKET_-SIZE_3_DATA1	BUCKET_-SIZE_3_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_3_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3

Address: 40H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_3_DATA1	DECAY_RATE_3_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_3_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection

Address: 41H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	IN_FREQ_READ_CH3	IN_FREQ_READ_CH2	IN_FREQ_READ_CH1	IN_FREQ_READ_CH0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	IN_FREQ_READ_CH[3:0]	These bits select an input clock, the frequency of which with respect to the reference clock can be read. 0000: Reserved. (default) 0001, 0010: Reserved. 0011: IN1_CMOS. 0100: IN2_CMOS. 0101 ~ 1111: Reserved.

IN_FREQ_READ_STS - Input Clock Frequency Read Value

Address: 42H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
IN_FREQ_VALUE7	IN_FREQ_VALUE6	IN_FREQ_VALUE5	IN_FREQ_VALUE4	IN_FREQ_VALUE3	IN_FREQ_VALUE2	IN_FREQ_VALUE1	IN_FREQ_VALUE0

Bit	Name	Description
7 - 0	IN_FREQ_VALUE[7:0]	These bits represent a 2's complement signed integer. If the value is multiplied by the value in the FREQ_MON_FACTOR[3:0] bits (b3~0, 2EH), the frequency of an input clock with respect to the reference clock in ppm will be gotten. The input clock is selected by the IN_FREQ_READ_CH[3:0] bits (b3~0, 41H). The value in these bits is updated every 16 seconds, starting when an input clock is selected.

IN1_IN2_CMOS_STS - CMOS Input Clock 1 & 2 Status

Address: 44H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN2_CMOS_FREQ_HARD_ALARM	IN2_CMOS_NO_ACTIVITY_ALARM	IN2_CMOS_PH_LOCK_ALARM	-	IN1_CMOS_FREQ_HARD_ALARM	IN1_CMOS_NO_ACTIVITY_ALARM	IN1_CMOS_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN2_CMOS_FREQ_HARD_ALARM	This bit indicates whether IN2_CMOS is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN2_CMOS_NO_ACTIVITY_ALARM	This bit indicates whether IN2_CMOS is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN2_CMOS_PH_LOCK_ALARM	This bit indicates whether IN2_CMOS is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN1_CMOS_FREQ_HARD_ALARM	This bit indicates whether IN1_CMOS is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN1_CMOS_NO_ACTIVITY_ALARM	This bit indicates whether IN1_CMOS is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN1_CMOS_PH_LOCK_ALARM	This bit indicates whether IN1_CMOS is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

6.2.5 T0 DPLL INPUT CLOCK SELECTION REGISTERS

INPUT_VALID1_STS - Input Clocks Validity 1

Address: 4AH
Type: Read
Default Value: XXXX00XX

7	6	5	4	3	2	1	0
-	-	-	-	IN2_CMOS	IN1_CMOS	-	-

Bit	Name	Description
7 - 4	-	Reserved.
3 - 2	INn_CMOS	This bit indicates the validity of the corresponding INn_CMOS. Here n is 2 or 1. 0: Invalid. (default) 1: Valid.
1 - 0	-	Reserved.

PRIORITY_TABLE1_STS - Priority Status 1

Address: 4EH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
HIGHEST_PRIORITY_VALIDATED3	HIGHEST_PRIORITY_VALIDATED2	HIGHEST_PRIORITY_VALIDATED1	HIGHEST_PRIORITY_VALIDATED0	CURRENTLY_SELECTED_INPUT3	CURRENTLY_SELECTED_INPUT2	CURRENTLY_SELECTED_INPUT1	CURRENTLY_SELECTED_INPUT0

Bit	Name	Description
7 - 4	HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the highest priority. 0000: No input clock is qualified. (default) 0001, 0010: Reserved. 0011: IN1_CMOS. 0100: IN2_CMOS. 0101 ~ 1111: Reserved.
3 - 0	CURRENTLY_SELECTED_INPUT[3:0]	These bits indicate the T0 selected input clock. 0000: No input clock is selected. (default) 0001, 0010: Reserved. 0011: IN1_CMOS. 0100: IN2_CMOS. 0101 ~ 1111: Reserved.

PRIORITY_TABLE2_STS - Priority Status 2

Address: 4FH Type: Read Default Value: XXXX0000							
7	6	5	4	3	2	1	0
-	-	-	-	SECOND_HIGHEST_PRIORITY_VALIDATED3	SECOND_HIGHEST_PRIORITY_VALIDATED2	SECOND_HIGHEST_PRIORITY_VALIDATED1	SECOND_HIGHEST_PRIORITY_VALIDATED0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the second highest priority. 0000: No input clock is qualified. (default) 0001, 0010: Reserved. 0011: IN1_CMOS. 0100: IN2_CMOS. 0101 ~ 1111: Reserved.

T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration

Address: 50H Type: Read / Write Default Value: XXXX0000							
7	6	5	4	3	2	1	0
-	-	-	-	T0_INPUT_SEL3	T0_INPUT_SEL2	T0_INPUT_SEL1	T0_INPUT_SEL0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	T0_INPUT_SEL[3:0]	This bit determines T0 input clock selection. It is valid only when the EXT_SW bit (b4, 0BH) is ‘0’. 0000: Automatic selection. (default) 0001, 0010: Reserved. 0011: Forced selection - IN1_CMOS is selected. 0100: Forced selection - IN2_CMOS is selected. 0101 ~ 1111: Reserved.

6.2.6 T0 DPLL STATE MACHINE CONTROL REGISTERS

OPERATING_STS - DPLL Operating Status

Address: 52H
Type: Read
Default Value: 1X0X0001

7	6	5	4	3	2	1	0
EX_SYNC_ALARM_MON	-	T0_DPLL_SOFT_FREQ_ALARM	-	T0_DPLL_LOCK	T0_DPLL_OPERATING_MODE2	T0_DPLL_OPERATING_MODE1	T0_DPLL_OPERATING_MODE0

Bit	Name	Description
7	EX_SYNC_ALARM_MON	This bit indicates whether the selected frame sync input signal is in external sync alarm status. 0: No external sync alarm. 1: In external sync alarm status. (default)
6	-	Reserved.
5	T0_DPLL_SOFT_FREQ_ALARM	This bit indicates whether the T0 DPLL is in soft alarm status. 0: No T0 DPLL soft alarm. (default) 1: In T0 DPLL soft alarm status.
4	-	Reserved.
3	T0_DPLL_LOCK	This bit indicates the T0 DPLL locking status. 0: Unlocked. (default) 1: Locked.
2 - 0	T0_DPLL_OPERATING_MODE[2:0]	These bits indicate the current operating mode of T0 DPLL. 000: Reserved. 001: Free-Run. (default) 010: Holdover. 011: Reserved. 100: Locked. 101: Pre-Locked2. 110: Pre-Locked. 111: Lost-Phase.

T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration

Address: 53H
Type: Read / Write
Default Value: XXXXX000

7	6	5	4	3	2	1	0
-	-	-	-	-	T0_OPERATING_MODE2	T0_OPERATING_MODE1	T0_OPERATING_MODE0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	T0_OPERATING_MODE[2:0]	These bits control the T0 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101: Forced - Pre-Locked2. 110: Forced - Pre-Locked. 111: Forced - Lost-Phase.

6.2.7 T0 DPLL & T0 APLL CONFIGURATION REGISTERS

T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration

Address: 55H
Type: Read / Write
Default Value: 00000X0X

7	6	5	4	3	2	1	0
T0_APLL_-PATH3	T0_APLL_-PATH2	T0_APLL_-PATH1	T0_APLL_-PATH0	T0_GSM_OBSA-I_16E1_16T1_-SEL1	T0_GSM_OBSA-I_16E1_16T1_-SEL0	T0_12E1_24T1_E3_T3_SEL1	T0_12E1_24T1_E3_T3_SEL0

Bit	Name	Description
7 - 4	T0_APLL_PATH[3:0]	These bits select an input to the T0 APLL. 0000: The output of T0 DPLL 77.76 MHz path. (default) 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100 ~ 1111: Reserved.
3 - 2	T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	These bits select an output clock from the T0 DPLL GSM/OBSAI/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: OBSAI. The default value of the T0_GSM_OBSAI_16E1_16T1_SEL0 bit is determined by the SONET/$\overline{SDH}$ pin during reset.
1 - 0	T0_12E1_24T1_E3_T3_SEL[1:0]	These bits select an output clock from the T0 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T0_12E1_24T1_E3_T3_SEL0 bit is determined by the SONET/$\overline{SDH}$ pin during reset.

T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration

Address: 56H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
T0_DPLL_START_DAMPING2	T0_DPLL_START_DAMPING1	T0_DPLL_START_DAMPING0	T0_DPLL_START_BW4	T0_DPLL_START_BW3	T0_DPLL_START_BW2	T0_DPLL_START_BW1	T0_DPLL_START_BW0

Bit	Name	Description
7 - 5	T0_DPLL_START_DAMPING[2:0]	These bits set the starting damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_START_BW[4:0]	These bits set the starting bandwidth for T0 DPLL. 00XXX: Reserved. 01000 ~ 01010 : Reserved. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration

Address: 57H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
T0_DPLL_ACQ_DAMPING2	T0_DPLL_ACQ_DAMPING1	T0_DPLL_ACQ_DAMPING0	T0_DPLL_ACQ_BW4	T0_DPLL_ACQ_BW3	T0_DPLL_ACQ_BW2	T0_DPLL_ACQ_BW1	T0_DPLL_ACQ_BW0

Bit	Name	Description
7 - 5	T0_DPLL_ACQ_DAMPING[2:0]	These bits set the acquisition damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_ACQ_BW[4:0]	These bits set the acquisition bandwidth for T0 DPLL. 00XXX ~ 01010 : Reserved. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration

Address: 58H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
T0_D-PLL_LOCKED_DAMPING2	T0_D-PLL_LOCKED_DAMPING1	T0_D-PLL_LOCKED_DAMPING0	T0_D-PLL_LOCKED_BW4	T0_D-PLL_LOCKED_BW3	T0_D-PLL_LOCKED_BW2	T0_D-PLL_LOCKED_BW1	T0_D-PLL_LOCKED_BW0

Bit	Name	Description
7 - 5	T0_DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_LOCKED_BW[4:0]	These bits set the locked bandwidth for T0 DPLL. 00XXX ~ 01010 : Reserved. 01011: 1.2 Hz. (default) 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration

Address: 59H
Type: Read / Write
Default Value: 1XXX1XXX

7	6	5	4	3	2	1	0
AUTO_BW_SEL	-	-	-	T0_LIMT	-	-	-

Bit	Name	Description
7	AUTO_BW_SEL	This bit determines whether starting or acquisition bandwidth / damping factor is used for T0 DPLL. 0: The starting and acquisition bandwidths / damping factors are not used. Only the locked bandwidth / damping factor is used regardless of the T0 DPLL locking stage. 1: The starting, acquisition or locked bandwidth / damping factor is used automatically depending on different T0 DPLL locking stages. (default)
6 - 4	-	Reserved.
3	T0_LIMT	This bit determines whether the integral path value is frozen when the T0 DPLL hard limit is reached. 0: Not frozen. 1: Frozen. It will minimize the subsequent overshoot when T0 DPLL is pulling in. (default)
2 - 0	-	Reserved.

PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration

Address: 5AH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT3	PH_LOS_COARSE_LIMT2	PH_LOS_COARSE_LIMT1	PH_LOS_COARSE_LIMT0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>COARSE_PH_LOS_LIMT_EN</td><td>This bit controls whether the occurrence of the coarse phase loss will result in the T0 DPLL unlocked.
0: Disabled.
1: Enabled. (default)</td></tr>
<tr><td>6</td><td>WIDE_EN</td><td>Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).</td></tr>
<tr><td>5</td><td>MULTI_PH_APP</td><td>This bit determines whether the PFD output of T0 DPLL is limited to ±1 UI or is limited to the coarse phase limit.
0: Limited to ±1 UI. (default)
1: Limited to the coarse phase limit. When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits; when the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH) for details.</td></tr>
<tr><td>4</td><td>MULTI_PH_8K_4K_2K_EN</td><td>This bit, together with the WIDE_EN bit (b6, 5AH) and the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH), determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz or 8 kHz. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits.
<table>
<tr><th>Selected Input Clock</th><th>MULTI_PH_8K_4K_2K_EN</th><th>WIDE_EN</th><th>Coarse Phase Limit</th></tr>
<tr><td rowspan="3">2 kHz, 4 kHz or 8 kHz</td><td>0</td><td>don’t-care</td><td>±1 UI</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>±1 UI</td></tr>
<tr><td>1</td><td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td></tr>
<tr><td rowspan="2">other than 2 kHz, 4 kHz and 8 kHz</td><td rowspan="2">don’t-care</td><td>0</td><td>±1 UI</td></tr>
<tr><td>1</td><td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td></tr>
</table></td></tr>
<tr><td>3 - 0</td><td>PH_LOS_COARSE_LIMT[3:0]</td><td>These bit set the coarse phase limit. The limit is used only in some cases. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).
0000: ±1 UI.
0001: ±3 UI.
0010: ±7 UI.
0011: ±15 UI.
0100: ±31 UI.
0101: ±63 UI. (default)
0110: ±127 UI.
0111: ±255 UI.
1000: ±511 UI.
1001: ±1023 UI.
1010-1111: Reserved.</td></tr>
</table>

PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration

Address: 5BH
Type: Read / Write
Default Value: 10XXX010

7	6	5	4	3	2	1	0
FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT2	PH_LOS_FINE_LIMT1	PH_LOS_FINE_LIMT0

Bit	Name	Description
7	FINE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the fine phase loss will result in the T0 DPLL unlocked. 0: Disabled. 1: Enabled. (default)
6	FAST_LOS_SW	This bit controls whether the occurrence of the fast loss will result in the T0 DPLL unlocked. 0: Does not result in the T0 DPLL unlocked. T0 DPLL will enter Temp-Holdover mode automatically. (default) 1: Results in the T0 DPLL unlocked. T0 DPLL will enter Lost-Phase mode if the T0 DPLL operating mode is switched automatically.
5 - 3	-	Reserved.
2 - 0	PH_LOS_FINE_LIMT[2:0]	These bits set a fine phase limit. 000: 0. 001: ± (45 ° ~ 90 °). 010: ± (90 ° ~ 180 °). (default) 011: ± (180 ° ~ 360 °). 100: ± (20 ns ~ 25 ns). 101: ± (60 ns ~ 65 ns). 110: ± (120 ns ~ 125 ns). 111: ± (950 ns ~ 955 ns).

T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration

Address: 5CH
Type: Read / Write
Default Value: 010001XX

7	6	5	4	3	2	1	0
MAN_HOLD-OVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLD-OVER_MODE1	TEMP_HOLD-OVER_MODE0	-	-

Bit	Name	Description
7	MAN_HOLDOVER	Refer to the description of the FAST_AVG bit (b5, 5CH).
6	AUTO_AVG	Refer to the description of the FAST_AVG bit (b5, 5CH).
5	FAST_AVG	This bit, together with the AUTO_AVG bit (b6, 5CH) and the MAN_HOLDOVER bit (b7, 5CH), determines a frequency offset acquiring method in T0 DPLL Holdover Mode.
4	READ_AVG	This bit controls the holdover frequency offset reading, which is read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH). 0: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is equal to the one written to them. (default) 1: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is not equal to the one written to them. The value is acquired by Automatic Slow Averaged method if the FAST_AVG bit (b5, 5CH) is '0'; or is acquired by Automatic Fast Averaged method if the FAST_AVG bit (b5, 5CH) is '1'.
3 - 2	TEMP_HOLDOVER_MODE[1:0]	These bits determine the frequency offset acquiring method in T0 DPLL Temp-Holdover Mode. 00: The method is the same as that used in T0 DPLL Holdover mode. 01: Automatic Instantaneous. (default) 10: Automatic Fast Averaged. 11: Automatic Slow Averaged.
1 - 0	-	Reserved.

FAST_AVG (bit 5) method table:

MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged (default)
		1	Automatic Fast Averaged
1	don't-care		Manual

T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1

Address: 5DH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLD-OVER_FREQ7	T0_HOLD-OVER_FREQ6	T0_HOLD-OVER_FREQ5	T0_HOLD-OVER_FREQ4	T0_HOLD-OVER_FREQ3	T0_HOLD-OVER_FREQ2	T0_HOLD-OVER_FREQ1	T0_HOLD-OVER_FREQ0

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[7:0]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2

Address: 5EH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLD-OVER_FREQ15	T0_HOLD-OVER_FREQ14	T0_HOLD-OVER_FREQ13	T0_HOLD-OVER_-FREQ12	T0_HOLD-OVER_FREQ11	T0_HOLD-OVER_-FREQ10	T0_HOLD-OVER_FREQ9	T0_HOLD-OVER_FREQ8

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[15:8]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3

Address: 5FH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLD-OVER_FREQ23	T0_HOLD-OVER_FREQ22	T0_HOLD-OVER_FREQ21	T0_HOLD-OVER_-FREQ20	T0_HOLD-OVER_-FREQ19	T0_HOLD-OVER_-FREQ18	T0_HOLD-OVER_-FREQ17	T0_HOLD-OVER_-FREQ16

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[23:16]	The T0_HOLDOVER_FREQ[23:0] bits represent a 2's complement signed integer. In T0 DPLL Holdover mode, the value written to these bits multiplied by 0.000011 is the frequency offset set manually; the value read from these bits multiplied by 0.000011 is the frequency offset automatically slow or fast averaged or manually set, as determined by the READ_AVG bit (b4, 5CH) and the FAST_AVG bit (b5, 5CH).

CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1

Address: 62H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_D-PLL_FREQ7	CURRENT_D-PLL_FREQ6	CURRENT_D-PLL_FREQ5	CURRENT_D-PLL_FREQ4	CURRENT_D-PLL_FREQ3	CURRENT_D-PLL_FREQ2	CURRENT_D-PLL_FREQ1	CURRENT_D-PLL_FREQ0

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[7:0]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2

Address: 63H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_D-PLL_FREQ15	CURRENT_D-PLL_FREQ14	CURRENT_D-PLL_FREQ13	CURRENT_D-PLL_FREQ12	CURRENT_D-PLL_FREQ11	CURRENT_D-PLL_FREQ10	CURRENT_D-PLL_FREQ9	CURRENT_D-PLL_FREQ8

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[15:8]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3

Address: 64H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_D-PLL_FREQ23	CURRENT_D-PLL_FREQ22	CURRENT_D-PLL_FREQ21	CURRENT_D-PLL_FREQ20	CURRENT_D-PLL_FREQ19	CURRENT_D-PLL_FREQ18	CURRENT_D-PLL_FREQ17	CURRENT_D-PLL_FREQ16

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[23:16]	The CURRENT_DPLL_FREQ[23:0] bits represent a 2's complement signed integer. If the value in these bits is multiplied by 0.000011, the current frequency offset of the T0 DPLL output in ppm with respect to the master clock will be gotten.

DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration

Address: 65H
Type: Read / Write
Default Value: 10001100

7	6	5	4	3	2	1	0
FRE-Q_LIMT_PH_LOS	DPLL_FREQ_-SOFT_LIMT6	DPLL_FREQ_-SOFT_LIMT5	DPLL_FREQ_-SOFT_LIMT4	DPLL_FREQ_-SOFT_LIMT3	DPLL_FREQ_-SOFT_LIMT2	DPLL_FREQ_-SOFT_LIMT1	DPLL_FREQ_-SOFT_LIMT0

Bit	Name	Description
7	FREQ_LIMT_PH_LOS	This bit determines whether the T0 DPLL in hard alarm status will result in it unlocked. 0: Disabled. 1: Enabled. (default)
6 - 0	DPLL_FREQ_SOFT_LIMT[6:0]	These bits represent an unsigned integer. If the value is multiplied by 0.724, the DPLL soft limit for T0 path in ppm will be gotten. The DPLL soft limit is symmetrical about zero.

DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1

Address: 66H
Type: Read / Write
Default Value: 10101011

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT7	DPLL_FREQ_HARD_LIMT6	DPLL_FREQ_HARD_LIMT5	DPLL_FREQ_HARD_LIMT4	DPLL_FREQ_HARD_LIMT3	DPLL_FREQ_HARD_LIMT2	DPLL_FREQ_HARD_LIMT1	DPLL_FREQ_HARD_LIMT0

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[7:0]	Refer to the description of the DPLL_FREQ_HARD_LIMT[15:8] bits (b7~0, 67H).

DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2

Address: 67H
Type: Read / Write
Default Value: 00011001

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT15	DPLL_FREQ_HARD_LIMT14	DPLL_FREQ_HARD_LIMT13	DPLL_FREQ_HARD_LIMT12	DPLL_FREQ_HARD_LIMT11	DPLL_FREQ_HARD_LIMT10	DPLL_FREQ_HARD_LIMT9	DPLL_FREQ_HARD_LIMT8

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[15:8]	The DPLL_FREQ_HARD_LIMT[15:0] bits represent an unsigned integer. If the value is multiplied by 0.0014, the DPLL hard limit for T0 path in ppm will be gotten. The DPLL hard limit is symmetrical about zero.

CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1

Address: 68H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA7	CURRENT_PH_DATA6	CURRENT_PH_DATA5	CURRENT_PH_DATA4	CURRENT_PH_DATA3	CURRENT_PH_DATA2	CURRENT_PH_DATA1	CURRENT_PH_DATA0

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[7:0]	Refer to the description of the CURRENT_PH_DATA[15:8] bits (b7~0, 69H).

CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2

Address: 69H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA15	CURRENT_PH_DATA14	CURRENT_PH_DATA13	CURRENT_PH_DATA12	CURRENT_PH_DATA11	CURRENT_PH_DATA10	CURRENT_PH_DATA9	CURRENT_PH_DATA8

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[15:8]	The CURRENT_PH_DATA[15:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the averaged phase error of the T0 DPLL feedback with respect to the selected input clock in ns will be gotten.

T0_APLL_BW_CNFG - T0 APLL Bandwidth Configuration

Address: 6AH
Type: Read / Write
Default Value: XX01XX01

7	6	5	4	3	2	1	0
-	-	T0_APLL_BW1	T0_APLL_BW0	-	-	-	-

Bit	Name	Description
7 - 6	-	Reserved.
5 - 4	T0_APLL_BW[1:0]	These bits set the bandwidth for T0 APLL. 00: 100 kHz. 01: 500 kHz. (default) 10: 1 MHz. 11: 2 MHz.
3 - 0	-	Reserved.

6.2.8 OUTPUT CONFIGURATION REGISTERS

OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration

Address: 6DH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
OUT1_PATH_-SEL3	OUT1_PATH_-SEL2	OUT1_PATH_-SEL1	OUT1_PATH_-SEL0	OUT1_DIVID-ER3	OUT1_DIVID-ER2	OUT1_DIVID-ER1	OUT1_DIVID-ER0

Bit	Name	Description
7 - 4	OUT1_PATH_SEL[3:0]	These bits select an input to OUT1. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1111: Reserved.
3 - 0	OUT1_DIVIDER[3:0]	These bits select a division factor of the divider for OUT1. The output frequency is determined by the division factor and the signal derived from T0 DPLL or T0 APLL output (selected by the OUT1_PATH_SEL[3:0] bits (b7~4, 6DH)). If the signal is derived from one of the T0 DPLL outputs, please refer to Table 22 for the division factor selection. If the signal is derived from the T0 APLL output, please refer to Table 23 for the division factor selection.

OUT1_INV_CNFG - Output Clock 1 Invert Configuration

Address:73H
Type: Read / Write
Default Value: XXXXX0XX

7	6	5	4	3	2	1	0
-	-	-	-	-	OUT1_INV	-	-

Bit	Name	Description
7 - 3	-	Reserved.
2	OUT1_INV	This bit determines whether the output on OUT1 is inverted. 0: Not inverted. (default) 1: Inverted.
1 - 0	-	Reserved.

FR_SYNC_CNFG - Frame Sync Output Configuration

Address:74H
Type: Read / Write
Default Value: 01X000XX

7	6	5	4	3	2	1	0
IN_2K_4K_8K_-INV	8K_EN	-	8K_PUL_POSI-TION	8K_INV	8K_PUL	-	-

Bit	Name	Description
7	IN_2K_4K_8K_INV	This bit determines whether the input clock is inverted before locked by the T0 DPLL when the input clock is 2 kHz, 4 kHz or 8 kHz. 0: Not inverted. (default) 1: Inverted.
6	8K_EN	This bit determines whether an 8 kHz signal is enabled to be output on FRSYNC_8K. 0: Disabled. FRSYNC_8K outputs low. 1: Enabled. (default)
5	-	Reserved.
4	8K_PUL_POSITION	This bit is valid only when FRSYNC_8K output pulse; i.e., when one of the 8K_PUL bit (b2, 74H) is '1' or when the 8K_PUL bit (b2, 74H) is '1'. It determines the pulse position referring to the standard 50:50 duty cycle. 0: Pulsed on the falling edge of the standard 50:50 duty cycle position. (default) 1: Pulsed on the rising edge of the standard 50:50 duty cycle position.
3	8K_INV	This bit determines whether the output on FRSYNC_8K is inverted. 0: Not inverted. (default) 1: Inverted.
2	8K_PUL	This bit determines whether the output on FRSYNC_8K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT1.
1 - 0	-	Reserved.

6.2.9 PBO & PHASE OFFSET CONTROL REGISTERS

PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration

Address:78H
Type: Read / Write
Default Value: 0X000110

7	6	5	4	3	2	1	0
IN_NOISE_WINDOW	-	PH_MON_EN	PH_MON_PBO_EN	PH_TR_MON_LIMT3	PH_TR_MON_LIMT2	PH_TR_MON_LIMT1	PH_TR_MON_LIMT0

Bit	Name	Description
7	IN_NOISE_WINDOW	This bit determines whether the input clock whose edge respect to the reference clock is outside ±5% is enabled to be selected for T0 DPLL. 0: Disabled. (default) 1: Enabled.
6	-	Reserved.
5	PH_MON_EN	This bit is valid only when the PH_MON_PBO_EN bit (b4, 78H) is '1'. It determines whether the Phase Transient Monitor is enabled to monitor the phase-time changes on the T0 selected input clock. 0: Disabled. (default) 1: Enabled.
4	PH_MON_PBO_EN	This bit determines whether a PBO event is triggered when the phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds with the PH_MON_EN bit being '1'. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits (b3~0, 78H). 0: Disabled. (default) 1: Enabled.
3 - 0	PH_TR_MON_LIMT[3:0]	These bits represent an unsigned integer. The Phase Transient Monitor limit in ns can be calculated as follows: *Limit (ns) = (PH_TR_MON_LIMT[3:0] + 7) X 156.*

6.2.10 SYNCHRONIZATION CONFIGURATION REGISTERS

SYNC_MONITOR_CNFG - Sync Monitor Configuration

Address:7CH
Type: Read / Write
Default Value: 00101011

7	6	5	4	3	2	1	0
SYNC_BYPASS	SYNC_MON_LIMT2	SYNC_MON_LIMT1	SYNC_MON_LIMT0	-	-	-	-

Bit	Name	Description
7	SYNC_BYPASS	This bit selects one frame sync input signal to synchronize the frame sync output signal. 0: EX_SYNC1 is selected. (default) 1: When the T0 selected input clock is IN1_CMOS, EX_SYNC1 is selected; when the T0 selected input clock is IN2_C-MOS, EX_SYNC2 is selected;when there is no T0 selected input clock, no frame sync input signal is selected.
6 - 4	SYNC_MON_LIMT[2:0]	These bits set the limit for the external sync alarm. 000: ±1 UI. 001: ±2 UI. 010: ±3 UI. (default) 011: ±4 UI. 100: ±5 UI. 101: ±6 UI. 110: ±7 UI. 111: ±8 UI.
3 - 0	-	These bits must be set to '1011'.

SYNC_PHASE_CNFG - Sync Phase Configuration

Address:7DH
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	SYNC_PH21	SYNC_PH20	SYNC_PH11	SYNC_PH10

Bit	Name	Description
7 - 4	-	Reserved.
3 - 2	SYNC_PH2[1:0]	These bits set the sampling of EX_SYNC2 when EX_SYNC2 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC2 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late.
1 - 0	SYNC_PH1[1:0]	These bits set the sampling of EX_SYNC1 when EX_SYNC1 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late.

7 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax}.

7.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \times \theta_{JA}$

Where:

θ_{JA} = *Junction-to-Ambient Thermal Resistance of the Package*

T_j = *Junction Temperature*

T_A = *Ambient Temperature*

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 32:

Power consumption is the core power excluding the power dissipated in the loads. Table 33 provides power consumption in special environments.

Table 32: Power Consumption and Maximum Junction Temperature

Package	Power Consumption (W)	Operating Voltage (V)	T_A (°C)	Maximum Junction Temperature (°C)
VFQFPN/NL68	1.57	3.6	85	125

7.2 EXAMPLE OF JUNCTION TEMPERATURE CALCULATION

Assume:

$T_A = 85°C$

θ_{JA} = *20.9 °C/W (VFQFPN/NL68 Soldered & when airfow rate is 0 m/s)*

P = 1.57W

The junction temperature T_j can be calculated as follows:

$T_j = T_A + P \times \theta_{JA} = 85°C + 1.57W \times 20.9°C/W = 117.8°C$

The junction temperature of 117.8°C is below the maximum junction temperature of 125°C so no extra heat enhancement is required.

In some operation environments, the calculated junction temperature might exceed the maximum junction temperature of 125°C and an external thermal solution such as a heatsink is required.

7.3 HEATSINK EVALUATION

A heatsink is expanding the surface area of the device to which it is attached. θ_{JA} is now a combination of device case and heat-sink thermal resistance, as the heat flowing from the die junction to ambient goes through the package and the heatsink. θ_{JA} can be calculated as follows:

Equation 2: $\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

Where:

θ_{JC} = *Junction-to-Case Thermal Resistance*

θ_{CH} = *Case-to-Heatsink Thermal Resistance*

θ_{HA} = *Heatsink-to-Ambient Thermal Resistance*

$\theta_{CH} + \theta_{HA}$ determines which heatsink and heatsink attachment can be selected to ensure the junction temperature does not exceed the maximum junction temperature. According to Equation 1 and 2,

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

Equation 3: $\theta_{CH} + \theta_{HA} = (T_j - T_A) / P - \theta_{JC}$

Assume:

$T_j = 125°C\ (T_{jmax})$

$T_A = 85°C$

P = 1.57W

θ_{JC} = *12.6°C/W (VFQFPN/NL68)*

$\theta_{CH} + \theta_{HA}$ ***can be calculated as follows:***

$\theta_{CH} + \theta_{HA} = (125°C - 85°C) / 1.57W - 12.6°C/W = 12.9°C/W$

That is, if a heatsink and heatsink attachment whose $\theta_{CH} + \theta_{HA}$ is below or equal to 12.9°C/W is used in such operation environment, the junction temperature will not exceed the maximum junction temperature.

Table 33: Thermal Data

Package	Pin Count	Thermal Pad	θ_{JC} (°C/W)	θ_{JB} (°C/W)	θ_{JA} (°C/W) Air Flow in m/s					
					0	1	2	3	4	5
VFQFPN/NL68	68	Yes/Exposed	9.1	8.3	39.4	34.1	31.7	30.2	29.1	28.2
VFQFPN/NL68	68	Yes/Soldered*	9.1	1.2	20.9	16.2	15.2	14.6	14.1	13.8
*note: Simulated with 3 x 3 array of thermal vias.										

7.4 VFQFPN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 18. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

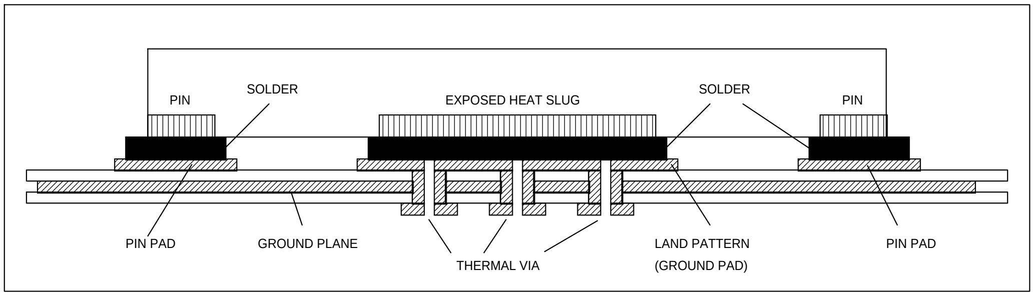


Figure 18. Assembly for Expose Pad thermal Release Path (Side View)

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as 'heat pipes'. The number of vias (i.e. 'heat pipes') are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Lead fame Base Package, Amkor Technology.

8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATING

Table 34: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage VDD	-0.5	4.0	V
V_{IN}	Input Voltage (non-supply pins)		5.5	V
V_{OUT}	Output Voltage (non-supply pins)		5.5	V
T_{STOR}	Storage Temperature	-50	+150	°C

8.2 RECOMMENDED OPERATION CONDITIONS

Table 35: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power Supply (DC voltage) VDD	3.0	3.3	3.6	V	
T_A	Ambient Temperature Range	-40		+85	°C	
I_{DD}	Supply Current		325	365	mA	Exclude the loading current and power
P_{TOT}	Total Power Dissipation		1.08	1.30	W	

8.3 I/O SPECIFICATIONS

8.3.1 CMOS INPUT / OUTPUT PORT

Table 36: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2.0			V	
V_{IL}	Input Voltage Low			0.8	V	
I_{IN}	Input Current			10	μA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 37: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2.0			V	
V_{IL}	Input Voltage Low			0.8	V	
P_U	Pull-Up Resistor	23		38	KΩ	TDI, TMS pin
		41		82		$\overline{\text{RST}}$ pin
		82		165		
I_{IN}	Input Current	85		140	μA	TDI, TMS pin
		40		80		$\overline{\text{RST}}$ pin
		20		40		
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 38: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2.0			V	
V_{IL}	Input Voltage Low			0.8	V	
P_D	Pull-Down Resistor	8		14	KΩ	$\overline{\text{TRST}}$ and TCK pin
		16		23		other CMOS input port with internal pull-down resistor
		183		366		SDI, CLKE pin
I_{IN}	Input Current	390		640	μA	$\overline{\text{TRST}}$ and TCK pin
		180		340		other CMOS input port with internal pull-down resistor
		15		30		SDI, CLKE pin
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 39: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4		V_{DD}	V	I_{OH} = 8 mA
	V_{OL}	Output Voltage Low	0		0.4	V	I_{OL} = 8 mA
	t_R	Rise time (20% to 80%)		3	4	ns	15 pF
	t_F	Fall time (20% to 80%)		3	4	ns	15 pF
Other Output	V_{OH}	Output Voltage High	2.4		V_{DD}	V	I_{OH} = 4 mA
	V_{OL}	Output Voltage Low	0		0.4	V	I_{OL}= 4 mA
	t_R	Rise Time (20% to 80%)			10	ns	50 pF
	t_F	Fall Time (20% to 80%)			10	ns	50 pF

8.4 JITTER & WANDER PERFORMANCE

Table 40: Output Clock Jitter Generation

Test Definition [1]	Peak to Peak Typ	RMS Typ	Note	Test Filter
N x 2.048MHz without APLL	<2 ns	<200 ps		20 Hz - 100 kHz
N x 2.048MHz with T0 APLL	<1 ns	<100 ps	See Table 41: Output Clock Phase Noise for details	20 Hz - 100 kHz
N x 1.544 MHz without APLL	<2 ns	<200 ps		10 Hz - 40 kHz
N x 1.544 MHz with T0 APLL	<1 ns	<100 ps	See Table 41: Output Clock Phase Noise for details	10 Hz - 40 kHz
44.736 MHz with T0 APLL	<1 ns	<100 ps	See Table 41: Output Clock Phase Noise for details	100 Hz - 800 kHz
44.736 MHz without APLL	<2 ns	<200 ps		100 Hz - 800 kHz
34.368 MHz with T0 APLL	<1 ns	<100 ps	See Table 41: Output Clock Phase Noise for details	10 Hz - 400 kHz
34.368 MHz without APLL	<2 ns	<200 ps		10 Hz - 400 kHz
OC-3 (Chip T0 DPLL + T0 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz output	0.004 UI p-p	0.001 UI RMS	GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
	0.004 UI p-p	0.001 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz - 1.3 MHz
	0.001 UI p-p	0.001 UI RMS	G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz - 1.3 MHz
OC-12 (Chip T0 DPLL + T0 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz output + Intel GD16523 + Optical transceiver)	0.018 UI p-p	0.007 UI RMS	GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps)	12 kHz - 5 MHz
	0.028 UI p-p	0.009 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-1608 ps)	1 kHz - 5 MHz
	0.002 UI p-p	0.001 UI RMS	G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-160 8ps)	250 kHz - 5 MHz
STM-16 (Chip T0 DPLL + T0 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz output + Intel GD16523 + Optical transceiver)	0.162 UI p-p	0.03 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-402 ps)	5 kHz - 20 MHz
	0.01 UI p-p	0.009 UI RMS	G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-402 ps)	1 MHz - 20 MHz

Note:
1. CMAC E2747 TCXO is used.

Table 41: Output Clock Phase Noise

Output Clock [1]	@100Hz Offset Typ	@1kHz Offset Typ	@10kHz Offset Typ	@100kHz Offset Typ	@1MHz Offset Typ	@5MHz Offset Typ	Unit
155.52 MHz (T0 DPLL + T0 APLL)	-82	-98	-107	-112	-119	-140	dBC/Hz
38.88 MHz (T0 DPLL + T0 APLL)	-94	-110	-118	-124	-131	-143	dBC/Hz
16E1 (T0 APLL)	-94	-110	-118	-125	-131	-142	dBC/Hz
16T1 (T0 APLL)	-95	-112	-120	-127	-132	-143	dBC/Hz
E3 (T0 APLL)	-93	-109	-116	-124	-131	-138	dBC/Hz
T3 (T0 APLL)	-92	-108	-116	-122	-126	-141	dBC/Hz

Note:
1. CMAC E2747 TCXO is used.

Table 42: Input Jitter Tolerance (155.52 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
12 μHz	> 2800
178 μHz	> 2800
1.6 mHz	> 311
15.6 mHz	> 311
0.125 Hz	> 39
19.3 Hz	> 39
500 Hz	> 1.5
6.5 kHz	> 1.5
65 kHz	> 0.15
1.3 MHz	> 0.15

Table 43: Input Jitter Tolerance (1.544 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	150
5 Hz	140
20 Hz	130
300 Hz	38
400 Hz	25
700 Hz	15
2400 Hz	5
10 kHz	1.2
40 kHz	0.5

Table 44: Input Jitter Tolerance (2.048 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	150
5 Hz	140
20 Hz	130
300 Hz	40
400 Hz	33
700 Hz	18
2400 Hz	5.5
10 kHz	1.3
50 kHz	0.4
100 kHz	0.4

Table 45: Input Jitter Tolerance (8 kHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	0.8
5 Hz	0.7
20 Hz	0.6
300 Hz	0.16
400 Hz	0.14
700 Hz	0.07
2400 Hz	0.02
3600 Hz	0.01

Table 46: T0 DPLL Jitter Transfer & Damping Factor

3 dB Bandwidth	Programmable Damping Factor
1.2 Hz	1.2, 2.5, 5, 10, 20
2.5 Hz	1.2, 2.5, 5, 10, 20
4 Hz	1.2, 2.5, 5, 10, 20
8 Hz	1.2, 2.5, 5, 10, 20
18 Hz	1.2, 2.5, 5, 10, 20
35 Hz	1.2, 2.5, 5, 10, 20
70 Hz	1.2, 2.5, 5, 10, 20
560 Hz	1.2, 2.5, 5, 10, 20

8.5 OUTPUT WANDER GENERATION

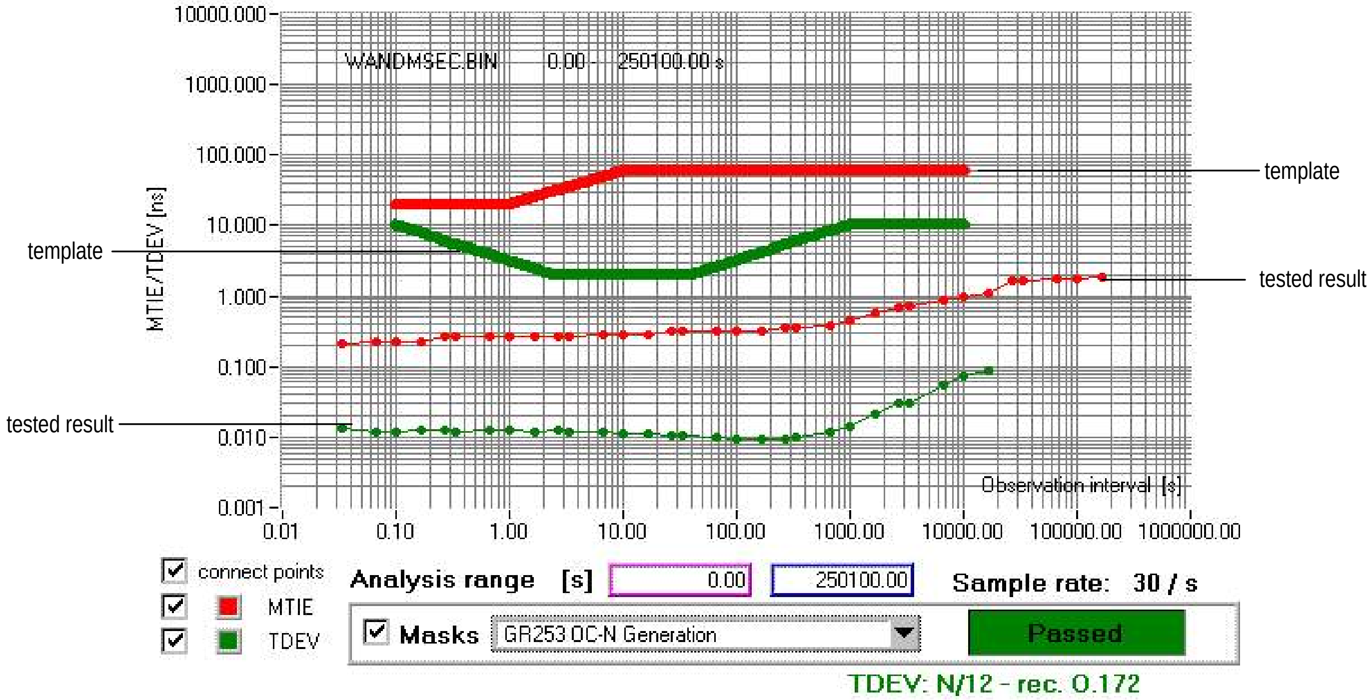


Figure 19. Output Wander Generation

8.6 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

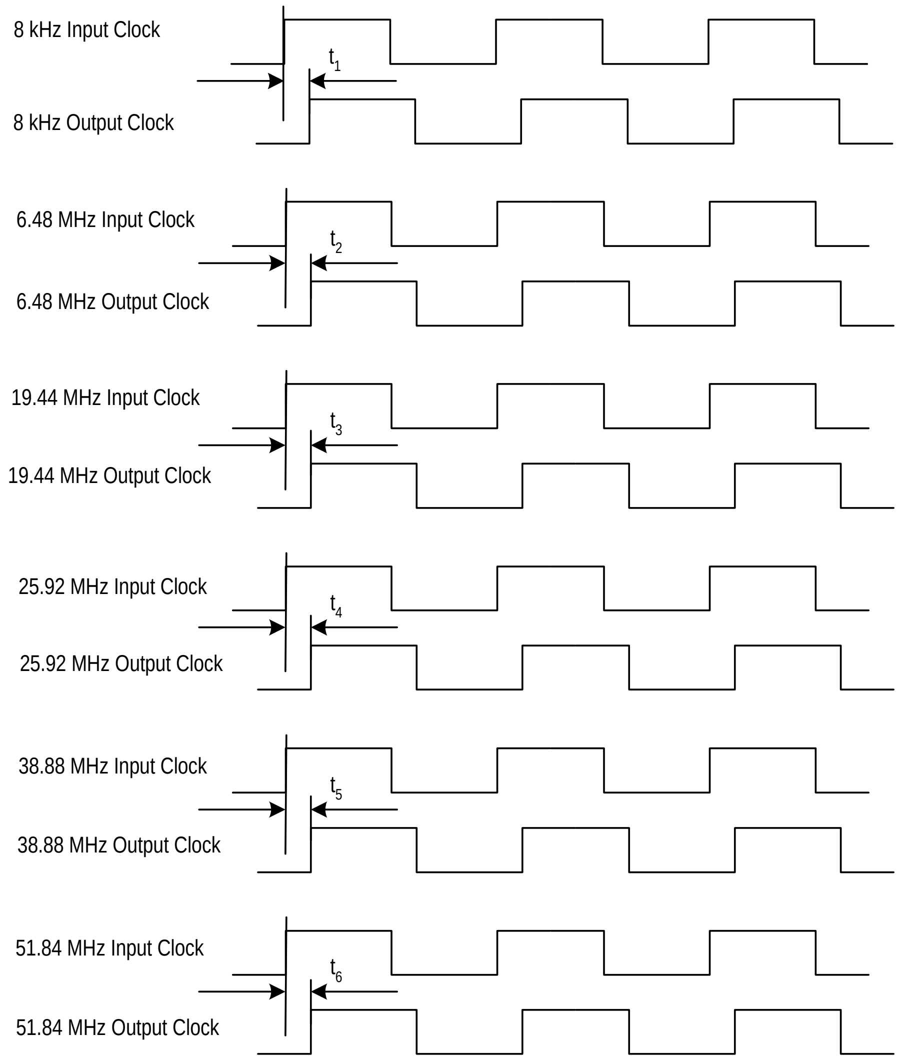


Figure 20. Input / Output Clock Timing

Table 47: Input/Output Clock Timing

Symbol	Typical Delay [1] (ns)	Peak to Peak Delay Variation (ns)
t_1	4	1.6
t_2	1	1.6
t_3	1	1.6
t_4	2	1.6
t_5	1.4	1.6
t_6	3	1.6

Note:
1. Typical delay provided as reference only.

8.7 OUTPUT CLOCK TIMING

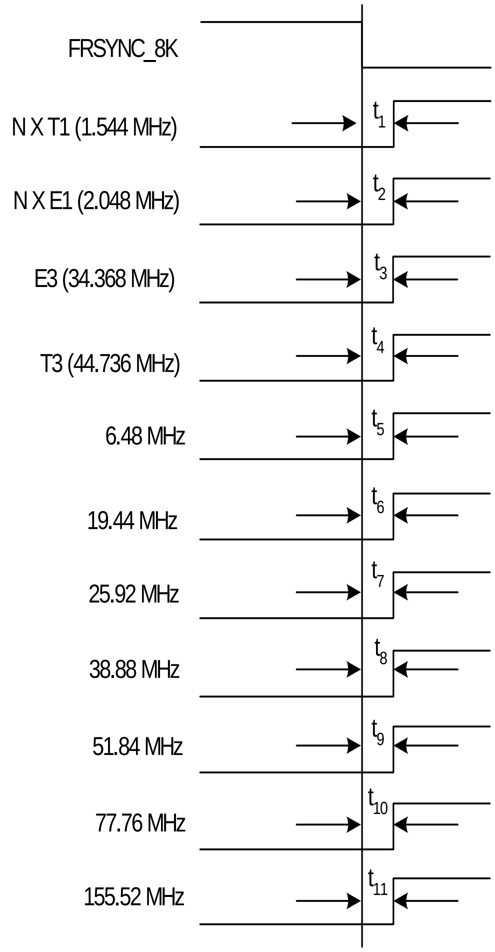


Table 48: Output Clock Timing

Symbol	Typical Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	0	2
t_2	0	2
t_3	0	2
t_4	0	2
t_5	0	2
t_6	0	2
t_7	0	2
t_8	0	2
t_9	0	2
t_{10}	0	2
t_{11}	0	1.5

3G	---	Third Generation
ADSL	---	Asymmetric Digital Subscriber Line
AMI	---	Alternate Mark Inversion
APLL	---	Analog Phase Locked Loop
ATM	---	Asynchronous Transfer Mode
BITS	---	Building Integrated Timing Supply
CMOS	---	Complementary Metal-Oxide Semiconductor
DCO	---	Digital Controlled Oscillator
DPLL	---	Digital Phase Locked Loop
DSL	---	Digital Subscriber Line
DSLAM	---	Digital Subscriber Line Access MUX
DWDM	---	Dense Wavelength Division Multiplexing
EPROM	---	Erasable Programmable Read Only Memory
GPS	---	Global Positioning System
GSM	---	Global System for Mobile Communications
IIR	---	Infinite Impulse Response
IP	---	Internet Protocol
ISDN	---	Integrated Services Digital Network
JTAG	---	Joint Test Action Group
LOS	---	Loss Of Signal
LPF	---	Low Pass Filter
MTIE	---	Maximum Time Interval Error
MUX	---	Multiplexer
OBSAI	---	Open Base Station Architecture Initiative
OC-n	---	Optical Carried rate, n = 1, 3, 12, 48, 192, 768; 51 Mbit/s, 155 Mbit/s, 622 Mbit/s, 2.5 Gbit/s, 10 Gbit/s, 40 Gbit/s.
PBO	---	Phase Build-Out

PDH	---	Plesiochronous Digital Hierarchy
PFD	---	Phase & Frequency Detector
PLL	---	Phase Locked Loop
RMS	---	Root Mean Square
PRS	---	Primary Reference Source
SDH	---	Synchronous Digital Hierarchy
SEC	---	SDH / SONET Equipment Clock
SMC	---	SONET Minimum Clock
SONET	---	Synchronous Optical Network
SSU	---	Synchronization Supply Unit
STM	---	Synchronous Transfer Mode
TCM-ISDN	---	Time Compression Multiplexing Integrated Services Digital Network
TDEV	---	Time Deviation
UI	---	Unit Interval
WLL	---	Wireless Local Loop

Index

S

V

PACKAGE DIMENSIONS - 68-PIN NL

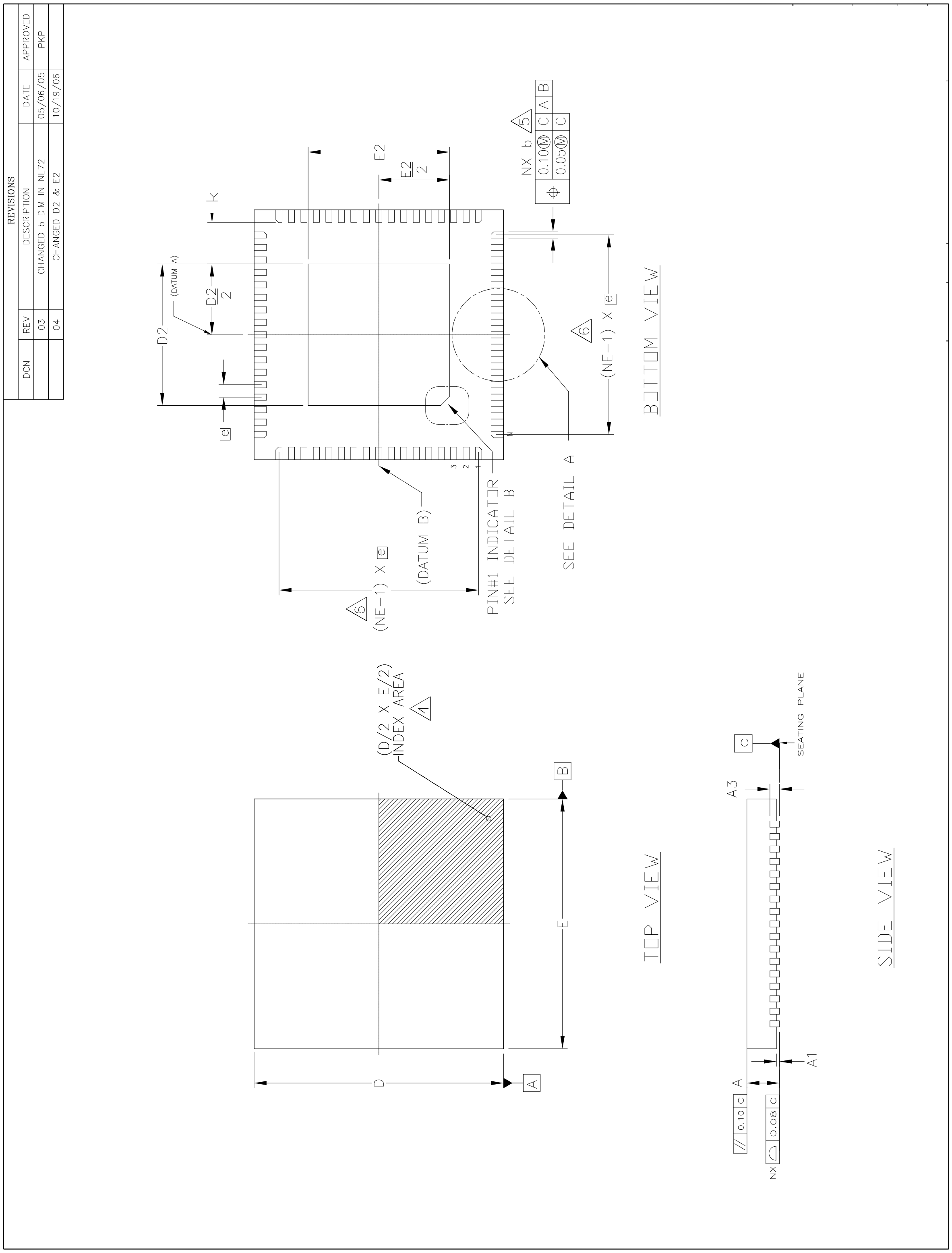
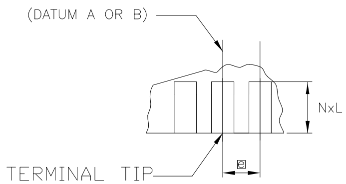


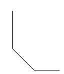
Figure 21. 68-Pin NL Package Dimensions (a) (in Millimeters)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	03	CHANGED b DIM IN NL72	05/06/05	PKP
	04	CHANGED D2 & E2	10/19/06	



68 LEAD

DETAIL A



68 LEAD

DETAIL B

SYM BOL	NL68			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
b	0.18	0.25	0.30	5
D		10.00 BSC		
E		10.00 BSC		
D2	7.60	7.70	7.80	8
E2	7.60	7.70	7.80	8
k	0.20	-	-	
L	0.45	0.50	0.55	
e		0.50 BSC		
N		68		6
Nd		17		6
Ne		17		6

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M−1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X−DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y−DIRECTION.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUB. 95 SEC. 4.3 SPP−002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

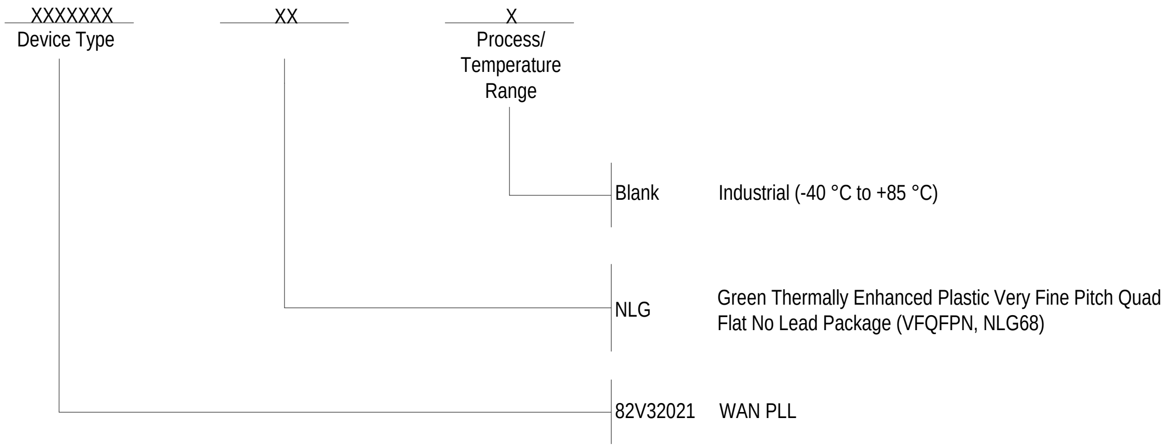
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.

6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

Figure 22. 68-Pin NL Package Dimensions (b) (in Millimeters)

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

09/11/2008	Page 103
03/20/2009	Pages 42, 43, 92, 93, 97
07/23/2009	Pages 12, 96
04/24/2015	Page 108 removed leaded device

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