RENESAS

2.5V Differential LVDS Clock Divider and Fanout Buffer

874208I

DATA SHEET

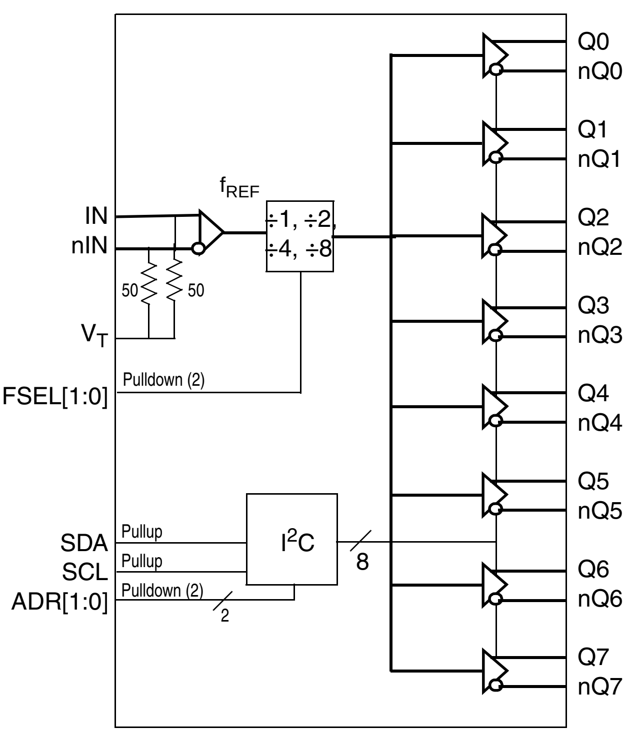
General Description

The 874208I is a high-performance differential LVDS clock divider and fanout buffer. The device is designed for the frequency division and signal fanout of high-frequency, low phase-noise clocks. The 874208I is characterized to operate from a 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 874208I ideal for those clock distribution applications demanding well-defined performance and repeatability. The integrated input termination resistors make interfacing to the reference source easy and reduce passive component count. Each output can be individually enabled or disabled in the high-impedance state controlled by a I^2C register. On power-up, all outputs are enabled.

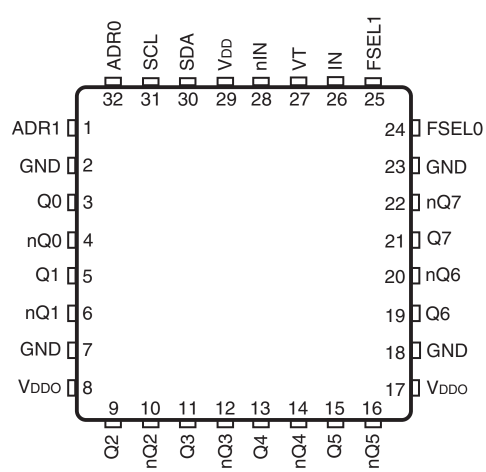
Features

- One differential input reference clock
- Differential pair can accept the following differential input levels: LVDS, LVPECL, CML
- Integrated input termination resistors
- Eight LVDS outputs
- Selectable clock frequency division of ÷1, ÷2, ÷4 and ÷8
- Maximum input clock frequency: 500MHz
- LVCMOS interface levels for the control inputs
- Internal regulator for improved noise immunity
- Individual output enable/disabled by I^2C interface
- Output skew: 28ps
- Additive Phase Jitter, RMS: 0.168ps (typical), 125MHz
- Low additive phase jitter
- Full 2.5V supply voltage
- Available in Lead-free (RoHS 6) package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



ICS874208I

32 Lead VFQFN

5mm x 5mm x 0.925mm package body

K Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 32	ADR1, ADR0	Input	Pulldown	I^2C Address inputs. LVCMOS/LVTTL compatible interface levels.
2, 7, 18, 23	GND	Power		Power supply ground.
3, 4	Q0, nQ0	Output		Differential output pair 0. LVDS interface levels.
5, 6	Q1, nQ1	Output		Differential output pair 1. LVDS interface levels.
8, 17	V_{DDO}	Power		Output power supply pins.
9, 10	Q2, nQ2	Output		Differential output pair 2. LVDS interface levels.
11, 12	Q3, nQ3	Output		Differential output pair 3. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential output pair 4. LVDS interface levels.
15, 16	Q5, nQ5	Output		Differential output pair 5. LVDS interface levels.
19, 20	Q6, nQ6	Output		Differential output pair 6. LVDS interface levels.
21, 22	Q7, nQ7	Output		Differential output pair 7. LVDS interface levels.
24, 25	FSEL0, FSEL1	Input	Pulldown	Frequency divider select controls. See Table 3A for function. LVCMOS/LVTTL interface levels.
26	IN	Input		Non-inverting differential clock input.
27	V_T	Termination input		Input for termination. Both IN and nIN inputs are internally terminated 50Ω to this pin. See input termination information in the applications section.
28	nIN	Input		Inverting differential clock input.
29	V_{DD}	Power		Power supply pins.
30	SDA	I/O	Pullup	I^2C Data Input/Output. Input: LVCMOS/LVTTL interface levels. Output: open drain.
31	SCL	Input	Pullup	I^2C clock input. LVCMOS/LVTTL compatible interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Input Frequency Divider Operation

The FSEL1 and FSEL0 controls configure the input frequency divider. In the default state (FSEL[1:0] are set to logic 0:0 or left open) the output frequency is equal to the input frequency (divide-by-1). The other FSEL[1:0] settings configure the input divider to ÷2, ÷4 or ÷8, respectively.

Table 3A. FSEL[1:0] Input Selection Function Table

Input		
FSEL1	**FSEL0**	**Operation**
0 (default)	0 (default)	$f_{Q[7:0]} = f_{REF} \div 1$
0	1	$f_{Q[7:0]} = f_{REF} \div 2$
1	0	$f_{Q[7:0]} = f_{REF} \div 4$
1	1	$f_{Q[7:0]} = f_{REF} \div 8$

NOTE: FSEL1, FSEL0 are asynchronous controls

Output Enable Operation

The output enable/disable state of each individual differential output Qx can be set by the content of the I^{2}C register (see Table 3C). A logic zero to an I^{2}C bit in register 0 enables the corresponding differential output, while a logic one disables the differential output (see Table 3B). After each power cycle, the device resets all I^{2}C bits (D[7:0]) to its default state (logic 0) and all Qx outputs are enabled. After the first valid I^{2}C write, the output enable state is controlled by the I^{2}C register. Setting and changing the output enable state through the I^{2}C interface is asynchronous to the input reference clock.

Table 3B. Individual Output Enable Control

Bit	
D[7:0]	**Operation**
0 (default)	Output Qx, nQx is enabled.
1	Output Qx, nQx is high-impedance.

Table 3C. Individual output enable control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Output	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Default	0	0	0	0	0	0	0	0

I^{2}C Interface Protocol

The ICS874208I uses an I^{2}C slave interface for writing and reading the device configuration to and from the on-chip configuration registers. This device uses the standard I^{2}C write format for a write transaction, and a standard I^{2}C read format for a read transaction. Figure 1 defines the I^{2}C elements of the standard I^{2}C transaction. These elements consist of a start bit, data bytes, an acknowledge or Not-Acknowledge bit and the stop bit. These elements are arranged to make up the complete I^{2}C transactions as shown in Figure 2 and Figure 3. Figure 2 is a write transaction while Figure 3 is read transaction. The 7-bit I^{2}C slave address of the 874208I is a combination of a 4-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0] (binary 11010, ADR1, ADR0). Bit 0 of slave address is used by the bus controller to select either the read or write mode. The hardware pins ADR1 and ADR0 should be individually set by the user to avoid address conflicts of multiple 874208I devices on the same bus.

Table 3D. I^{2}C Slave Address

7	6	5	4	3	2	1	0
1	1	0	1	0	ADR1	ADR0	R/W

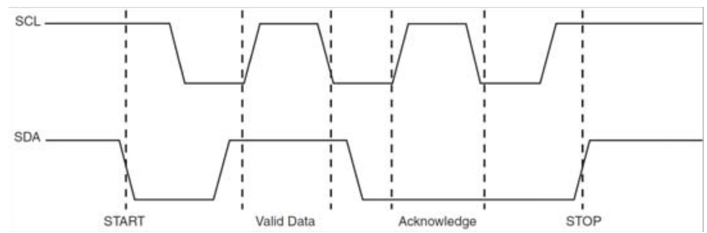


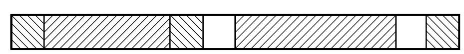
Figure 1: Standard I^{2}C Transaction

START (ST) – defined as high-to-low transition on SDA while holding SCL HIGH.

DATA – between START and STOP cycles, SDA is synchronous with SCL. Data may change only when SCL is LOW and must be stable when SCL is HIGH.

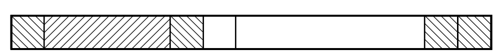
ACKNOWLEDGE (AK) – SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

STOP (SP) – defined as low-to-high transition on SDA while holding SCL HIGH



S DevAdd W A Data Byte A P

Figure 2: Write Transaction



S DevAdd R A Data Byte A P

Figure 3: Read Transaction

S – Start or Repeated Start
W – R/~W is set for Write
R – R/~W is set for Read
A – Ack
DevAdd – 7 bit Device Address
RegAdd – 8 bit Register Address, MSB = Q7 and LSB = Q0
P – Stop

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.5V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
Maximum Junction Temperature, TJ_{MAX}	125°C
ESD - Human Body Model; NOTE 1	2000V
ESD - Charged Device Model; NOTE 1	500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101. ESD ratings are target specifications.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5V	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5V	2.625	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				203	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	FSEL1, FSEL0, ADR[1:0]	$V_{DD} = V_{IN}$ = 2.625V			150	µA
		SCK, SDA	$V_{DD} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	FSEL1, FSEL0, ADR[1:0]	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		SCK, SDA	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{IN}	Input Voltage Swing	IN, nIN		0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			1.2		V_{DD}	V
V_{DIFF}	Differential Input Voltage Swing	IN, nIN		0.3		2.4	V
R_{IN}	Input Resistance	IN, nIN to V_T		45	50	66	Ω
R_{IN}, D_{IFF}	Differential Input Resistance	IN to nIN, V_T = open		90	100	132	Ω

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		400	460	600	mV
ΔV_{OD}	V_{OD} Magnitude Change			15	94	mV
V_{OS}	Offset Voltage		1.09	1.15	1.18	V
ΔV_{OS}	V_{OS} Magnitude Change			2	14	mV

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, $V_{DD} = V_{DDO} = 2.5V$, $T_A = -40°C$ to 85°C

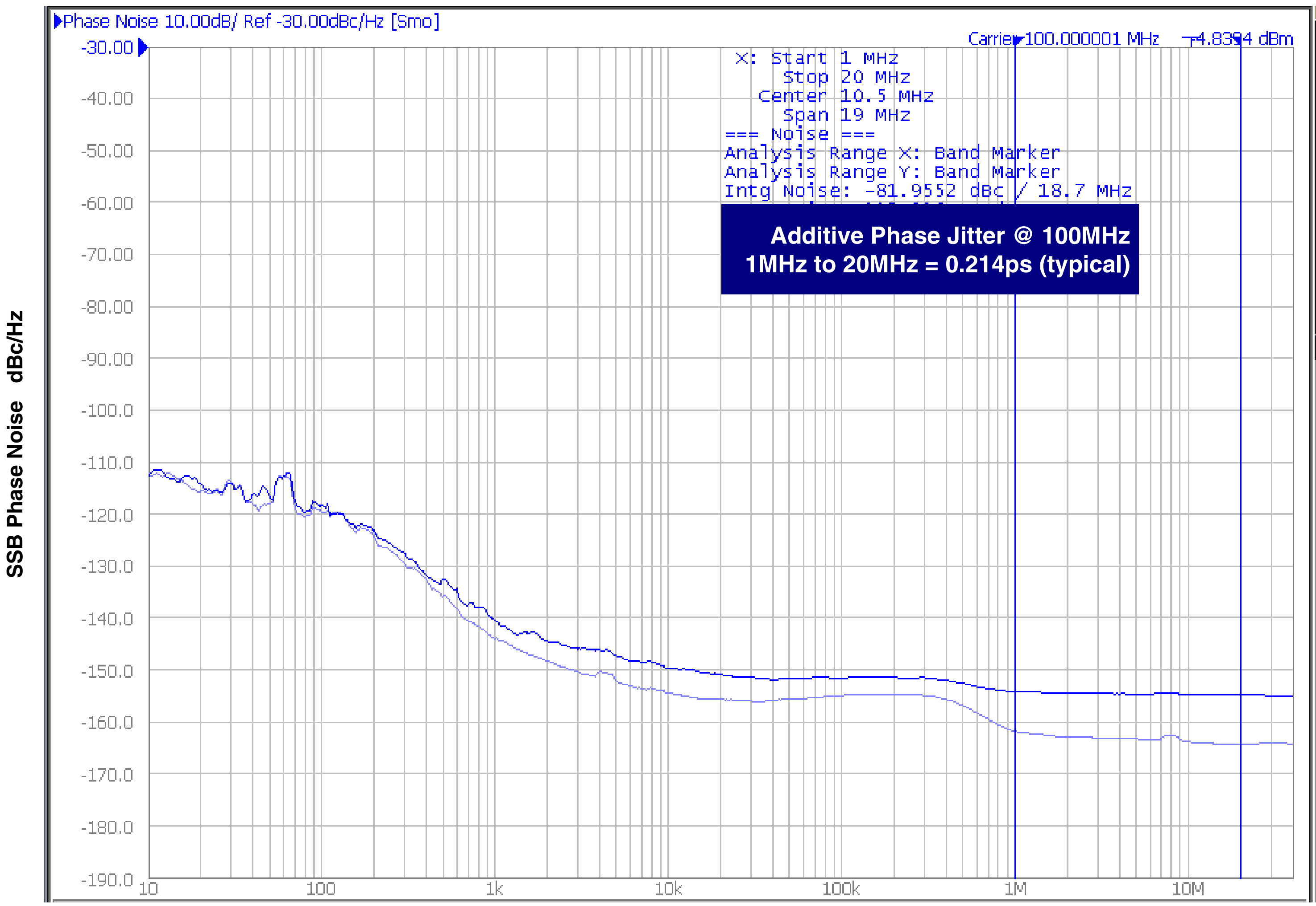
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	IN, nIN			500	MHz
f_{OUT}	Output Frequency	FSEL[1:0] = 00			500	MHz
		FSEL[1:0] = 01			250	MHz
		FSEL[1:0] = 10			125	MHz
		FSEL[1:0] = 11			62.5	MHz
f_{SCK}	I^2C Clock Frequency				400	kHz
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, measured with FSEL[1:0] = 00	f_{REF} = 100MHz, Integration Range: 1MHz – 20MHz		0.214	0.260	ps
		f_{REF} = 125MHz, Integration Range: 1MHz – 20MHz		0.168	0.208	ps
		f_{REF} =156.25, Integration Range: 1MHz – 20MHz		0.124	0.152	ps
t_{PD}	Propagation Delay; NOTE 1	FSEL[1:0] = 00	1.30	1.89	2.30	ns
		FSEL[1:0] = 01	210	2.60	2.80	ns
		FSEL[1:0] = 10	2.60	3.33	3.60	ns
		FSEL[1:0] = 11	2.90	3.73	4.00	ns
*t*sk(o)	Output Skew; NOTE 2, 3			28	60	ps
*t*sk(p)	Pulse Skew			27	50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4, 5				600	ps
odc	Output Duty Cycle; NOTE 6	Any Frequency		50		%
		at f_{REF} = 100MHz	48	50	52	%
		at f_{REF} = 125MHz	48	50	52	%
		at f_{REF} = 156.25MHz	48	50	52	%
t_{PDZ}	Output Enable and Disable Time; NOTE 7	Output enable/disable state from/to active/inactive			1	µs
t_R / t_F	Output Rise/ Fall Time	20% to 80%	200	422	650	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Part-to-part skew specification does not guarantee divider synchronization between devices
NOTE 6: If FSEL[1:0] = 00 (divide-by-one), the output duty cycle will depend on the input duty cycle.
NOTE 7: Measured from SDA rising edge of I^2C stop command.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

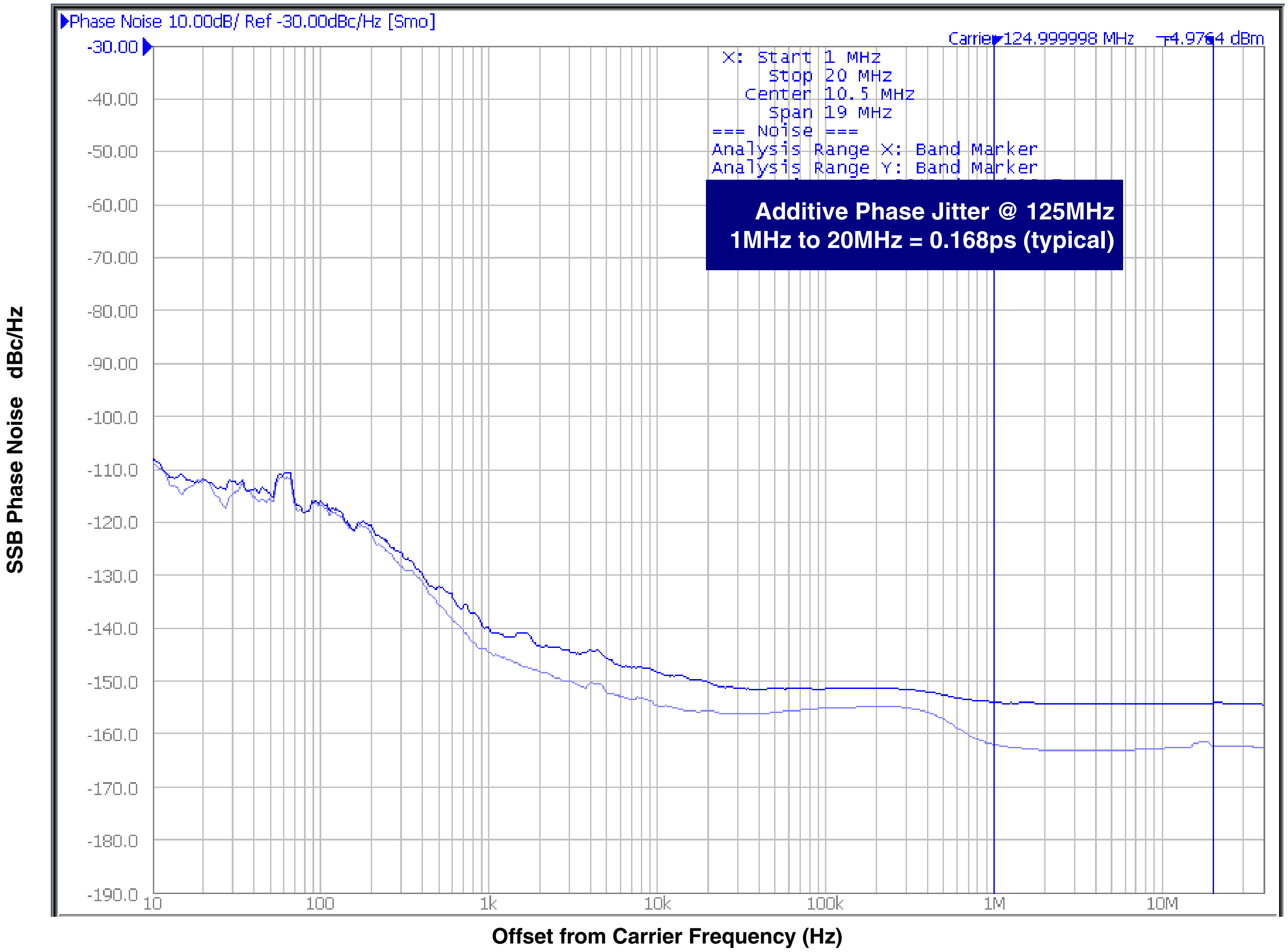
Additive Phase Jitter (100MHz)



Offset from Carrier Frequency (Hz)

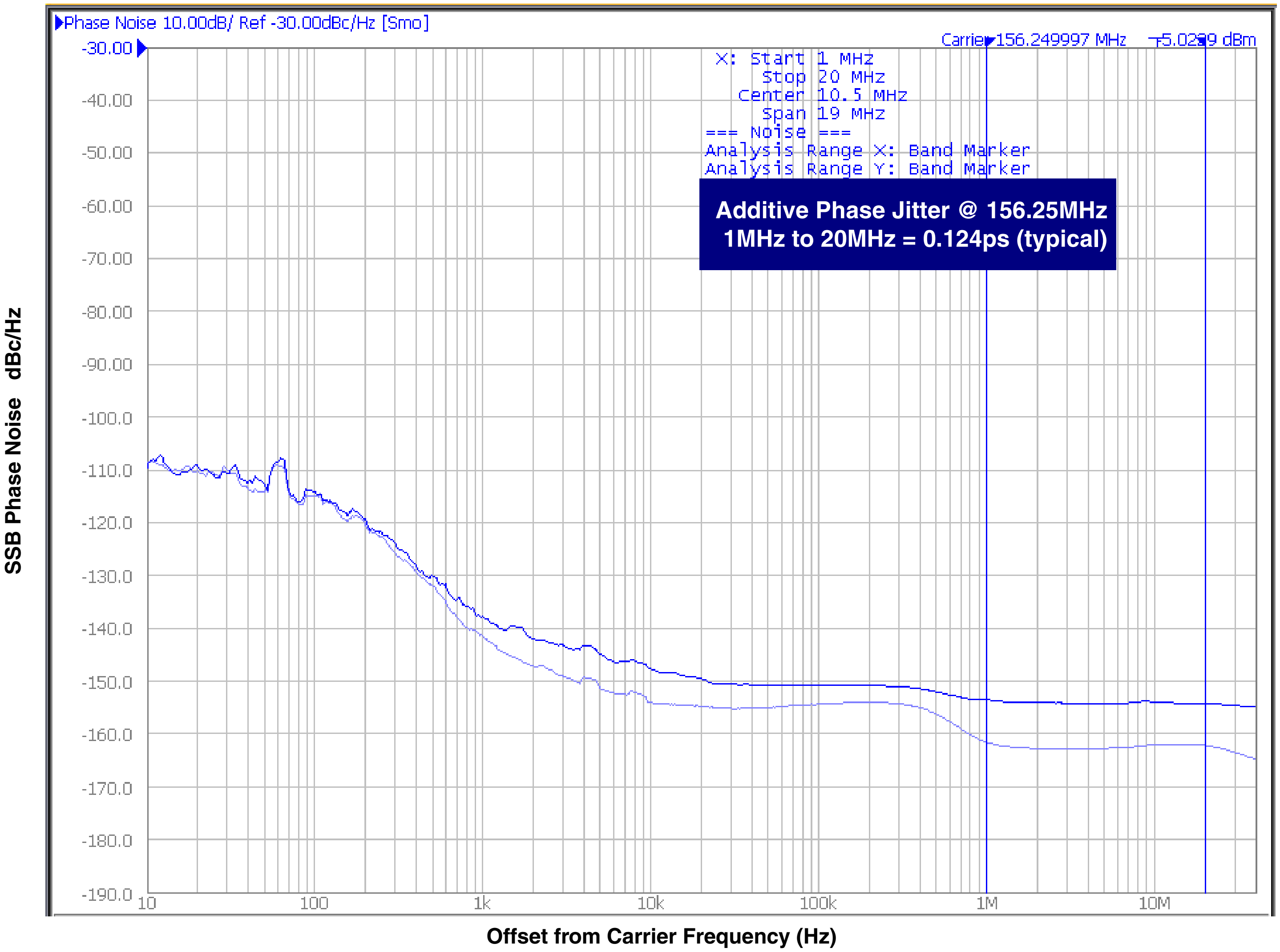
Measured using a Rohde & Schwarz SMA100 as the input source.

Additive Phase Jitter (125MHz)



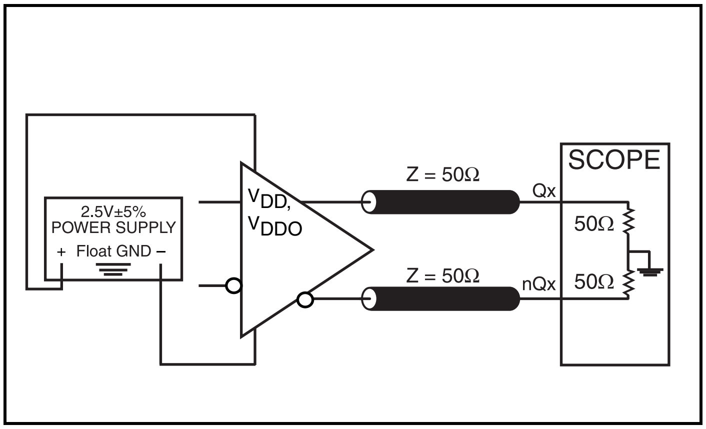
Measured using a Rohde & Schwarz SMA100 as the input source.

Additive Phase Jitter (156.25MHz)

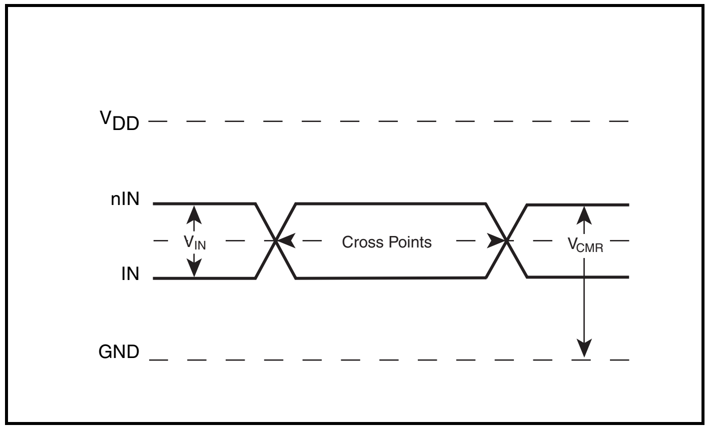


Measured using a Rohde & Schwarz SMA100 as the input source.

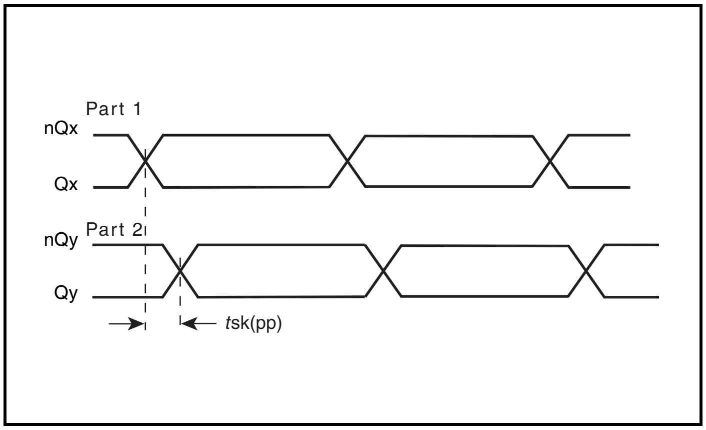
Parameter Measurement Information



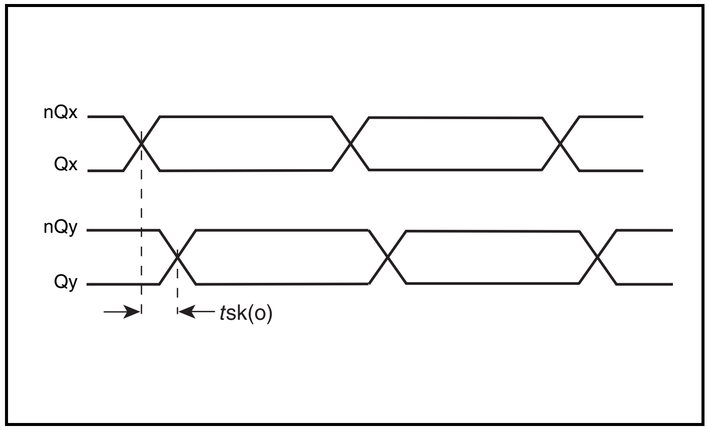
LVDS Output Load AC Test Circuit



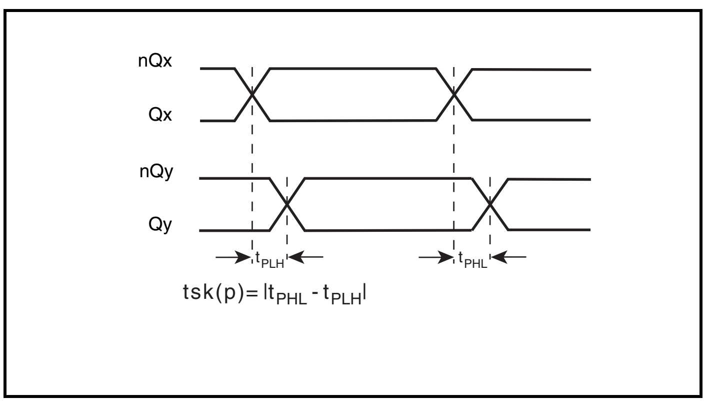
Differential Input Level



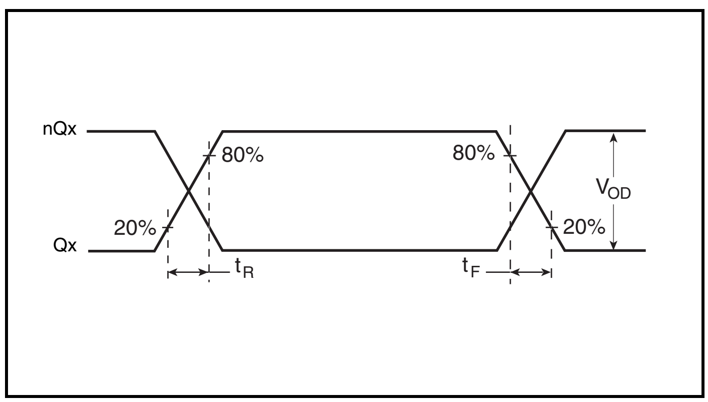
Part-to-Part Skew



Output Skew

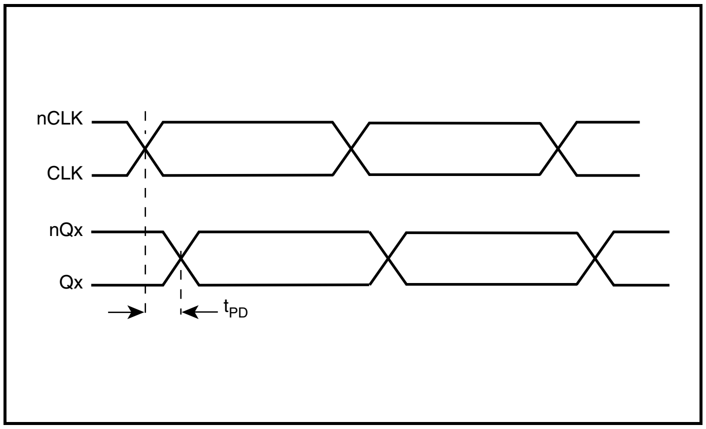


Pulse Skew

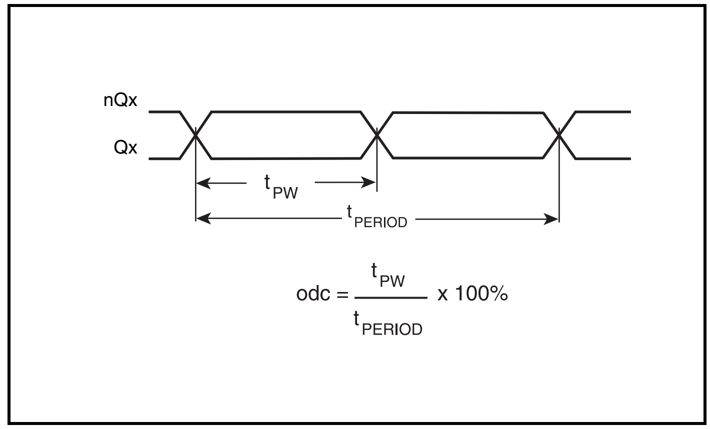


Output Rise/Fall Time

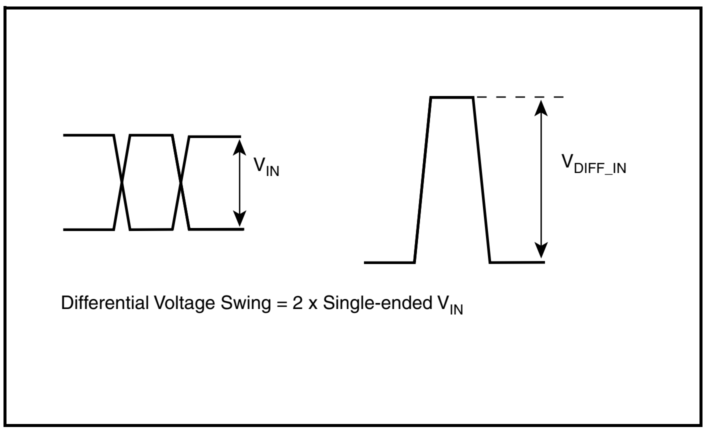
Parameter Measurement Information, continued



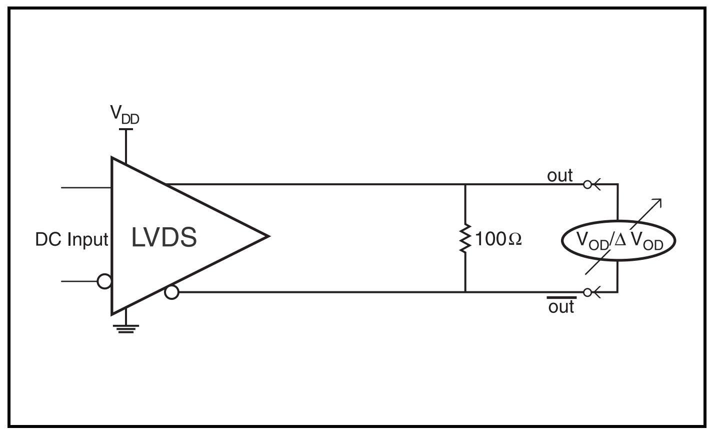
Propagation Delay



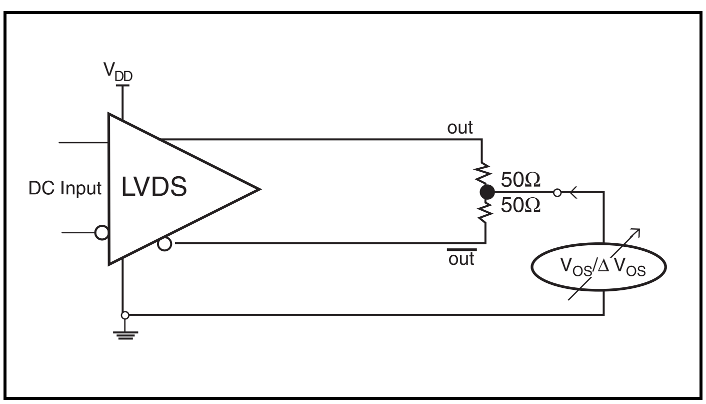
Output Duty Cycle/Pulse Width/Period



Single-Ended & Differential Input Voltage Swing



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both differential signals must meet the V_{IN} and V_{IH} input requirements. *Figures 4A to 4C to* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

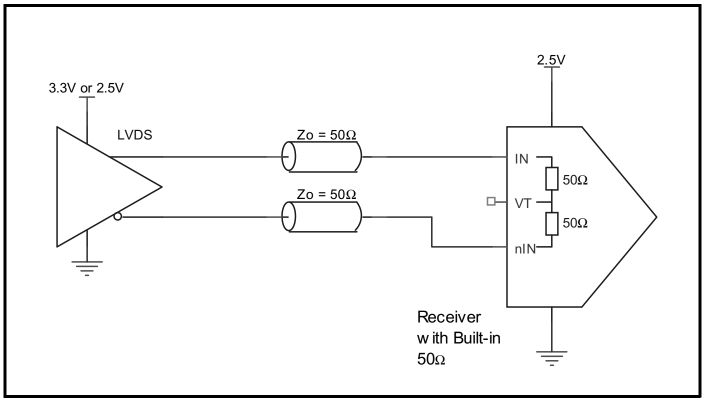


Figure 4A: IN/nIN Input with Built-In 50Ω driven by an LVDS Driver

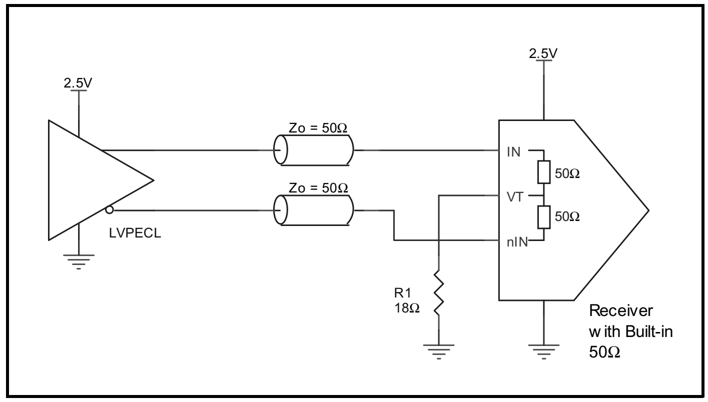


Figure 4C: IN/nIN Input with Built-In 50Ω driven by an LVPECL Driver

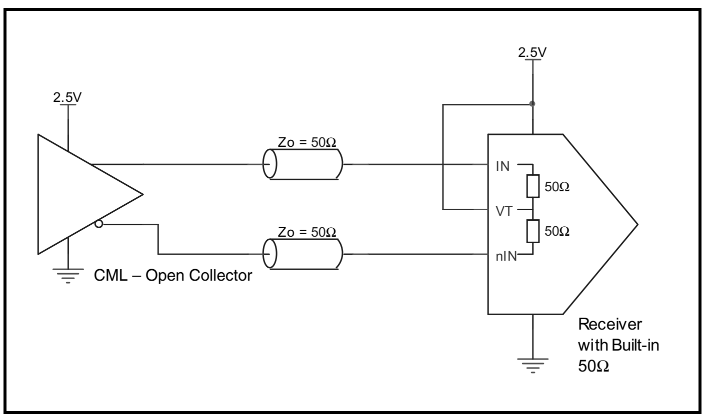


Figure 4B: IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 5. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

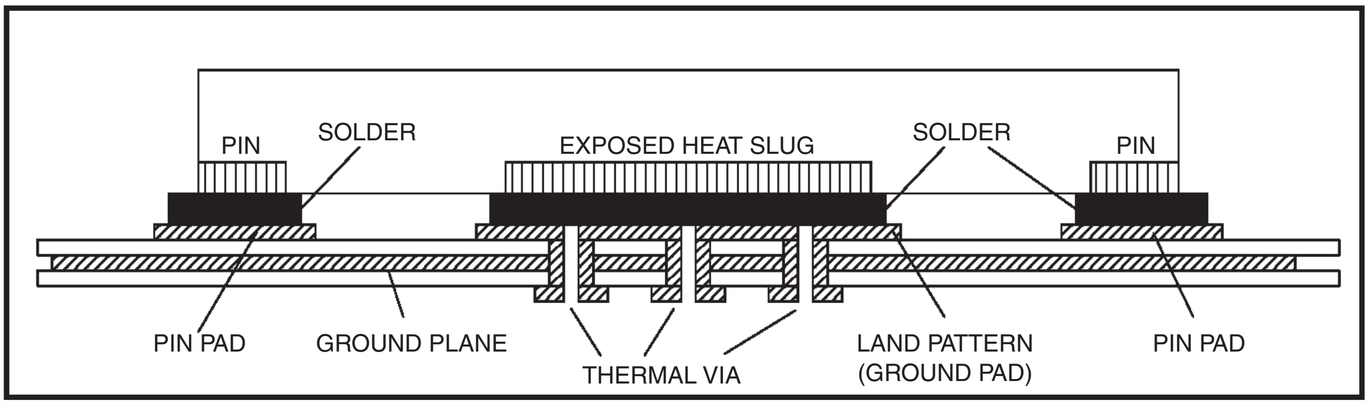


Figure 5: P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

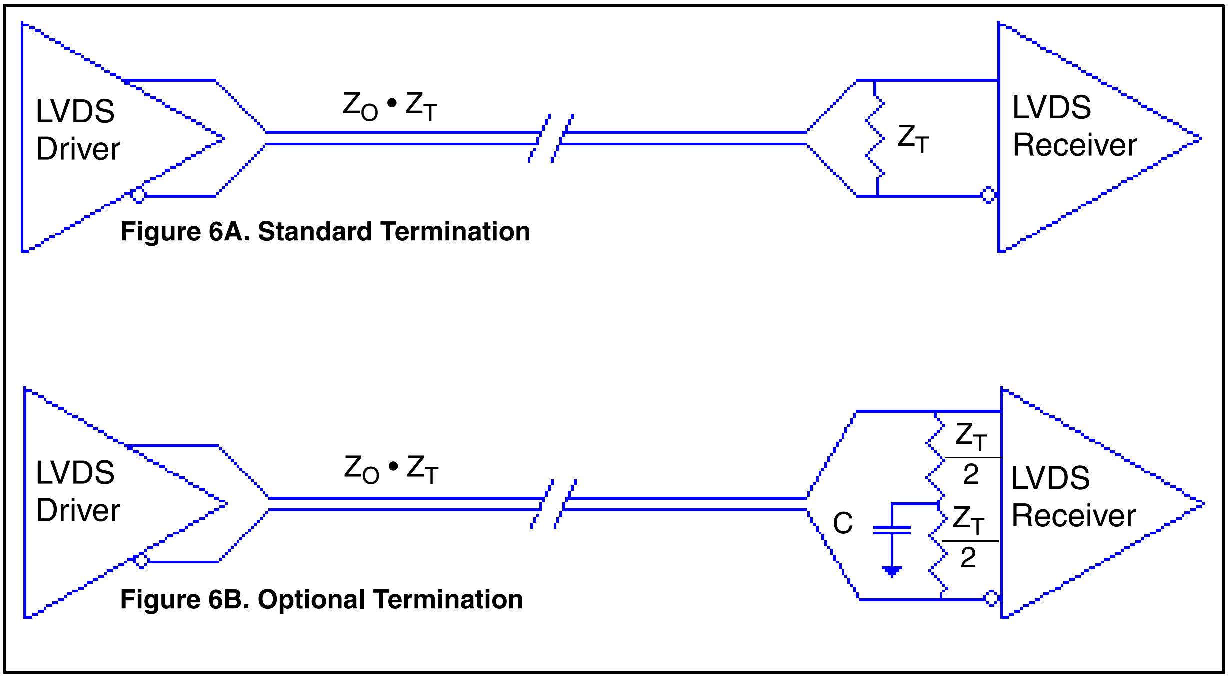
Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS874208I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS874208I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} *(I_{DD_MAX} + I_{DDO_MAX})= 2.625V * (15mA + 203mA) = **572.25mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX}$ = 4 * $(V_{IN\_MAX})^2$ / R_{T_MIN} = $(1.2V)^2$ / 80Ω = **72mW**

Total Power$_{\_MAX}$ = 572.25mW + 72mW = **644.25mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.644W * 33.1°C/W = 106.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

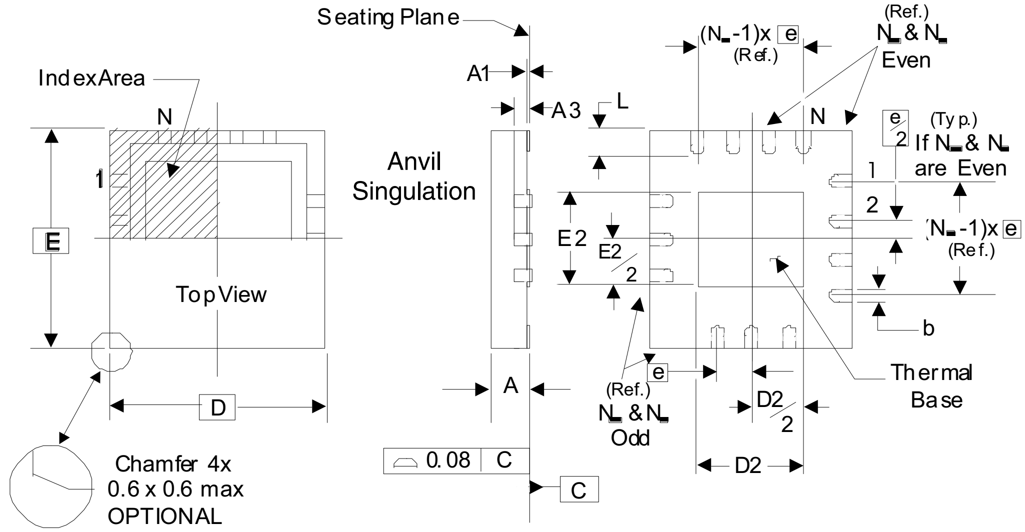
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

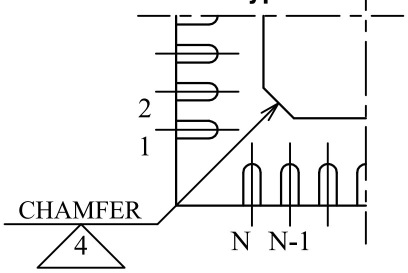
The transistor count for 874208I is: 7007

Package Outline and Package Dimensions

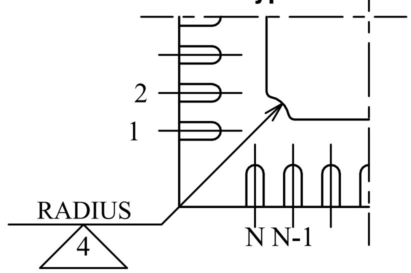
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874208BKILF	ICS74208BIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
874208BKILFT	ICS74208BIL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	4B	4	Updated Minimum and Maximum levels of R_{IN} and R_{IN}, D_{IFF} per PCN# N1408-01	9/18/14

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