General Description

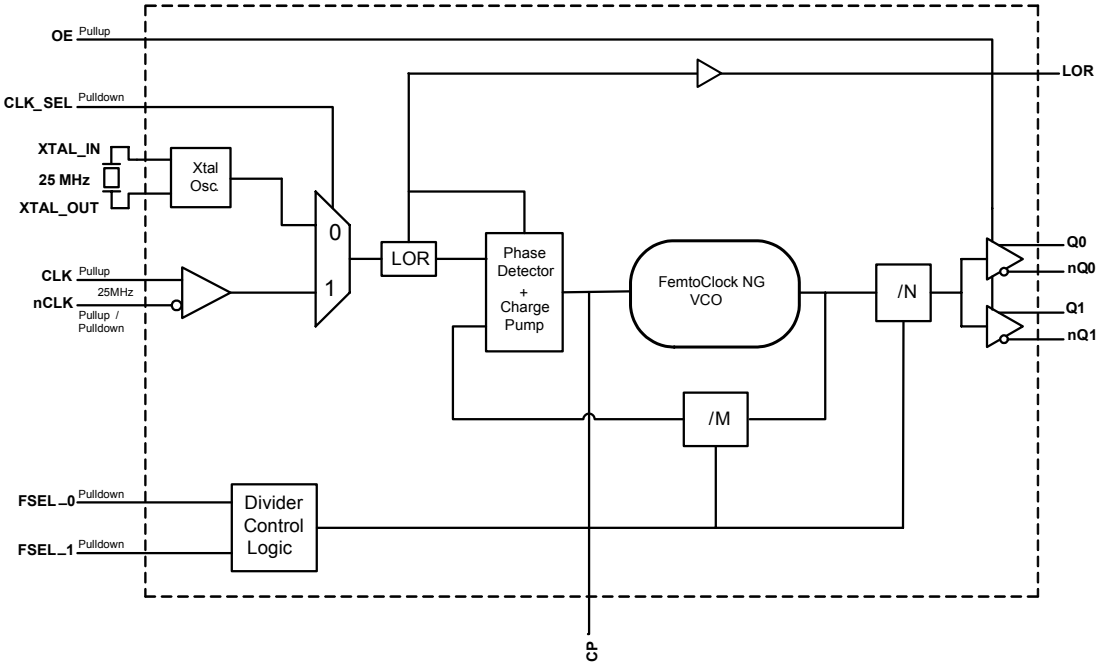
The ICS843N3960I is a LVPECL Clock Synthesizer. The ICS843N3960I can synthesize 100MHz, 125MHz, 156.25MHz and 212.5MHz from a single 25MHz crystal or reference clock.

Utilizing an external loop filter capacitor, the ICS843N3960I is capable of holdover mode when the main reference clock becomes unstable, making this ideal for redundant timing applications.

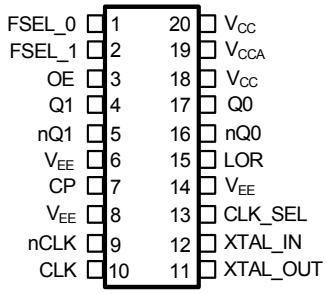
Features

- Fourth Generation FemtoClock® NG PLL technology
- Two differential LVPECL outputs
- Crystal oscillator interface designed for 12pF, 25MHz parallel resonant crystal
- CLK/nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- RMS phase jitter at 100MHz (12kHz – 20MHz): 0.510ps (max.)
- RMS phase jitter at 125MHz (12kHz – 20MHz): 0.575ps (max.)
- RMS phase jitter at 156.25MHz (12kHz – 20MHz): 0.504ps (max.)
- RMS phase jitter at 212.5MHz (12kHz – 20MHz): 0.512ps (max.)
- 3.3V power supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS843N3960I
20 Lead TSSOP, E-Pad
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	FSEL0, FSEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3A.
3	OE	Input	Pullup	Active HIGH output enable. LVCMOS/LVTTL interface levels.
4, 5	Q1, nQ1	Output		Differential output pair. 3.3V LVPECL interface levels.
6, 8, 14	V_{EE}	Power		Negative supply pins.
7	CP	Output		External loop filter capacitor output pin.
9	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
10	CLK	Input	Pulldown	Non-inverting differential clock input.
11, 12	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
13	CLK_SEL	Input	Pulldown	Input source control pin. LVCMOS/LVTTL interface levels. See Table 3C.
15	LOR	Output		Loss of Reference output pin. See LOR Functionality section.
16, 17	nQ0, Q0	Output		Differential output pair. 3.3V LVPECL interface levels.
18, 20	V_{CC}	Power		Core supply pins.
19	V_{CCA}	Power		Analog supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				3.5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	LOR			18		Ω

Function Tables

Table 3A. Output Frequency Table

FSEL_1	FSEL_0	M Divider	N Divider	Output Frequencies (MHz)
0 (default)	0 (default)	80	20	100
0	1	100	16	156.25
1	0	80	16	125
1	1	85	10	212.5

Table 3B. Output Enable & Clock Enable Function Table

Control Input	Output	
OE	Q0, nQ0	Q1, nQ1
0	High-Impedance	High-Impedance
1 (default)	Enabled	Enabled

Table 3C. CLK_SEL Function Table

Control Input	
CLK_SEL	Input Select
0 (default)	Crystal Interface
1	CLK, nCLK selected

LOR Functionality

The ICS843N3960I has a Loss of Reference (LOR) output that is used to indicate when the input reference has been lost, resulting in a logic high value on the LOR output. The LOR output is set high when the input clock experiences a single missed clock edge, or is completely lost. Once the input clock is recovered, the LOR output is set back to its low state.

The LOR output pin is deemed in be in a valid state 100ms after the device has been powered up and the FemtoClock ® NG VCO is phase locked.

NOTE: The LOR output pin will not accurately reflect the state of the input if the device is powered up without an input clock present or properly selected through the input mux interface (CLK_SEL). If this condition occurs, the device must be power cycled to reset the LOR circuitry.

Holdover Behavior

The ICS843N3960 has a holdover function. Holdover is accomplished by putting the charge pump in a high impedance state after the LOR output has been asserted high. This mode provides a stable output frequency even when the primary reference has been lost.

During holdover mode, the charge pump is placed in a high impedance state and the external charge pump capacitor, CP, is used to keep the internal VCO tuning voltage steady. Due to leakage current on this capacitor, the VCO accuracy, in terms of PPM, will vary over time. By using a 100uF capacitor on CP, the ICS843N3960I can achieve holdover accuracy of 275ppm over a ten second period. Note that holdover accuracy can only be achieved when the input reference clock has been stable for longer than 1ms.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	34.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.16	3.3	3.465	V
I_{CCA}	Analog Supply Current				16	mA
I_{EE}	Power Supply Current				122	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE	V_{CC} = V_{IN} = 3.465V			5	µA
		FSEL[1:0], CLK_SEL	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OE	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		FSEL[1:0], CLK_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	LOR	V_{CC} = 3.3V ± 5%, I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage	LOR	V_{CC} = 3.3V ± 5%, I_{OL} = 12mA			0.5	V

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as crossing point.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance				12	pF

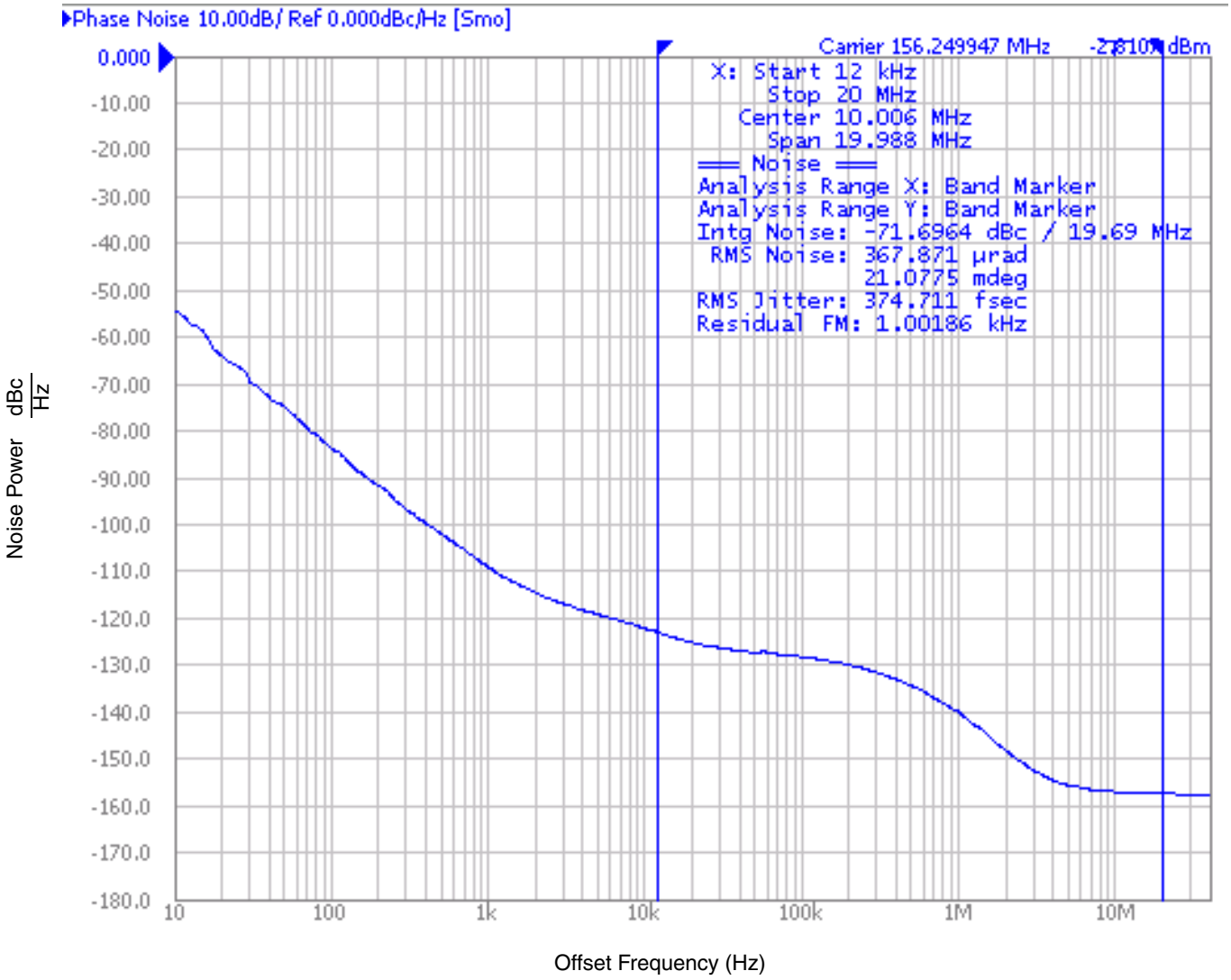
AC Electrical Characteristics

Table 6. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°

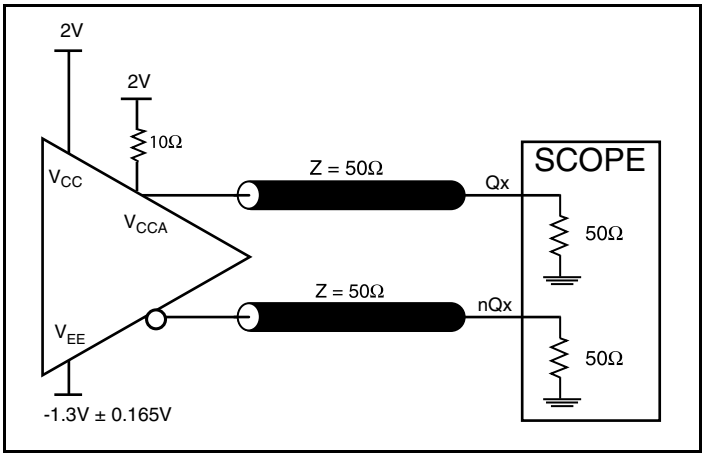
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FSEL_[0:1] = 00		100		MHz
		FSEL_[0:1] = 01		156.25		MHz
		FSEL_[0:1] = 10		125		MHz
		FSEL_[0:1] = 11		212.5		MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	100MHz, Integration Range: 12kHz – 20MHz		0.331	0.510	ps
		125MHz, Integration Range: 12kHz – 20MHz		0.300	0.575	ps
		156.25MHz, Integration Range: 12kHz – 20MHz		0.375	0.504	ps
		212.5MHz, Integration Range: 12kHz – 20MHz		0.300	0.512	ps
tsk(o)	Output Skew; NOTE 2, 3				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	285		600	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

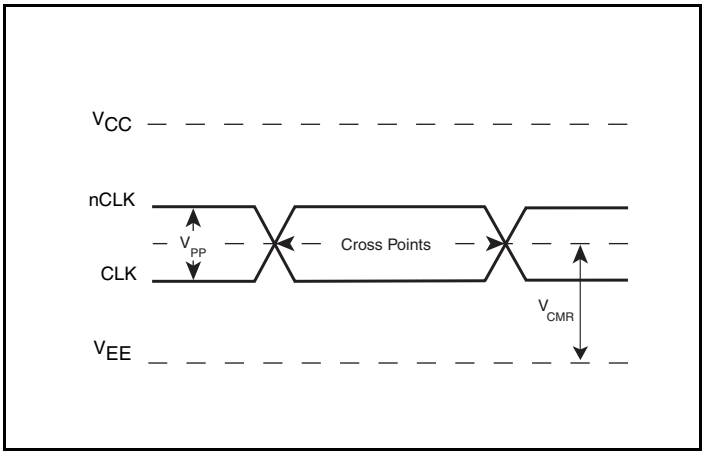
Typical Phase Noise at 156.25MHz



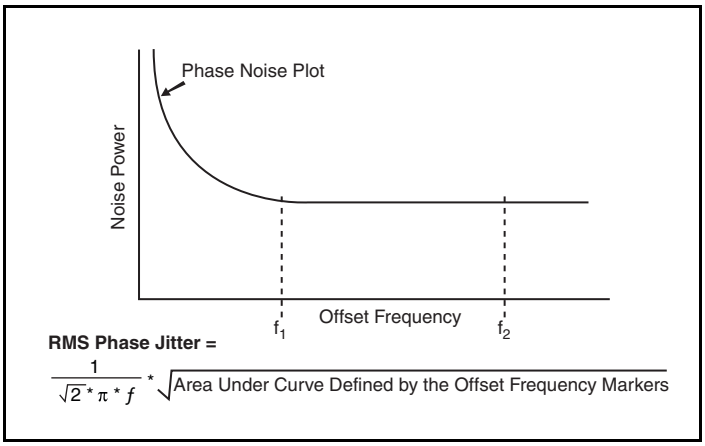
Parameter Measurement Information



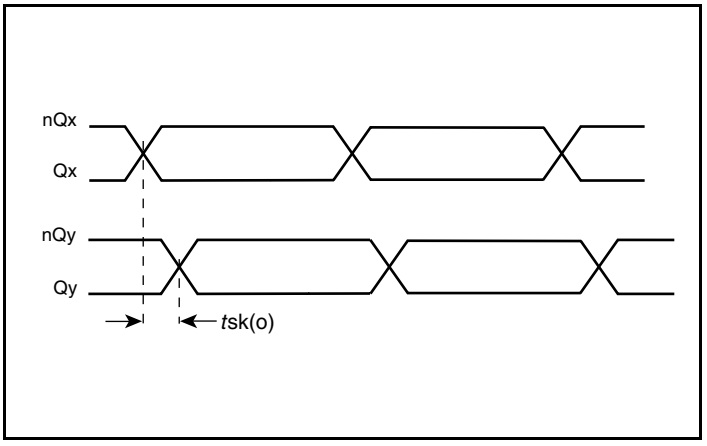
3.3V LVPECL Output Load AC Test Circuit



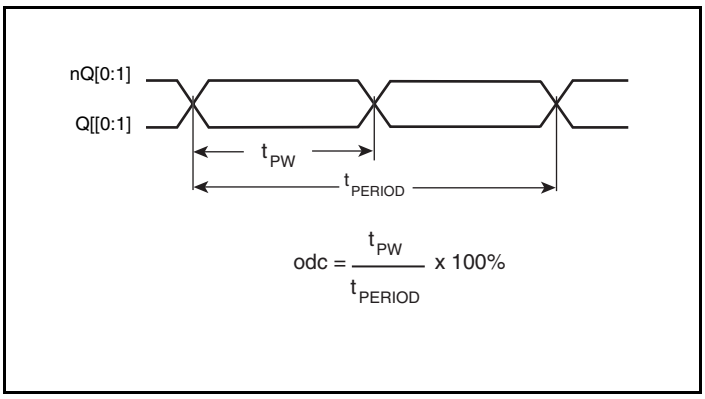
Differential Input Levels



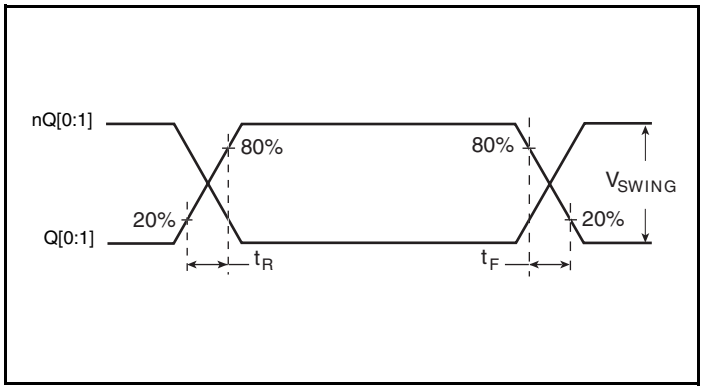
RMS Phase Jitter



Output Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

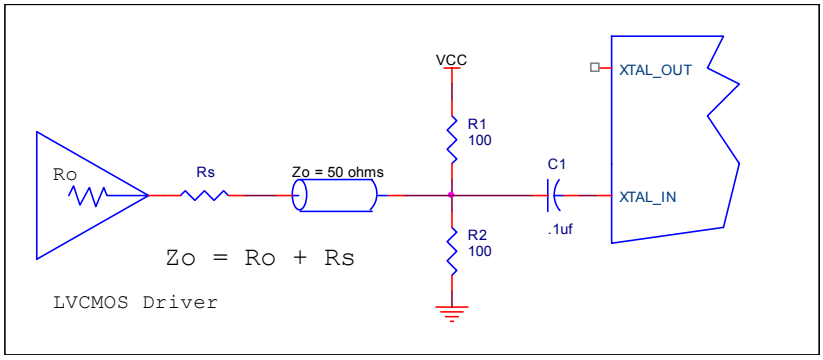


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

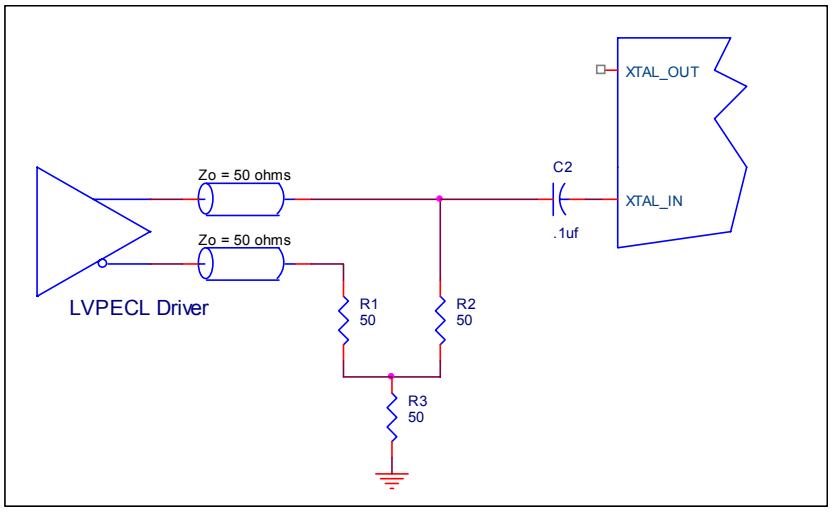


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. If the driver is from another vendor, use their termination recommendation.

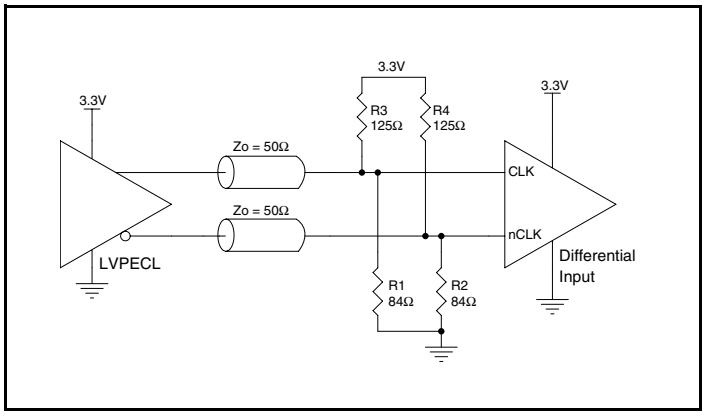


Figure 2A. CLK/nCLK Input Driven by a 3.3V HCSL Driver

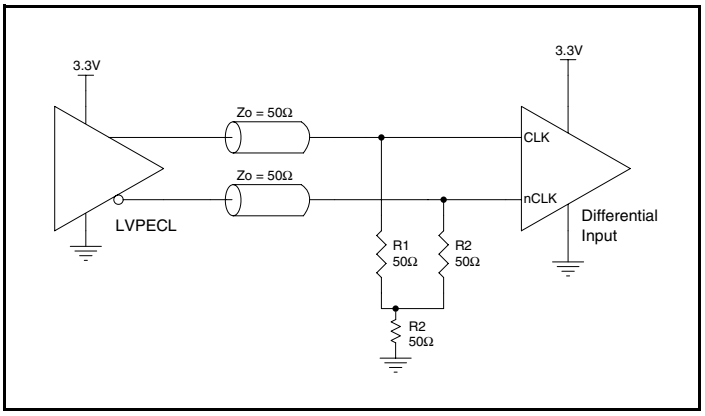


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

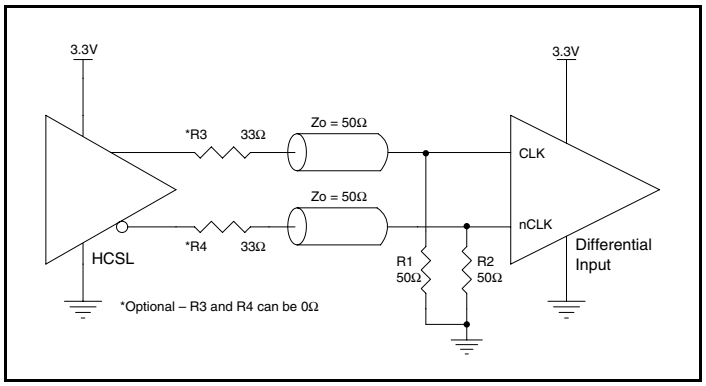


Figure 2C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

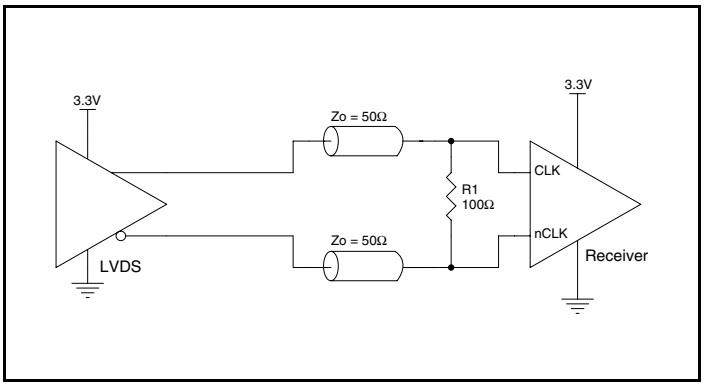


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

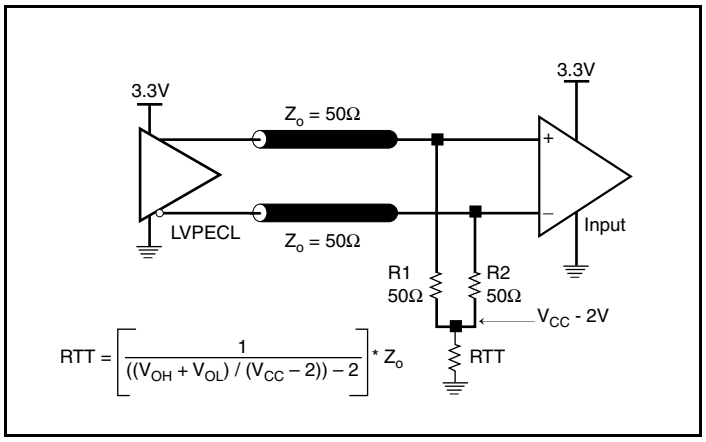


Figure 3A. 3.3V LVPECL Output Termination

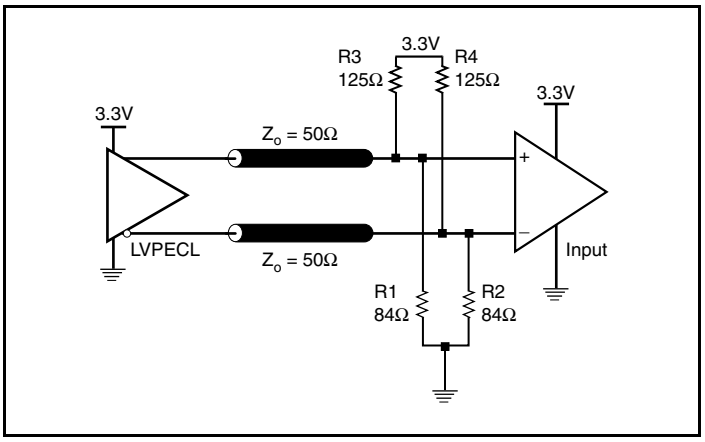


Figure 3B. 3.3V LVPECL Output Termination

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

The unused LVCMOS output can be left floating. We recommend that there is no trace attached.

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

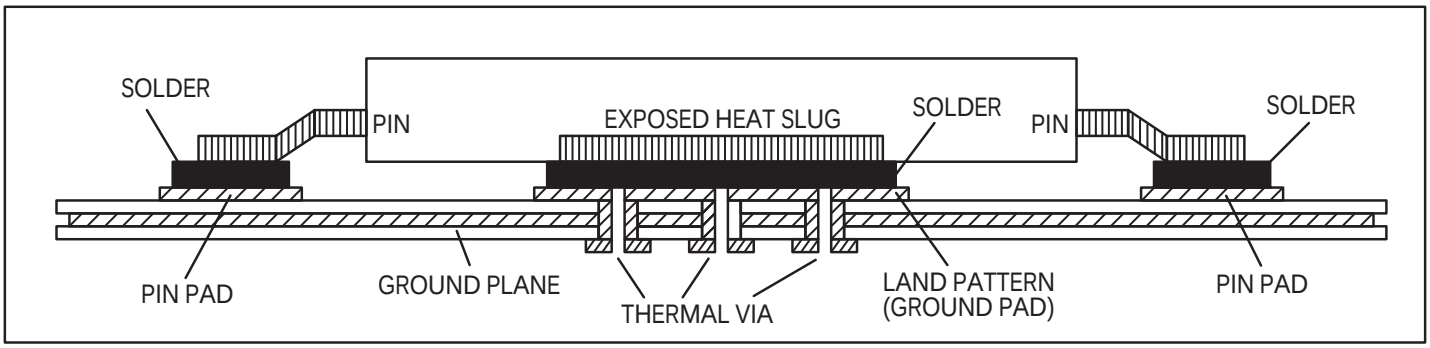


Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Example

Figure 5 shows an example ICS843N3960I application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. Load caps C1 = C2 = 4pF are recommended for frequency accuracy, but these may be adjusted for different board layouts. If different crystal types are used, please consult IDT for recommendations.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite bead, 10uf and 0.1uF capacitors connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. If AC coupling for PECL levels is required to the CLK, nCLK and/or Q0 and Q1 outputs, please refer to the IDT application note, Termination - 3.3V PECL

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843N3960I provides separate VCC and VCCA power supplies to isolate any high switching noise from coupling into the internal PLL.

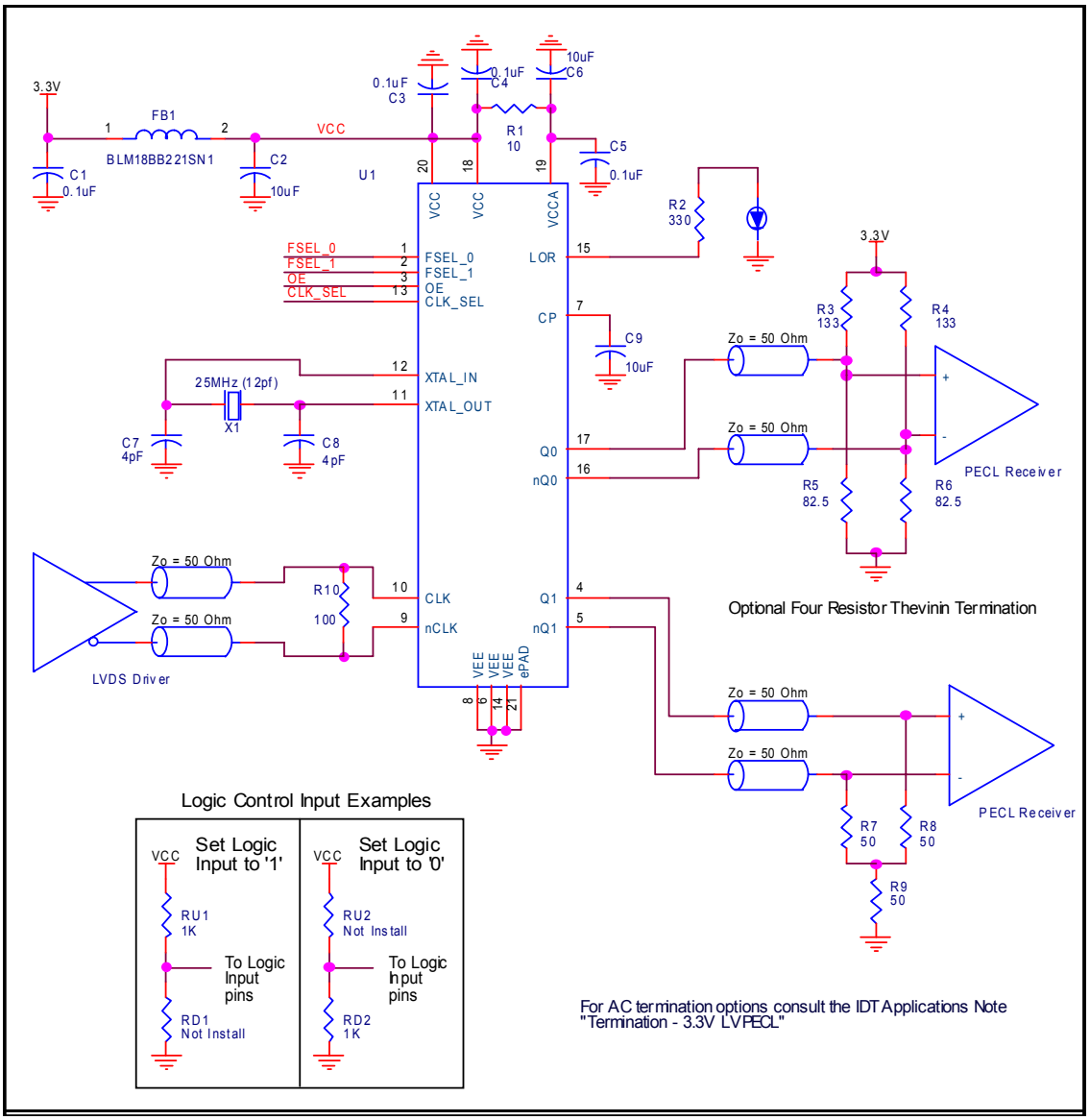


Figure 5. ICS843N3960I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843N3960I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843N3960I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 122mA = **422.73mW**
- Power $(outputs)_{MAX}$ = **30.0mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.0mW = **60.0mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 422.73mW + 60.0mW = **482.73mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 34.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.483W * 34.3°C/W = 101.56°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead TSSOP, E-Pad Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	34.3°C/W	29.9°C/W	28.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*

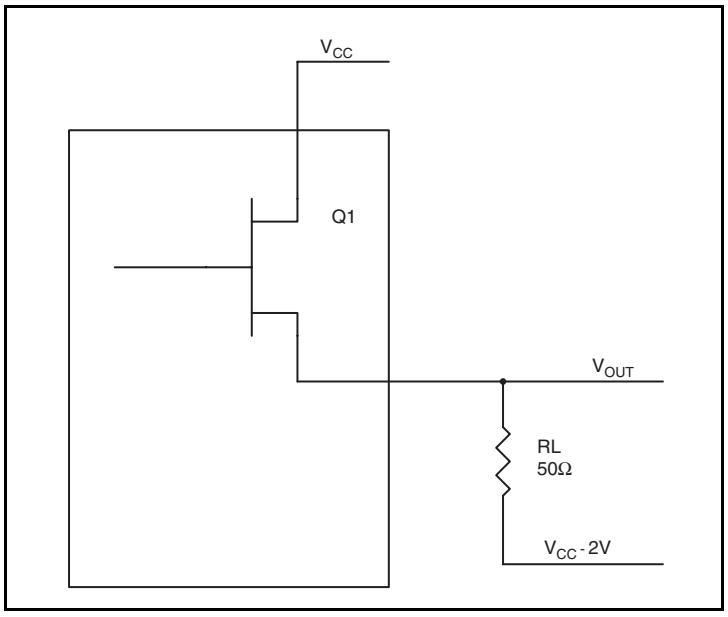


Figure 6. LVPECL Driver Circuit and Termination

To calculate power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V. These are typical calculations. (NOTE: Below are Final release estimation values.)

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} –0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 0.9V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP, E-Pad

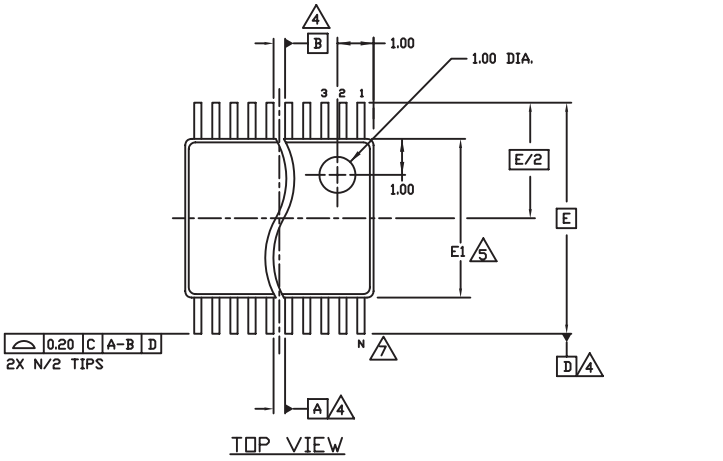
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	34.3°C/W	29.9°C/W	28.4°C/W

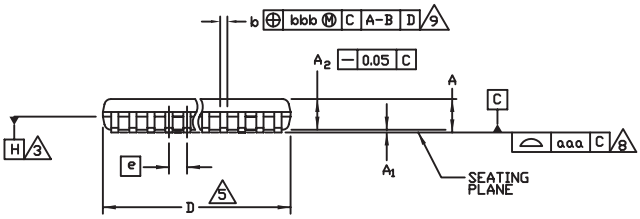
Transistor Count

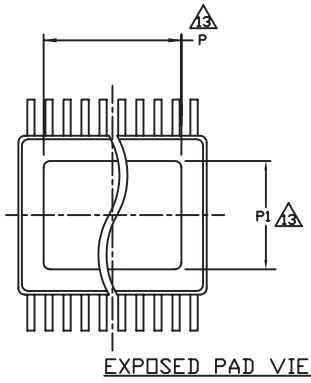
The transistor count for ICS843N3960I is: 24,851

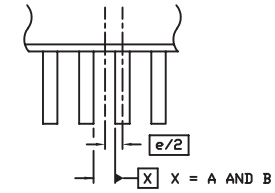
Package Outline and Package Dimensions

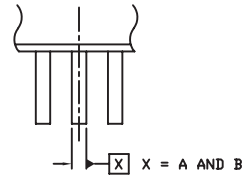
Package Outline - G Suffix for 20 Lead TSSOP, E-Pad

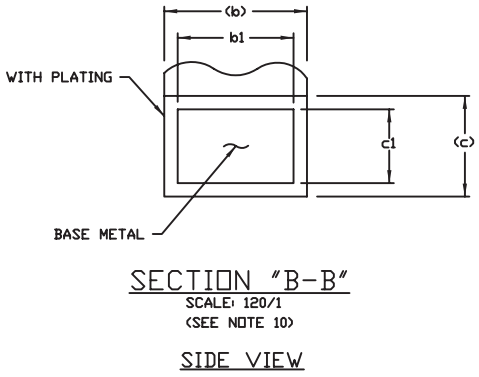


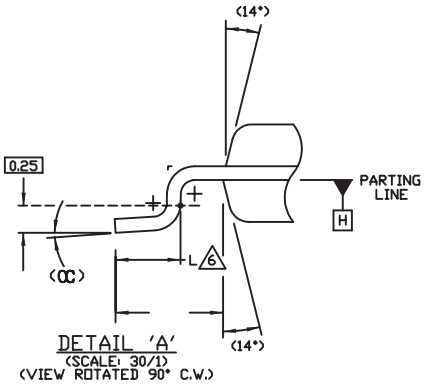












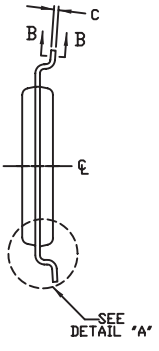


Table 8. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		20	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	6.40	6.50	6.60
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P			4.2
P1			3.0
α	0°		8°
ααα		0.076	
bbb		0.10	

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843N3960DGILF	ICS3N3960DIL	“Lead-Free” 20 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
843N3960DGILFT	ICS3N3960DIL	“Lead-Free” 20 Lead TSSOP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	Block Diagram - deleted LOR label.	9/24/2012
		1	Features Section - changed “typical” to “max.”	
	T1	2	Pin Description Table - corrected reference for LOR, Pin 15.	
	T4B	4	Table 4B - LVCMOS DC Characteristics Table - Deleted “NOTE 1” from V_{OH}/V_{OL}; corrected typo in V_{OL} test condition from -12mA to 12mA; added test condition to I_{IL}.	
	T6	6	AC Characteristics Table - changed f_{OUT} (test condition 01) from 125MHz to 156.25MHz; (test condition 10) from 156.25MHz to 125MHz.	

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