

## General Description

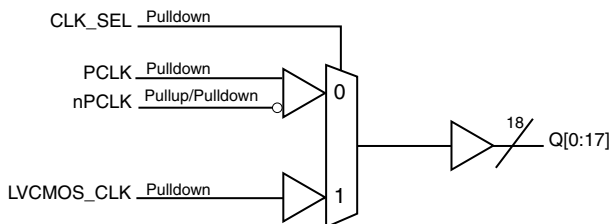
The 83940I-01 is a low skew, 1-to-18 LVPECL-to-LVCMOS/ LVTTL Fanout Buffer. The 83940I-01 has two selectable clock inputs. The PCLK, nPCLK pair can accept LVPECL or SSTL input levels. The single-ended clock input accepts LVCMOS or LVTTL input levels.

The 83940I-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the 83940I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

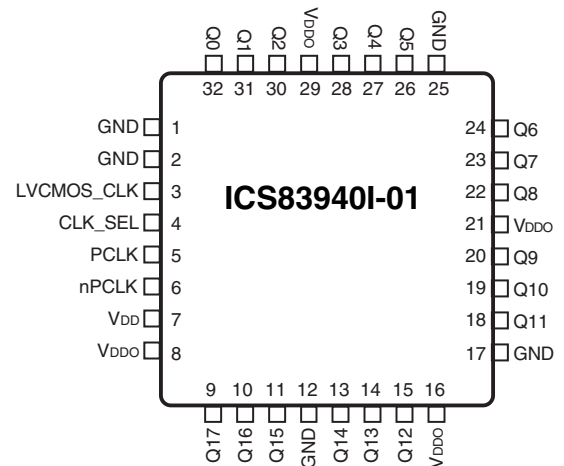
## Features

- Eighteen LVCMOS/LVTTL outputs, 23Ω typical output impedance
- Selectable LVCMOS\_CLK or LVPECL clock inputs
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, SSTL
- LVCMOS\_CLK supports the following input types: LVCMOS or LVTTL
- Maximum output frequency: 175MHz
- Additive phase jitter, RMS: 0.108ps (typical), 3.3V/3.3V
- Output skew: 115ps (maximum)
- Part-to-part skew: 800ps (maximum), 3.3V/3.3V
- Operating supply modes:
  - Core/Output 3.3V/3.3V
  - 3.3V/2.5V
  - 2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



**32-Lead LQFP**  
**7mm x 7mm x 1.4mm package body**  
**Y Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Power supply ground.
3	LVC MOS_CLK	Input	Pulldown	Single-ended clock input. LVC MOS/LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects LVC MOS_CLK input. When LOW, selects PCLK, nPCLK inputs. LVC MOS / LVTTL interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7	$V_{DD}$	Power		Power supply pin.
8, 16, 21, 29	$V_{DDO}$	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVC MOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output)			9		pF
$R_{OUT}$	Output Impedance		17	23	28	$\Omega$

## Function Tables

**Table 3A. Clock Select Function Table**

Control Input	Clock	
CLK_SEL	PCLK, nPCLK	LVC MOS_CLK
0	Selected	De-selected
1	De-selected	Selected

**Table 3B. Clock Input Function Table**

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVC MOS_CLK	PCLK	nPCLK	Q[0:17]		
0	–	0	1	LOW	Differential to Single-Ended	Non-Inverting
0	–	1	0	HIGH	Differential to Single-Ended	Non-Inverting
0	–	0	Biased; NOTE 1	LOW	Single-Ended to Single-Ended	Non-Inverting
0	–	1	Biased; NOTE 1	HIGH	Single-Ended to Single-Ended	Non-Inverting
0	–	Biased; NOTE 1	0	HIGH	Single-Ended to Single-Ended	Inverting
0	–	Biased; NOTE 1	1	LOW	Single-Ended to Single-Ended	Inverting
1	0	–	–	LOW	Single-Ended to Single-Ended	Non-Inverting
1	1	–	–	HIGH	Single-Ended to Single-Ended	Non-Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels*.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	3.6V
Inputs, $V_I$	-0.3V to $V_{DD} + 0.3V$
Outputs, $V_O$	-0.3V to $V_{DDO} + 0.3V$
Input Current, $I_{IN}$	$\pm 20\text{mA}$
Package Thermal Impedance, $\theta_{JA}$	53.5°C/W (0 mps)
Storage Temperature, $T_{STG}$	-40°C to 125°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				26	mA
$I_{DDO}$	Output Supply Current	No Load			28	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				25	mA
$I_{DDO}$	Output Supply Current	No Load			26	mA

**Table 4C. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				26	mA
$I_{DDO}$	Output Supply Current	No Load			26	mA

**Table 4D. LVCMOS DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVC MOS_CLK	$V_{DD} = 3.3V$ or $2.5V$		$V_{DD} + 0.3$	V
		CLK_SEL				
$V_{IL}$	Input Low Voltage	LVC MOS_CLK	$V_{DD} = 3.3V$ or $2.5V$	-0.3	1.3	V
		CLK_SEL	$V_{DD} = 3.3V$ or $2.5V$	-0.3	0.8	V
$I_{IH}$	Input High Current	CLK_SEL, LVC MOS_CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK_SEL, LVC MOS_CLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-5	$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1		$V_{DDO} = 3.465V$	2.8		V
			$V_{DDO} = 2.625V$	2.1		V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{DDO} = 3.465V$ or $2.65V$		0.55	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section, *Output Load Test Circuit diagram*.

**Table 4E. LVPECL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK, nPCLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	PCLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-10	$\mu\text{A}$
		nPCLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-150	$\mu\text{A}$
$I_{IN}$	Input Current				$\pm 200$	$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage		500		1000	mV
$V_{CMR}$	Common Mode Input Voltage; NOTE 1		$V_{DD} - 1.4$		$V_{DD} - 0.6$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

**Table 4F. LVPECL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK, nPCLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	PCLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-10	$\mu\text{A}$
		nPCLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$		-150	$\mu\text{A}$
$I_{IN}$	Input Current				$\pm 200$	$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage		300		1000	mV
$V_{CMR}$	Common Mode Input Voltage; NOTE 1		$V_{DD} - 1.4$		$V_{DD} - 0.6$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{OUT}$	Output Frequency				175	MHz	
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.6		3.0	ns
		LVCOSMOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.8		3.0	ns
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.6		3.3	ns
		LVCOSMOS_CLK; NOTE 2, 5	$f > 150MHz$	1.8		3.2	ns
$f_{jit}$	Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	PCLK, nPCLK	155.52MHz, Integration Range: 12kHz – 20MHz		0.145		ps
		LVCOSMOS_CLK			0.108		ps
$t_{sk(o)}$	Output Skew; NOTE 3, 5	Measured on the Rising Edge @ $V_{DDO}/2$			115	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$			1.4	ns
		LVCOSMOS_CLK	$f \leq 150MHz$			1.2	ns
	Part-to-Part Skew; NOTE 6	PCLK/nPCLK	$f > 150MHz$			1.7	ns
		LVCOSMOS_CLK	$f > 150MHz$			1.4	ns
	Part-to-Part Skew; NOTE 4, 5	PCLK/nPCLK	Measured on the Rising Edge @ $V_{DDO}/2$			975	ps
		LVCOSMOS_CLK				800	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		800	ps	
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%	

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at 150MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

**Table 5B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{OUT}$	Output Frequency				175	MHz	
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.7	3.2	ns	
		LVCOSMOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.7	3.0	ns	
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.6	3.4	ns	
		LVCOSMOS_CLK; NOTE 2, 5	$f > 150MHz$	1.8	3.3	ns	
$f_{jit}$	Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	PCLK, nPCLK	155.52MHz, Integration Range: 12kHz – 20MHz	0.199		ps	
		LVCOSMOS_CLK		0.137		ps	
$t_{sk(o)}$	Output Skew; NOTE 3, 5	Measured on the Rising Edge @ $V_{DDO}/2$			150	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$		1.5	ns	
		LVCOSMOS_CLK	$f \leq 150MHz$		1.3	ns	
	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150MHz$		1.8	ns	
		LVCOSMOS_CLK	$f > 150MHz$		1.5	ns	
	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on the Rising Edge @ $V_{DDO}/2$			975	ps
		LVCOSMOS_CLK				875	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		800	ps	
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%	

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at 150MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

**Table 5C. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{OUT}$	Output Frequency				175	MHz	
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.2	3.8	ns	
		LVCOSMOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.5	3.2	ns	
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.5	3.7	ns	
		LVCOSMOS_CLK; NOTE 2, 5	$f > 150MHz$	2.0	3.6	ns	
$\sigma_{jit}$	Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	PCLK, nPCLK	155.52MHz, Integration Range: 12kHz – 20MHz	0.323		ps	
		LVCOSMOS_CLK		0.116		ps	
$t_{sk(o)}$	Output Skew; NOTE 3, 5	Measured on the Rising Edge @ $V_{DDO}/2$			150	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$		2.6	ns	
		LVCOSMOS_CLK	$f \leq 150MHz$		1.7	ns	
	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150MHz$		2.2	ns	
		LVCOSMOS_CLK	$f > 150MHz$		1.7	ns	
	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on the Rising Edge @ $V_{DDO}/2$			1.2	ns
		LVCOSMOS_CLK				1	ns
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		800	ps	
odc	Output Duty Cycle	$f \leq 150MHz$	43		57	%	

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at 150MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

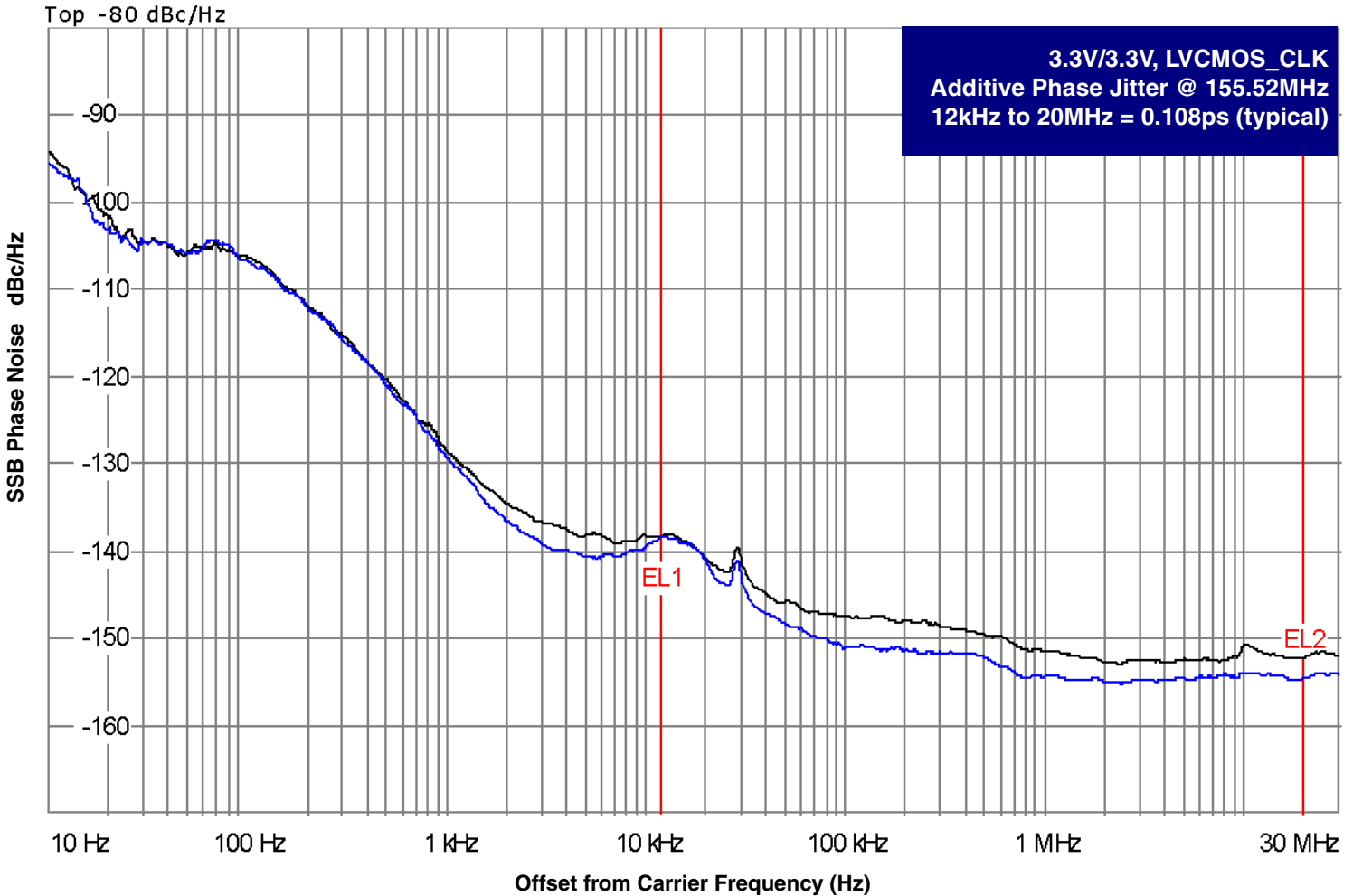
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .



## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

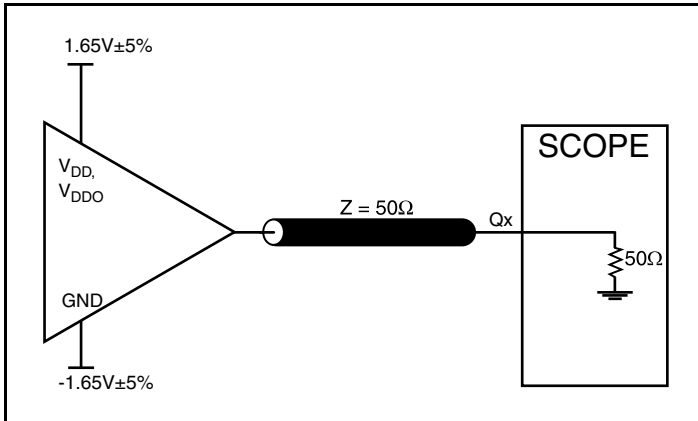
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



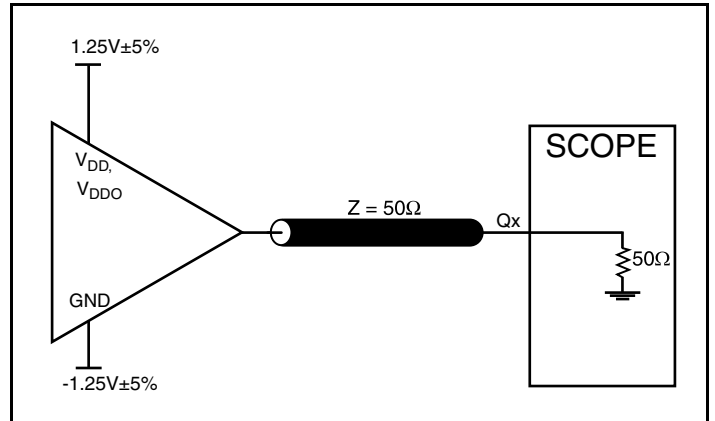
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator, "SMA 100A 9kHz – 6GHz Low Noise Signal Generator" as external input to an Agilent 8133A 3GHz Pulse Generator".

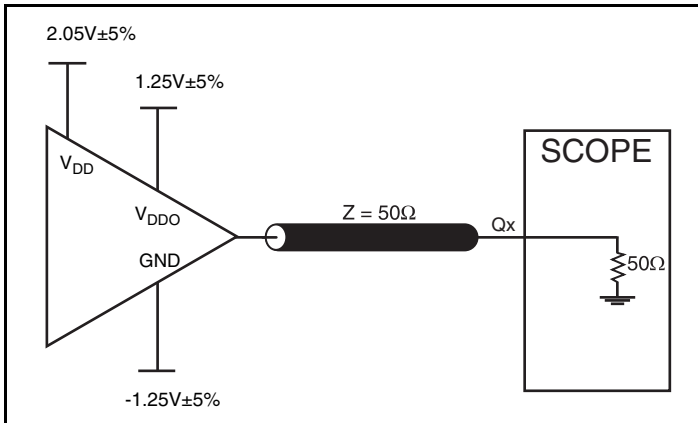
## Parameter Measurement Information



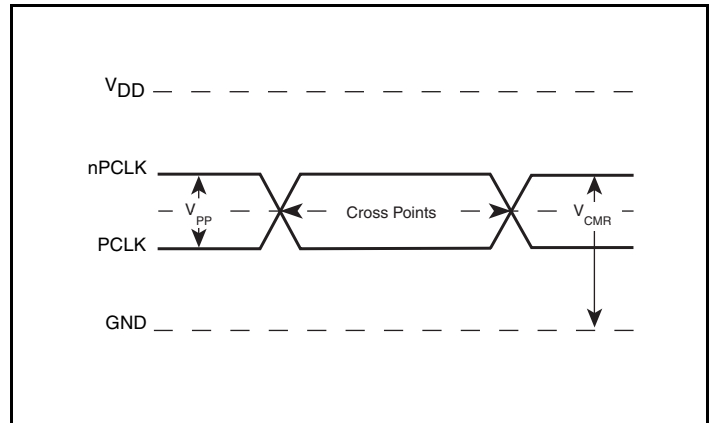
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



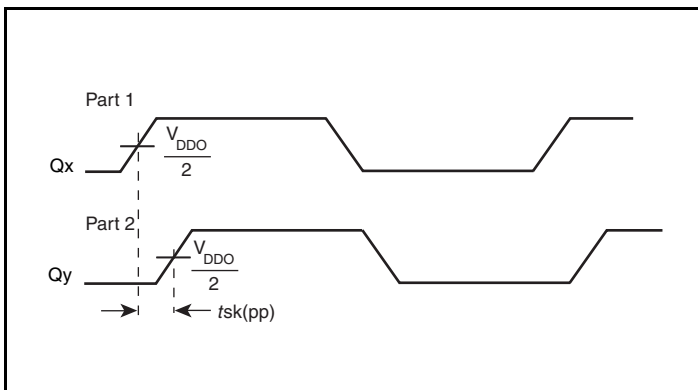
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



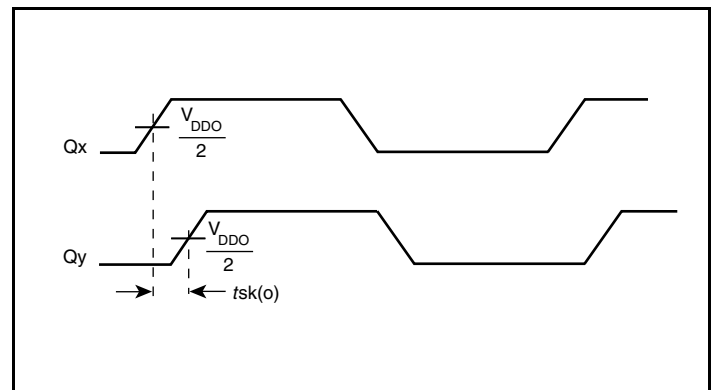
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



Differential Input Level

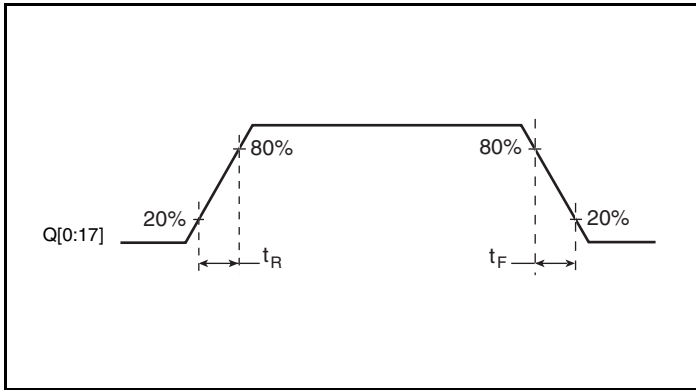


Part-to-Part Skew

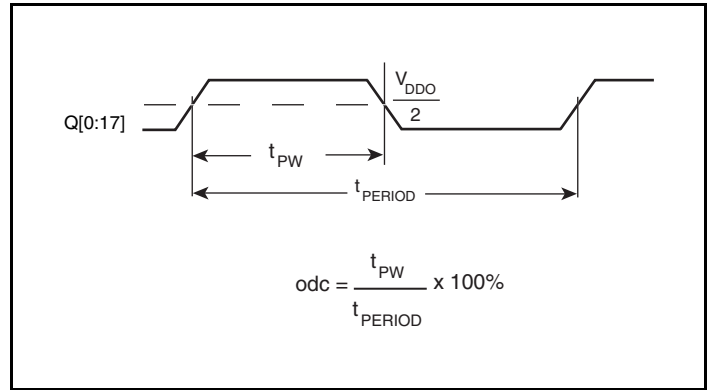


Output Skew

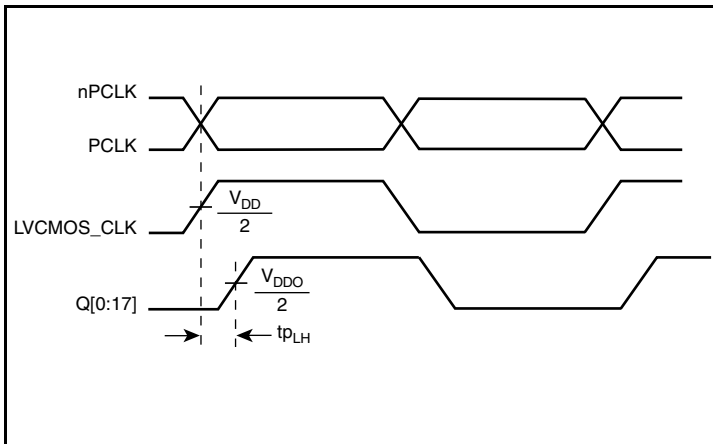
Parameter Measurement Information, continued



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

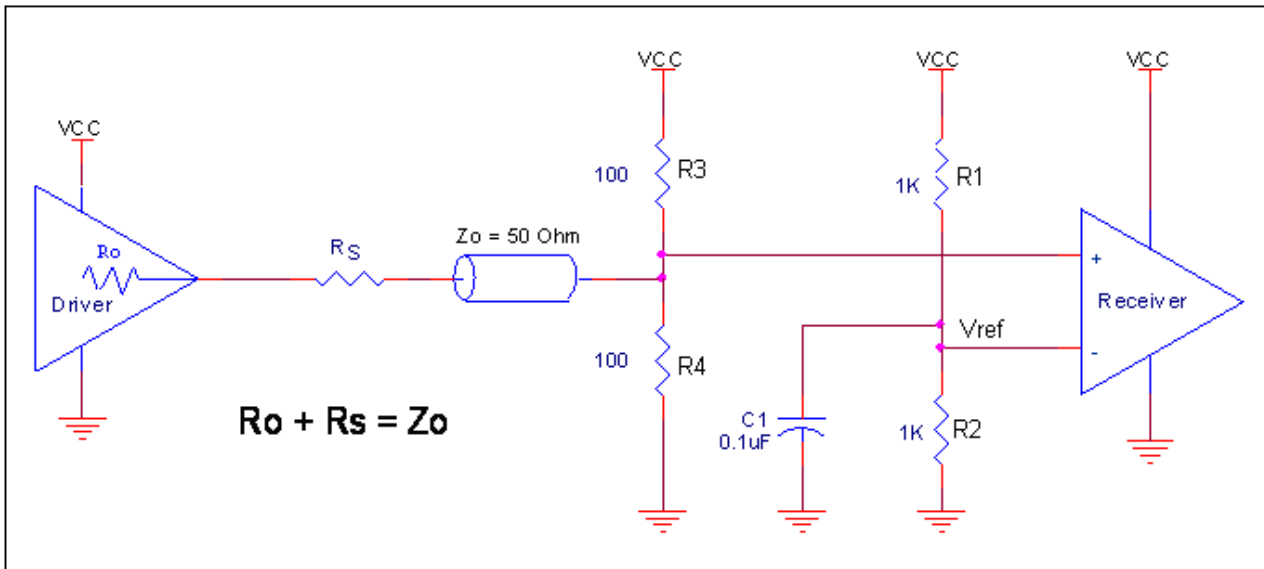
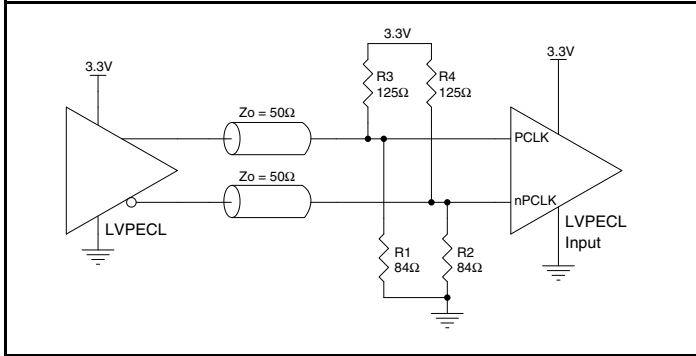


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

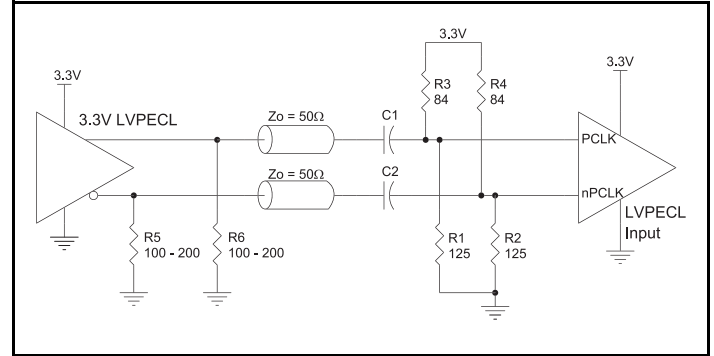
## LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, SSTL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

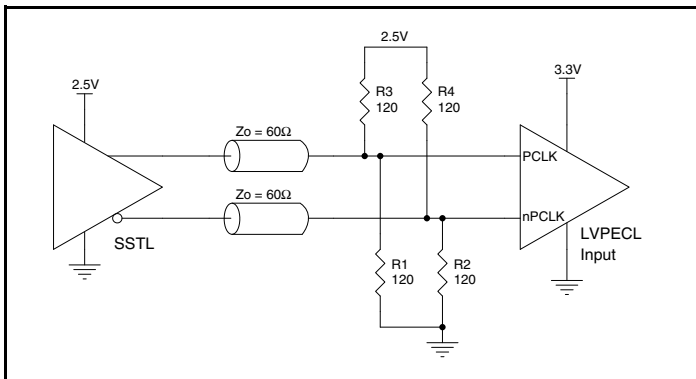
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**



**Figure 2C. PCLK/nPCLK Input Driven by an SSTL Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

#### LVCNOS\_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCNOS\_CLK input to ground.

#### LVCNOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCNOS Outputs

All unused LVCNOS output can be left floating. There should be no trace attached.

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS83940DI-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS83940DI-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDO}) = 3.465V * (26mA + 28mA) = \mathbf{187.11mW}$

### Dynamic Power Dissipation at 175MHz

$$\text{Power (175MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 * \text{number of outputs} = 9pF * 175MHz * (3.465V)^2 * 18 = \mathbf{340.4mW}$$

### Total Power Dissipation

- Total Power**  
 = Power (core)<sub>MAX</sub> + Power (175MHz)  
 = 187.15mW + 340.4mW  
 = **527.5mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 53.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.528\text{W} * 53.5^\circ\text{C/W} = 113.2^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 32 Lead LQFP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	53.5°C/W	48.0°C/W	44.0°C/W

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	53.5°C/W	48.0°C/W	44.0°C/W

## Transistor Count

The transistor count for 83940I-01 is: 819

# Package Outline and Package Dimensions

## Package Outline - Y Suffix for 32 Lead LQFP

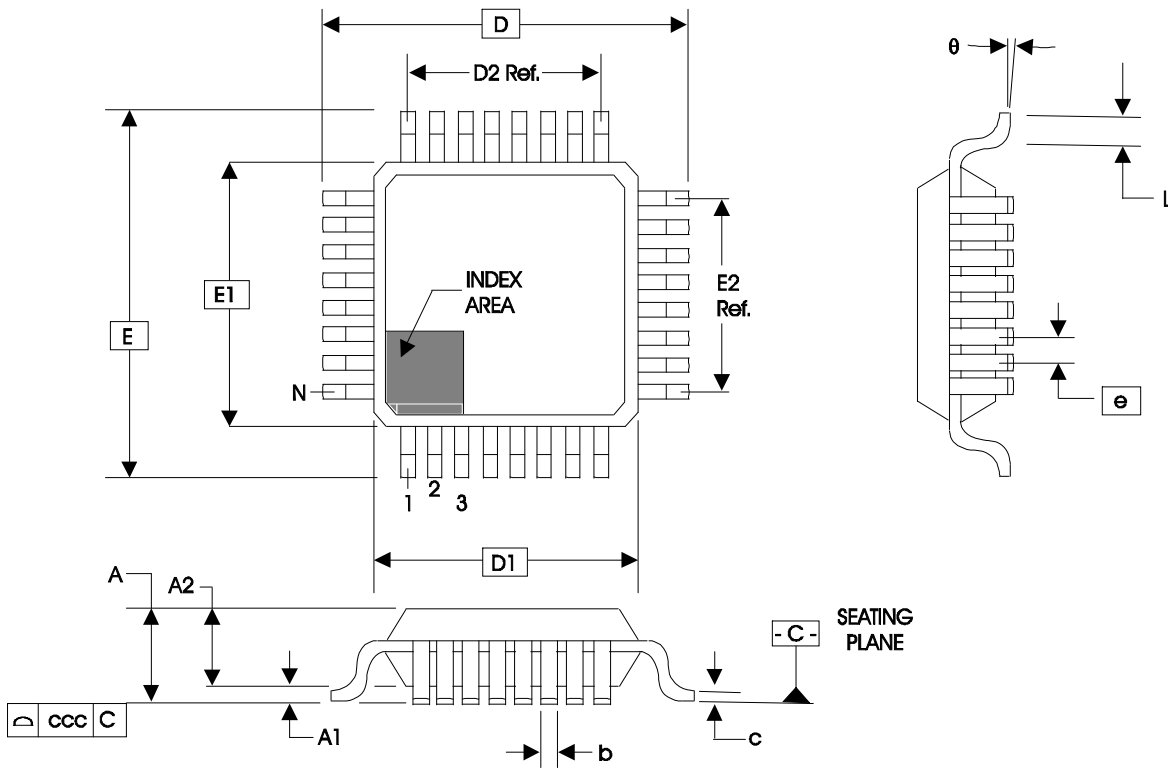


Table 8. Package Dimensions for 32 Lead LQFP

JEDEC Variation: ABC - HD			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.60 Ref.		
e	0.80 Basic		
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026



## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83940DYI-01LF	ICS83940DI01L	"Lead-Free" 32 Lead LQFP	Tray	-40°C to 85°C
83940DYI-01LFT	ICS83940DI01L	"Lead-Free" 32 Lead LQFP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	17	Ordering Information - removed leaded devices. Updated data sheet format.	3/27/15



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