HIP2105, HIP2106A

Low Voltage Driver for Synchronous Rectification

FN8999
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The HIP2105 and HIP2106A are high frequency MOSFET drivers optimized to drive two N-channel power MOSFETs in a synchronous buck converter topology. The HIP2105 has HI/LI inputs and the HIP2106A has a single PWM input. Both these drivers, combined with Renesas multi-phase buck PWM controllers, form a complete single-stage core-voltage regulator solution with high-efficiency performance at high switching frequency for advanced microprocessors.

The HIP2105 and HIP2106A are biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3nF load with less than 15ns rise/fall time. Bootstrapping of the upper gate driver is implemented using an internal low forward voltage drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-channel MOSFETs. Adaptive shoot-through protection on the HIP2106A is integrated to prevent both MOSFETs from conducting simultaneously.

The HIP2105 and HIP2106A feature a 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The HIP2106A also features an input that recognizes a high-impedance state, working together with Renesas multi-phase 3.3V or 5V PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the Schottky diode that may be used in a power system to protect the load from negative output voltage damage.

Features

- Adaptive shoot-through protection (HIP2106A only)
- HI and LI inputs (HIP2105 only)
- 0.4Ω ON-resistance and 4A sink current capability
- Low tri-state hold-off time (20ns) (HIP2106A only)
- Supports 3.3V and 5V HI/LI or PWM input
- Power-On Reset (POR)
- Dual Flat No-Lead (DFN) package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads - product outline
  - Near chip-scale package footprint; improves PCB efficiency and thinner in profile

Applications

- Wireless chargers
- High frequency low profile high efficiency DC/DC converters
- High current low voltage DC/DC converters
- E-cigarette

Related Literature

For a full list of related documents, visit our website

- HIP2105 and HIP2106A product pages

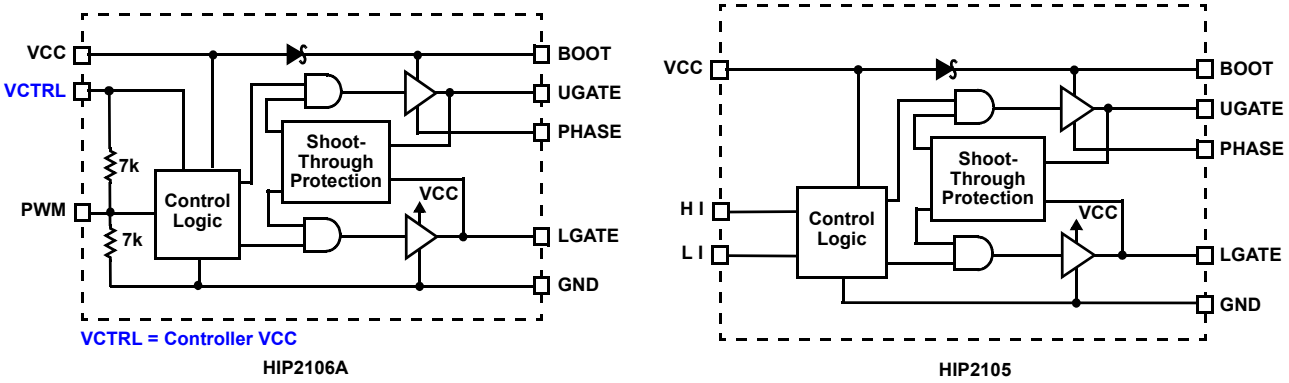


Figure 1. Block Diagrams

Contents

1. Overview

1.1 Typical Applications

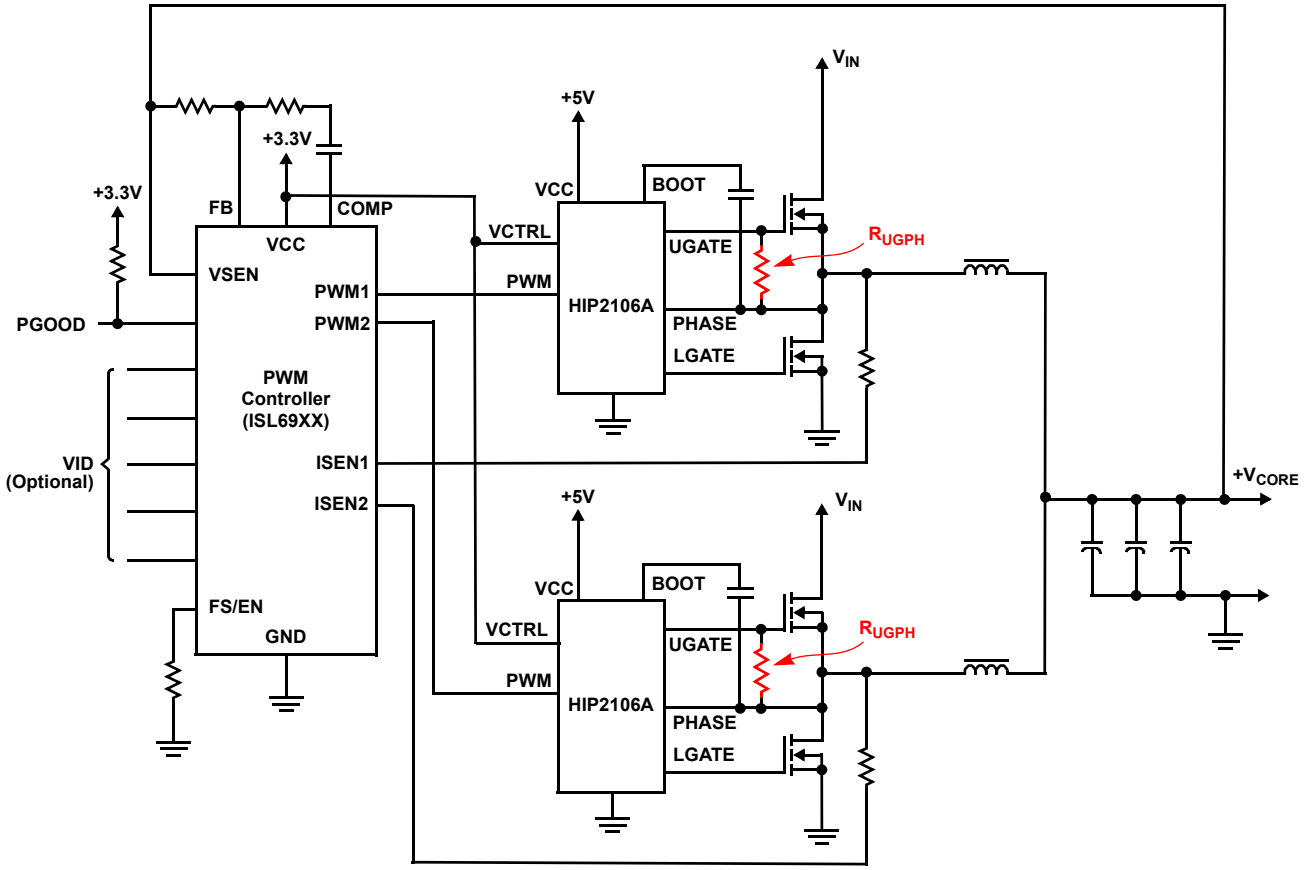


Figure 2. Multi-Phase Converter Using HIP2106A Gate Drivers

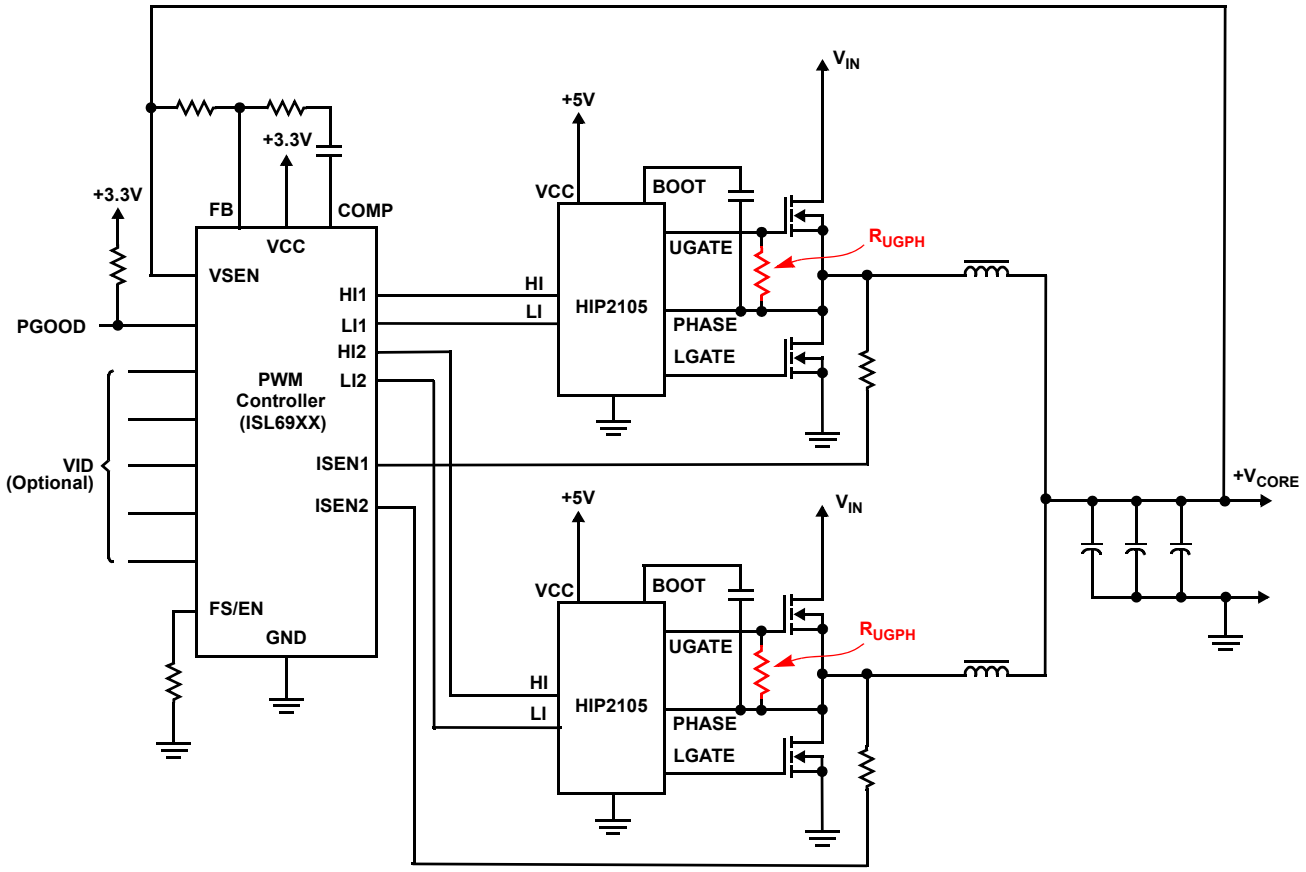


Figure 3. Multi-Phase Converter Using HIP2105 Gate Drivers

1.2 Ordering Information

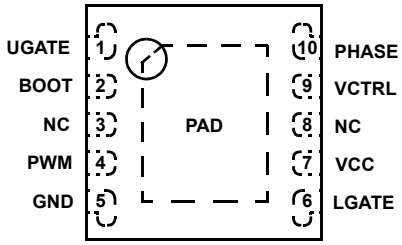
Part Number (Notes 2, 3)	Part Marking	Temperature Range (°C)	Tape and Reel (Units) (Note 1)	Package	Pkg. Dwg. #
HIP2106AIRZ	06IZ	-40 to +85	-	10 Ld 3x3 DFN	L10.3x3C
HIP2106AIRZ-T	06IZ	-40 to +85	6k	10 Ld 3x3 DFN	L10.3x3C
HIP2105FRZ	05FZ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3C
HIP2105FRZ-T	05FZ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3C
HIP2105-6MBEVAL1Z	HIP2105/6A Mother Board				
HIP2105DBEVAL1Z	HIP2105 Daughter Board				
HIP2106ADBEVAL1Z	HIP2106A Daughter Board				

Notes:

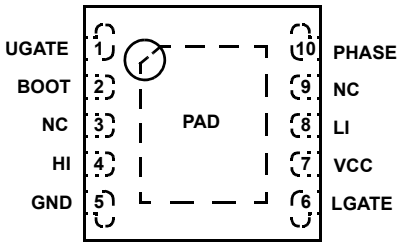
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the HIP2105 and HIP2106A product information pages. For more information about MSL, refer to TB363.

1.3 Pin Configurations

HIP2106A
10 Ld 3x3 DFN
Top View



HIP2105
10 Ld 3x3 DFN
Top View



1.4 Pin Descriptions

Pin Name	HIP2106A Pin #	HIP2105 Pin #	Description
UGATE	1	1	Upper gate drive output. Connect to the gate of the high-side N-channel power MOSFET. A gate resistor is never recommended on this pin, because it interferes with the operation shoot-through protection circuitry.Gate resistor avoidance only applies to HIP2106A. HIP2105 does not have adaptive shoot-through protection.
BOOT	2	2	Floating bootstrap supply pin for the upper gate drive. Connect a bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge used to turn on the upper MOSFET. See "Bootstrap Considerations" on page 11 for guidance in choosing the appropriate capacitor value.
NC	3, 8	3, 9	No connect.
PWM	4	-	The PWM signal (for HIP2106A) is the control input for the driver. The PWM signal can enter three distinct states during operation, see "PWM Input and Threshold Control (HIP2106A)" on page 10 for further details. Connect this pin to the PWM output of the controller.
HI	-	4	The HI signal (for the HIP2105) is the input drive for the high side gate drive output.
GND	5	5	Ground pin. All signals are referenced to this node.
LGATE	6	6	Lower gate drive output. Connect to the gate of the low-side N-channel power MOSFET. A gate resistor is never recommended on this pin, because it interferes with the operation shoot-through protection circuitry.Gate resistor avoidance only applies to HIP2106A. HIP2105 does not have adaptive shoot-through protection.
VCC	7	7	Connect this pin to a +5V bias supply. Locally bypass with a high quality ceramic capacitor to ground.
LI	-	8	This pin is the input drive for the low-side gate output.
VCTRL	9	-	This VCTRL pin (for HIP2106A) sets the PWM logic threshold. Connect this pin to 3.3V source for 3.3V PWM input or pull it to 5V source for 5V PWM input.
PHASE	10	10	Connect this pin to the source of the upper MOSFET. This pin provides the return path for the upper gate driver current.
Thermal Pad	Pad	Pad	The metal pad underneath the center of the IC is a thermal substrate. The PCB "thermal land" design for this exposed die pad should include vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the DFN to achieve its full thermal potential. This pad should be either grounded or floating, and it should not be connected to other nodes. Refer to TB389 for design guidelines.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage (V_{CC}, VCTRL)	-0.3	7	V
Input Voltage (V_{EN}, V_{PWM}, V_{HI}, V_{LI})	-0.3	V_{CC} + 0.3	V
BOOT Voltage ($V_{BOOT-GND}$)	-0.3	25 (DC) or 36 (<200ns)	V
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$)	-0.3	7 (DC)	V
	-0.3	9 (<10ns)	V
PHASE Voltage	GND - 0.3	25 (DC)	V
	GND - 8 (<20ns Pulse Width, 10µJ)	30 (<100ns)	V
UGATE Voltage	V_{PHASE} - 0.3 (DC)	V_{BOOT}	V
	V_{PHASE} - 5 (<20ns Pulse Width, 10µJ)	V_{BOOT}	V
LGATE Voltage	GND - 0.3 (DC)	V_{CC} + 0.3	V
	GND - 2.5 (<20ns Pulse Width, 5µJ)	V_{CC} + 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	2		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 4, 5)	48	7

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range (HIP2106A)	-40	+85	°C
Ambient Temperature Range (HIP2105)	-40	+125	°C
Maximum Operating Junction Temperature		+125	°C
Supply Voltage, V_{CC}	4.5	5.5	V

2.4 Electrical Specifications

Recommended operating conditions, V_{CC} = 5V ±10%, unless otherwise specified, **Boldface limits apply across the operating temperature range -40°C to +85°C for HIP2106A and -40°C to +125°C for HIP2105.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
V_{CC} Supply Current						
Bias Supply Current - HIP2106A	I_{VCC}	PWM pin floating, V_{VCC} = 5V	-	190	-	µA
Bias Supply Current - HIP2105	I_{VCC}	HI/LI pin floating, V_{VCC} = 5V	-	80	-	µA
POR Rising			-	3.4	**4.2**	V
POR Falling			**2.2**	3.1	-	V
Hysteresis			-	300	-	mV
VCTRL Input (HIP2106A only)						
Rising Threshold			-	2.75	**2.90**	V
Falling Threshold			**2.4**	2.65	-	V
PWM Input (HIP2106A only)						
Sinking Impedance	R_{PWM_SNK}		-	3.5	-	kΩ
Source Impedance	R_{PWM_SRC}		-	3.5	-	kΩ
Tri-State Lower Threshold		V_{VCTRL} = 3.3V (-110mV hysteresis)	-	1.1	-	V
		V_{VCTRL} = 5V (-250mV hysteresis)	-	1.5	-	V
Tri-State Upper Threshold		V_{VCTRL} = 3.3V (+110mV hysteresis)	-	1.9	-	V
		V_{VCTRL} = 5V (+250mV hysteresis)	-	3.25	-	V
Tri-State Shutdown Hold-Off Time	t_{TSSHD}	t_{PDLU} or t_{PDLL} + gate falling time	-	20	-	ns
HI/LI Input (HIP2105 only)						
V_{IH} and V_{IL} Rising	V_{IH}	V_{DD} = 4.5V	**1.3**	1.65	**2**	V
		V_{DD} = 5.0V	**1.4**	1.75	**2.1**	
		V_{DD} = 5.5V	**1.5**	1.9	**2.2**	V
V_{IH} and V_{IL} Falling	V_{IL}	V_{DD} = 4.5V	**0.9**	1.1	**1.45**	V
		V_{DD} = 5.0V	**0.95**	1.2	**1.55**	
		V_{DD} = 5.5V	**1.05**	1.3	**1.65**	V
Switching Time (HIP2106A, See Figure 6 on page 9)						
UGATE Rise Time (Note 6)	t_{RU}	V_{VCC} = 5V, 3nF load	-	8	-	ns
LGATE Rise Time (Note 6)	t_{RL}	V_{VCC} = 5V, 3nF load	-	8	-	ns
UGATE Fall Time (Note 6)	t_{FU}	V_{VCC} = 5V, 3nF load	-	8	-	ns
LGATE Fall Time (Note 6)	t_{FL}	V_{VCC} = 5V, 3nF load	-	4	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 5V, outputs unloaded	-	20	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 5V, outputs unloaded	-	15	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, outputs unloaded	-	19	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, outputs unloaded	-	18	-	ns
Tri-State to UG/LG Rising Propagation Delay	t_{PTS}	V_{VCC} = 5V, outputs unloaded	-	30	-	ns
Switching Time (HIP2105, See Figure 7 on page 9)						
UGATE Rise Time (Note 6)	t_{RU}	V_{VCC} = 5V, 3nF load	-	15	-	ns
LGATE Rise Time (Note 6)	t_{RL}	V_{VCC} = 5V, 3nF load	-	10	-	ns
UGATE Fall Time (Note 6)	t_{FU}	V_{VCC} = 5V, 3nF load	-	15	-	ns

Recommended operating conditions, V_{CC} = 5V ±10%, unless otherwise specified, **Boldface limits apply across the operating temperature range -40°C to +85°C for HIP2106A and -40°C to +125°C for HIP2105.**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
LGATE Fall Time (Note 6)	t_{FL}	V_{VCC} = 5V, 3nF load	-	6	-	ns
HI to UGATE Falling Propagation Delay	t_{PDFU}	V_{VCC} = 5V, outputs unloaded	-	35	-	ns
LI to LGATE Falling Propagation Delay	t_{PDFL}	V_{VCC} = 5V, outputs unloaded	-	20	-	ns
HI to UGATE Rising Propagation Delay	t_{PDRU}	V_{VCC} = 5V, outputs unloaded	-	29	-	ns
LI to LGATE Rising Propagation Delay	t_{PDRL}	V_{VCC} = 5V, outputs unloaded	-	15	-	ns
Turn-On/Off Propagation Mismatch (HO rising to LO falling)	t_{MHRLF}	V_{VCC} = 5V, outputs unloaded	-	9	-	ns
Turn-On/Off Propagation Mismatch (LO rising to HO falling)	t_{MLRHF}	V_{VCC} = 5V, outputs unloaded	-	20	-	ns
Output (Note 6)						
Upper Drive Source Resistance	r_{UG_SRC}	250mA source current	-	1.0	**2.5**	Ω
Upper Drive Sink Resistance	r_{UG_SNK}	250mA sink current	-	1.0	**2.5**	Ω
Lower Drive Source Resistance	r_{LG_SRC}	250mA source current	-	1.0	**2.5**	Ω
Lower Drive Sink Resistance	r_{LG_SNK}	250mA sink current	-	0.4	**1.0**	Ω

Notes:
6. Limits established by characterization and are not production tested.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 Timing Test Setups

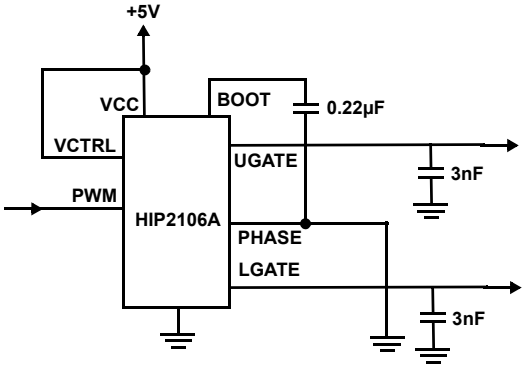


Figure 4. HIP2106A Rise/Fall Timing Test Setup

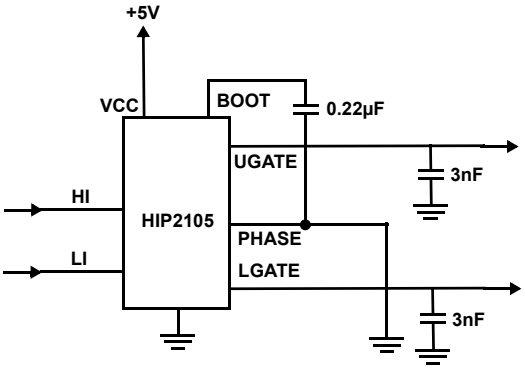


Figure 5. HIP2105 Rise/Fall Timing Test Setup

2.6 Timing Diagrams

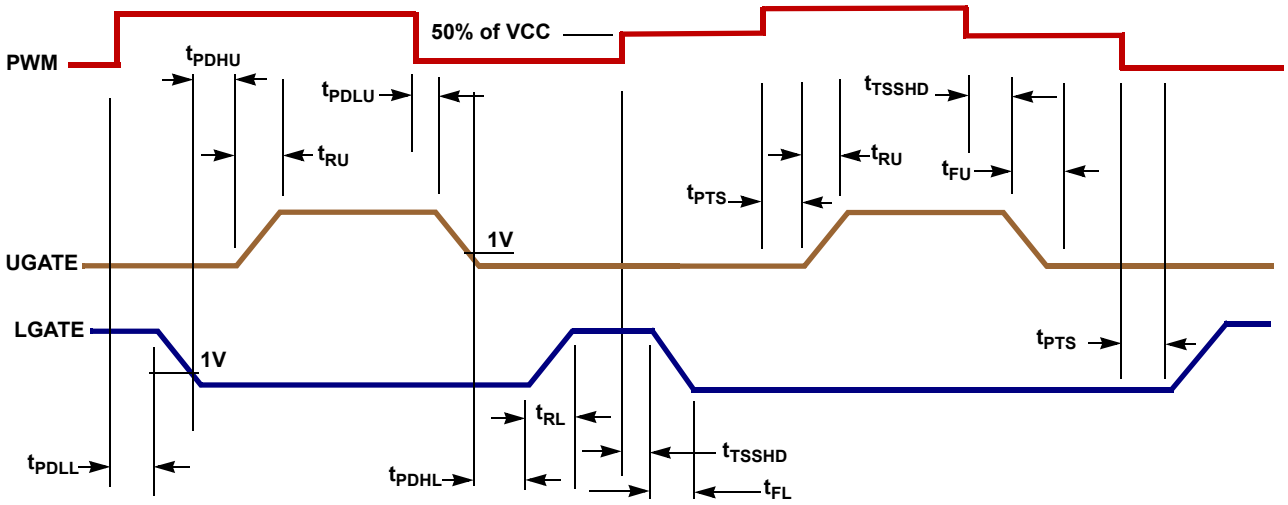


Figure 6. HIP2106A Timing Diagram

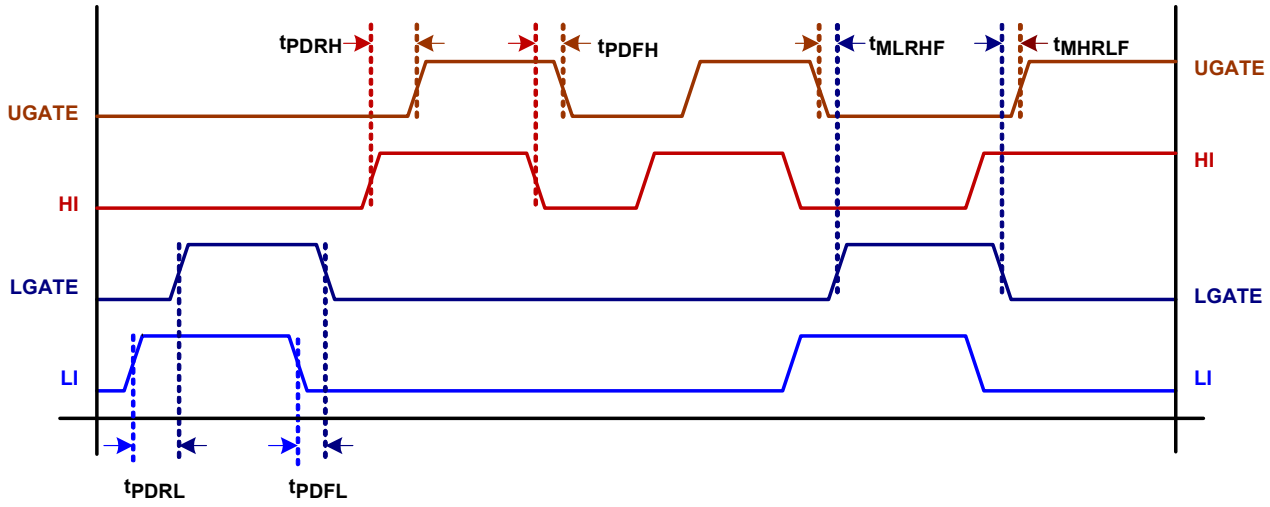


Figure 7. HIP2105 Timing Diagram

3. Device Information

3.1 Operation and Adaptive Shoot-Through Protection (HIP2106A)

Designed for high speed switching, the HIP2106A MOSFET driver controls both high-side and low-side N-channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Figure 4 on page 8). After a short propagation delay (t_{PDLL}), the lower gate begins to fall. Typical fall times (t_{FL}) are provided in the "Electrical Specifications" table on page 7. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time (t_{PDHU}) after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise (t_{RU}) and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay (t_{PDLU}) is encountered before the upper gate begins to fall (t_{FU}). The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET after a short delay time, t_{PDHL}, after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises (t_{RL}), turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with a large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω ON-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

3.1.1 PWM Input and Threshold Control (HIP2106A)

A unique feature of the HIP2106A is the programmable PWM logic threshold set by the control pin (VCTRL) voltage. The VCTRL pin should connect to the VCC of the controller, thus the PWM logic threshold follows the voltage level of the controller. For 5V applications, this pin can tie to the driver VCC and simplify the routing.

The HIP2106A also features adaptable tri-state PWM input. When the PWM signal enters the shutdown window, either MOSFET previously conducting is turned off. If the PWM signal remains within the shutdown window for longer than the gate turn-off propagation delay of the previously conducting MOSFET, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. The PWM rising and falling thresholds outlined in the "Electrical Specifications" on page 7 determine when the lower and upper gates are enabled. During normal operation in a typical application, the PWM rise and fall times through the shutdown window should not exceed either output's turn-off propagation delay plus the MOSFET gate discharge time to ~1V. Abnormally long PWM signal transition times through the shutdown window will simply introduce additional dead time between turn off and turn on of the synchronous bridge's MOSFETs. For optimal performance, no more than 50pF parasitic capacitive load should be present on the PWM line of the HIP2106A (assuming a Renesas PWM controller is used).

3.2 HI/LI Inputs (HIP2105)

Designed for high speed switching, the HIP2105 MOSFET driver controls both high-side and low-side N-channel FETs from two externally provided HI and LI signals. The external signal source in this case will provide the required dead time control

A falling transition on LI initiates the turn-off of the lower MOSFET (see Figure 5 on page 8). After a short propagation delay (t_{PDFL}), the lower gate begins to fall. Typical fall times (t_{FL}) are provided in the "Electrical Specifications" table on page 7. After an externally set dead time the HI will initiate the turn on of the upper MOSFET, after a short propagation delay (t_{PDRH}) the UGATE begins to rise with rise time given by (t_{RH}). At the end

of the high-side on-time the HI will initiate a fall, after a propagation delay of (t_{PDFH}) the UGATE will turn off with a fall time (t_{FH}). Once the UGATE is off and the dead time has elapsed, the LGATE turn on is initiated by the LI input with a propagation delay of (t_{PDRL}) and the cycle repeats. However, by internal hardwired logic if both HI and LI are high or low the UGATE and LGATE outputs remain in the low state to prevent a shoot-through condition. Additionally, if one of the inputs is high and the other input goes high, any output that is high transitions low to prevent a shoot-through condition.

3.3 Bootstrap Considerations

This driver features an internal bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

Equation 1 helps select a proper bootstrap capacitor size:

(EQ. 1)
$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet VCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, Q_G, from the datasheet is 10nC at 4.5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 22nC at V_{CC} levels. assuming a 200mV droop in drive voltage over the PWM cycle. A bootstrap capacitance of at least 0.110µF is required. The next larger standard value capacitance is 0.22µF. A good quality ceramic capacitor is recommended.

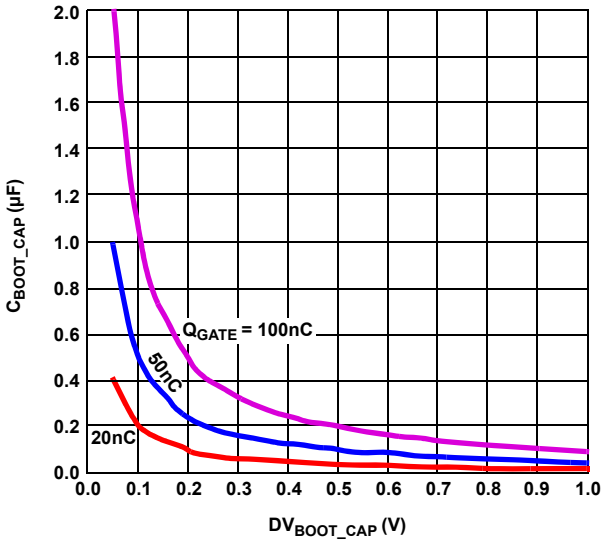


Figure 8. Bootstrap Capacitance vs Boot Ripple Voltage

3.4 Power Dissipation

Package power dissipation is mainly a function of the switching frequency (f_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. See "Layout Considerations" on page 13 for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses

due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively:

(EQ. 2)
$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC$$
$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet VCC^2}{V_{GS1}} \bullet f_{SW} \bullet N_{Q1}$$
$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet VCC^2}{V_{GS2}} \bullet f_{SW} \bullet N_{Q2}$$

(EQ. 3)
$$I_{VCC} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}}\right) \bullet VCC \bullet f_{SW} + I_Q$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate-to-source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs, respectively. The I_Q V_{CC} product is the quiescent power of the driver without capacitive load and is typically negligible.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}, should be a short to avoid interfering with the operation shoot-through protection circuitry) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 9 and 10 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

(EQ. 4)
$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC$$
$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$
$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$
$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

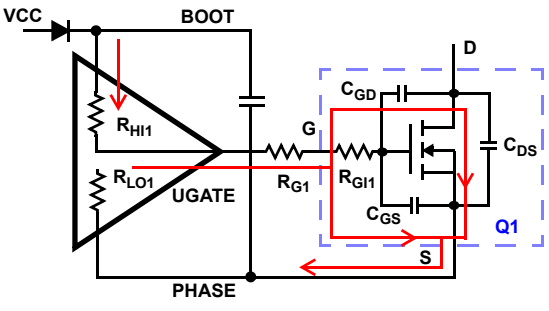


Figure 9. Typical Upper-Gate Drive Turn-On Path

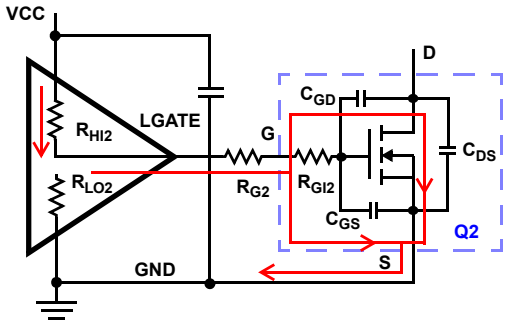


Figure 10. Typical Lower-Gate Drive Turn-On Path

4. Application Information

4.1 MOSFET Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs, and packaging can go a long way toward minimizing such unwanted stress.

The D^2-PAK, or D-PAK packaged MOSFETs, have large parasitic lead inductances and are not recommended unless additional circuits are implemented to prevent the BOOT and PHASE pins from exceeding the device rating. Low-profile MOSFETs, such as direct FETs and multi-source leads devices (SO-8, LFPAK, PowerPAK), have low parasitic lead inductances and are preferred.

4.2 Layout Considerations

A good layout helps reduce the ringing on the switching node (PHASE) and significantly lowers the stress applied to the output drives. Use the following advice for an optimized layout:

- Keep decoupling loops (VCC - GND and BOOT - PHASE) as short as possible.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node. Ideally, place the source of the upper and the drain of the lower MOSFET as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Place the input capacitors (especially ceramic decoupling) as close to the drain of the upper and source of the lower MOSFETs as possible.

In addition, for heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes improve heat dissipation and allow the part to achieve its full thermal potential. Figures 11 and 12 show a layout example.

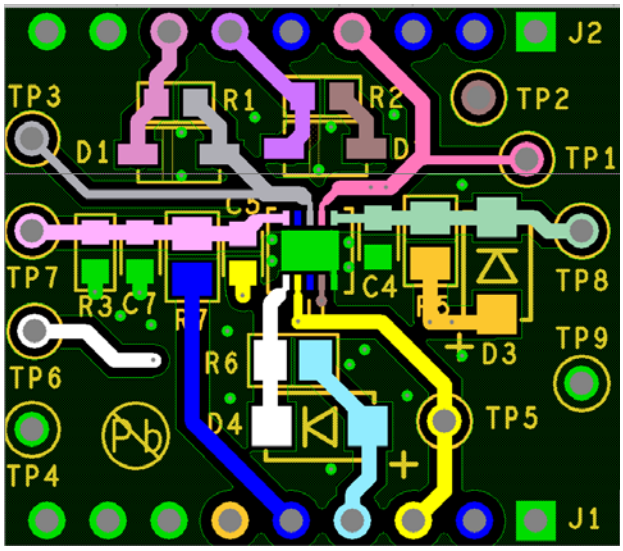


Figure 11. HIP2105DBEVAL1Z Top Layer

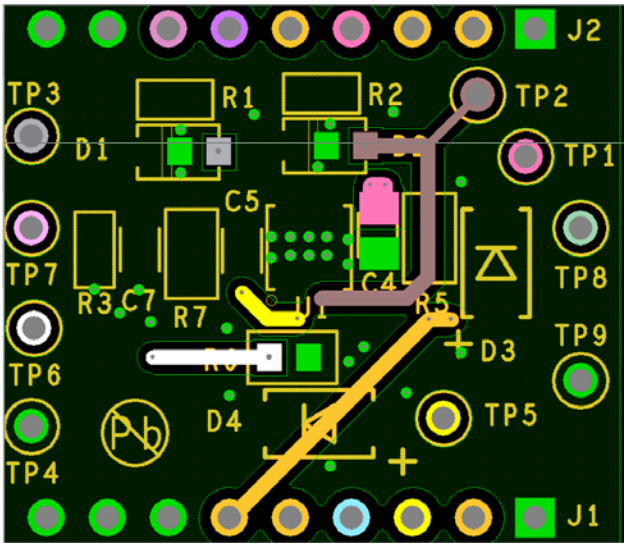


Figure 12. HIP2105DBEVAL1Z Bottom Layer

4.3 Upper MOSFET Self Turn-On Effects at Startup

If the driver has insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, because of self-coupling through the internal C_{GD} of the MOSFET, the UGATE could momentarily rise up to a level greater than the threshold voltage of the MOSFET. This could potentially turn on the upper switch and result in damaging inrush energy. Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, a 5kΩ to 10kΩ resistor is typically sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated with Equation 5, which assume a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. These equations are provided for guidance purpose only. Therefore, the actual coupling effect should be examined using a very high impedance (10MΩ or greater) probe to ensure a safe design margin.

(EQ. 5)
$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right)$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

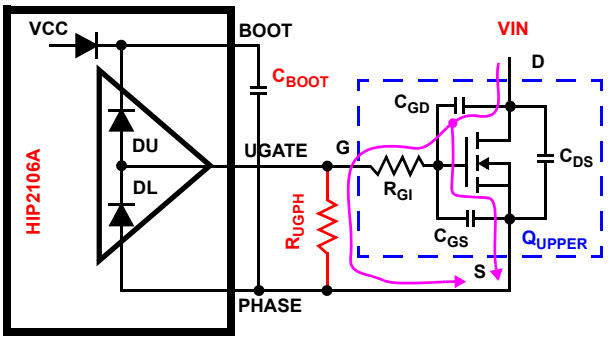


Figure 13. Gate-to-Source Resistor to Reduce Upper MOSFET Miller Coupling

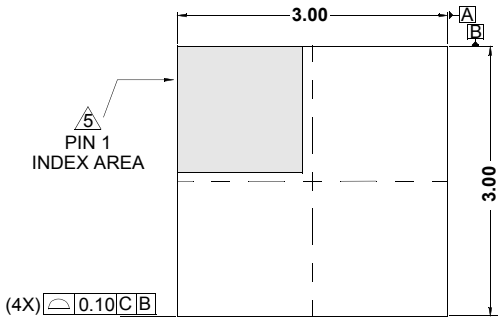
5. Revision History

Rev.	Date	Description
1.00	Jun 6, 2018	Updated the first Features bullet and added the second one. In the second paragraph on page 1 changed 10ns to 15ns. Added the HIP2105 product information throughout datasheet. Updated Ordering information by adding Tape and Reel column and updating Note 1. Updated Pin descriptions for the UGATE and LGATE pins. Added CDM ESD and Latch-up Information Updated the Supply Voltage Maximum to 5.5V and added Minimum specification of 4.5V under "Recommended Operating Conditions" on page 6. Removed minimum value for the Maximum Operating Junction Temperature. Updated POR Falling typical from 3.0 to 3.1 Updated Hysteresis typical from 400 to 300 VIH and VIL Rising VDD = 4.5V Min changed from 1.22 to 1.3, Typ changed from 1.5 to 1.65, and max changed from 1.8 to 2V. VIH and VIL Rising VDD = 5.0 added Row VIH and VIL Rising VDD = 5.5V Min changed from 2.0 to 1.5, Typ changed from 2.4 to 1.9, and max changed from 2.7 to 2.2V. VIH and VIL Falling VDD = 4.5V Min changed from 0.8 to 0.9, Typ changed from 1.0 to 1.1, and max changed from 1.2 to 1.45V. VIH and VIL Falling VDD = 5.0V added Row VIH and VIL Falling VDD = 5.5V Min changed from 1.2 to 1.05, Typ changed from 1.5 to 1.3, and max changed from 1.7 to 1.65V. Added layout files to Layout Considerations section.
0.00	Jan 18, 2018	Initial release

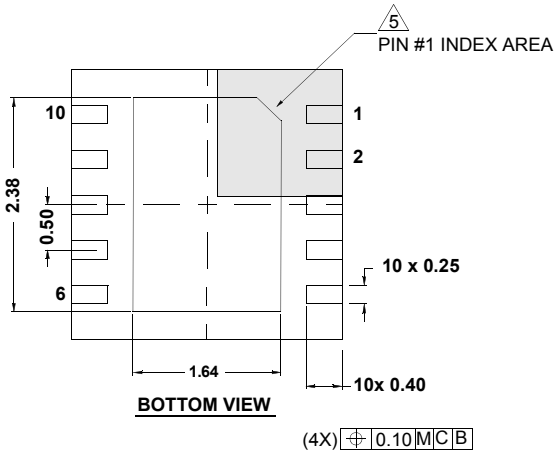
6. Package Outline Drawing

For the most recent package outline drawing, see L10.3x3C.

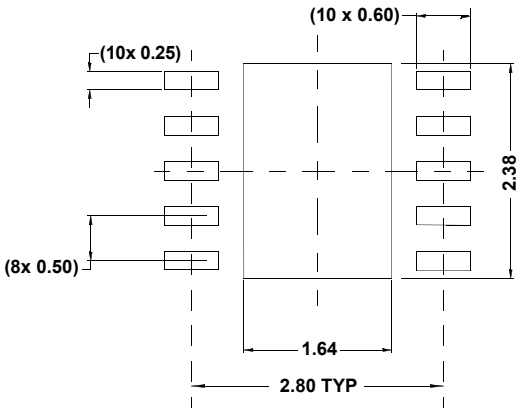
L10.3x3C
10 LEAD DUAL FLAT PACKAGE (DFN)
Rev 4, 3/15



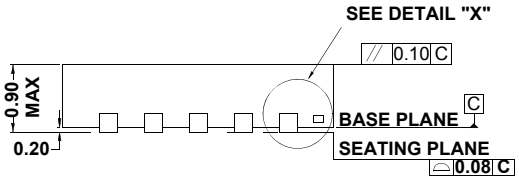
TOP VIEW



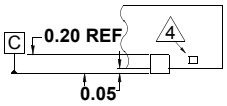
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.

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(Rev.4.0-1 November 2017)

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