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April 1st, 2010
Renesas Electronics Corporation

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HD74LS194A

4-bit Bidirectional Universal Shift Register

REJ03D0456-0300
Rev.3.00
Jul.15.2005

The bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs. Operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely;

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

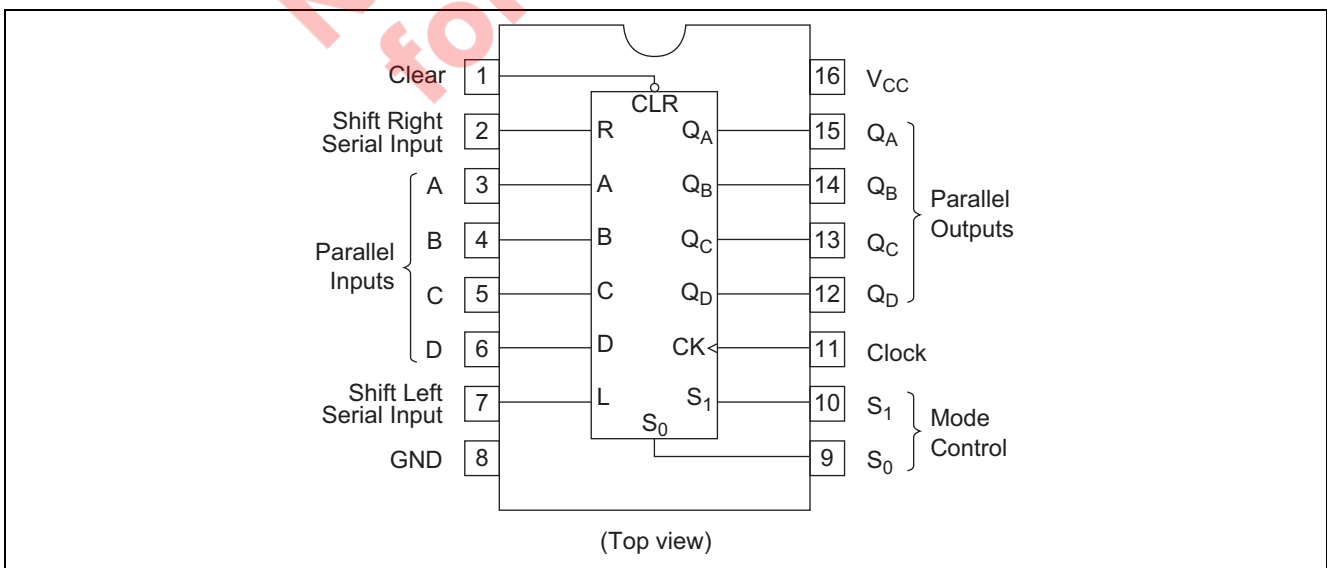
Clocking of the flip-flop is inhibited when both mode control inputs are low.

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS194AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS194AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

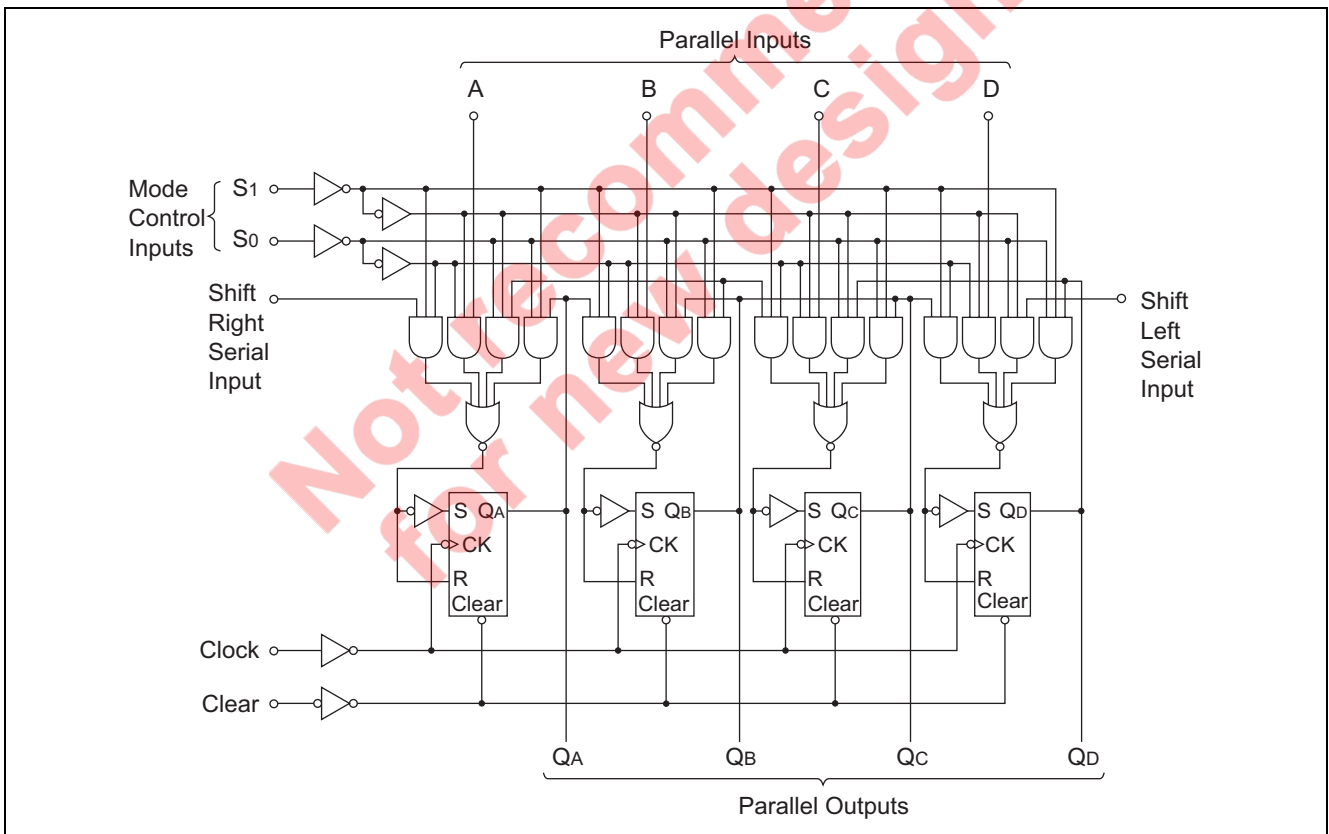


Function Table

Clear	Mode		Clock	Inputs						Outputs			
	S ₁	S ₀		Serial		Parallel				Q _A	Q _B	Q _C	Q _D
				Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

- Notes:
1. H; high level, L; low level, X; irrelevant
 2. ↑; transition from low to high level
 3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively
 4. Q_{A0} to Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady-state input conditions were established.
 5. Q_{An} to Q_{Dn}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the most-recent ↑ transition of the clock.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_w(CK)$	20	—	—	ns
Clear pulse width	$t_w(CLR)$	20	—	—	ns
Setup time	Mode Control	30	—	—	ns
	A, B, C, D, R, L	20	—	—	ns
	CLR (inactive state)	25	—	—	ns
Hold time	t_h	0	—	—	ns

Electrical Characteristics

($T_a = -20$ to $+75$ °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ μA
	V_{OL}	—	—	0.4	V	$I_{OL} = 4$ mA
		—	—	0.5	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $I_{OL} = 8$ mA, $V_{IL} = 0.8$ V
Input current	I_{IH}	—	—	20	μA	$V_{CC} = 5.25$ V, $V_I = 2.7$ V
	I_{IL}	—	—	-0.4	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V
	I_I	—	—	0.1	mA	$V_{CC} = 5.25$ V, $V_I = 7$ V
Short-circuit output current	I_{OS}	-20	—	-100	mA	$V_{CC} = 5.25$ V
Supply current**	I_{CC}	—	15	23	mA	$V_{CC} = 5.25$ V
Input clamp voltage	V_{IK}	—	—	-1.5	V	$V_{CC} = 4.75$ V, $I_{IN} = -18$ mA

Notes: * $V_{CC} = 5$ V, $T_a = 25$ °C

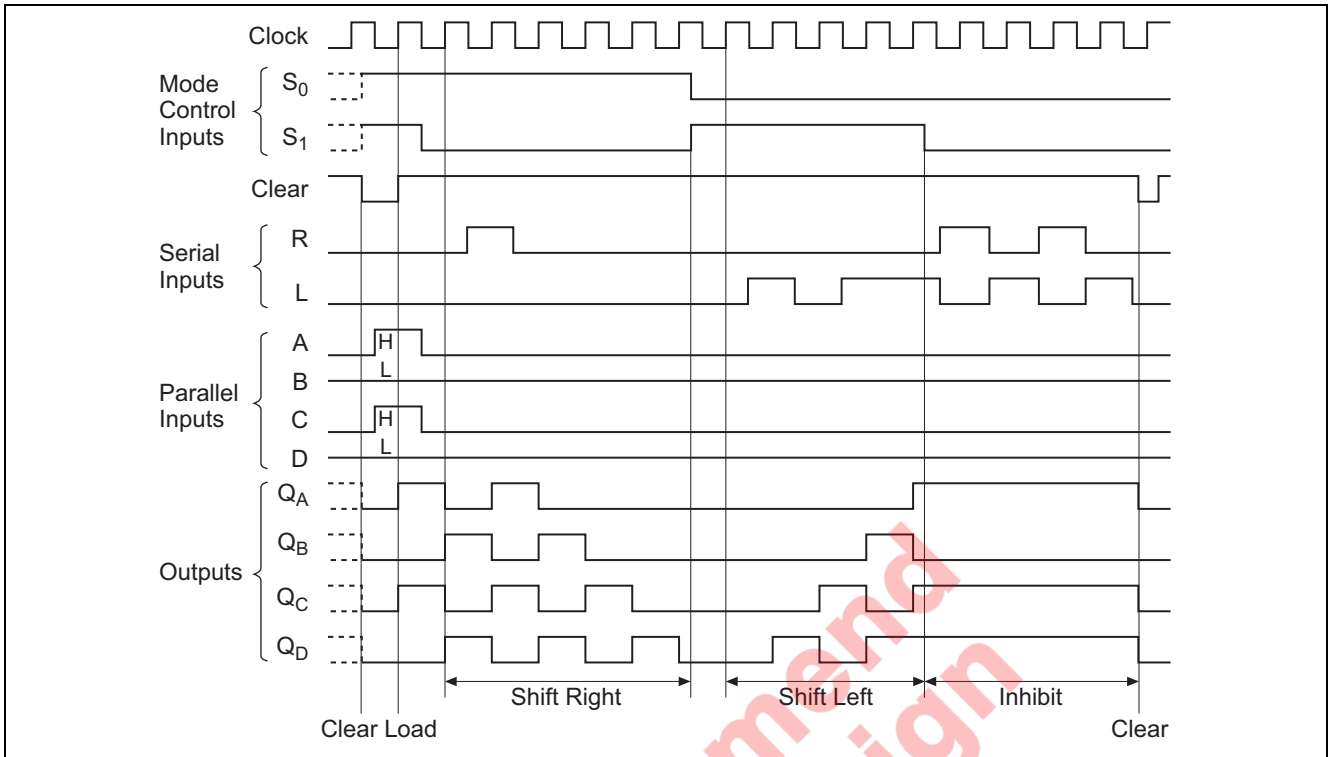
** With all outputs open, inputs A through D grounded, and 4.5 V applied to S_0 , S_1 , clear and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

Switching Characteristics

($V_{CC} = 5$ V, $T_a = 25$ °C)

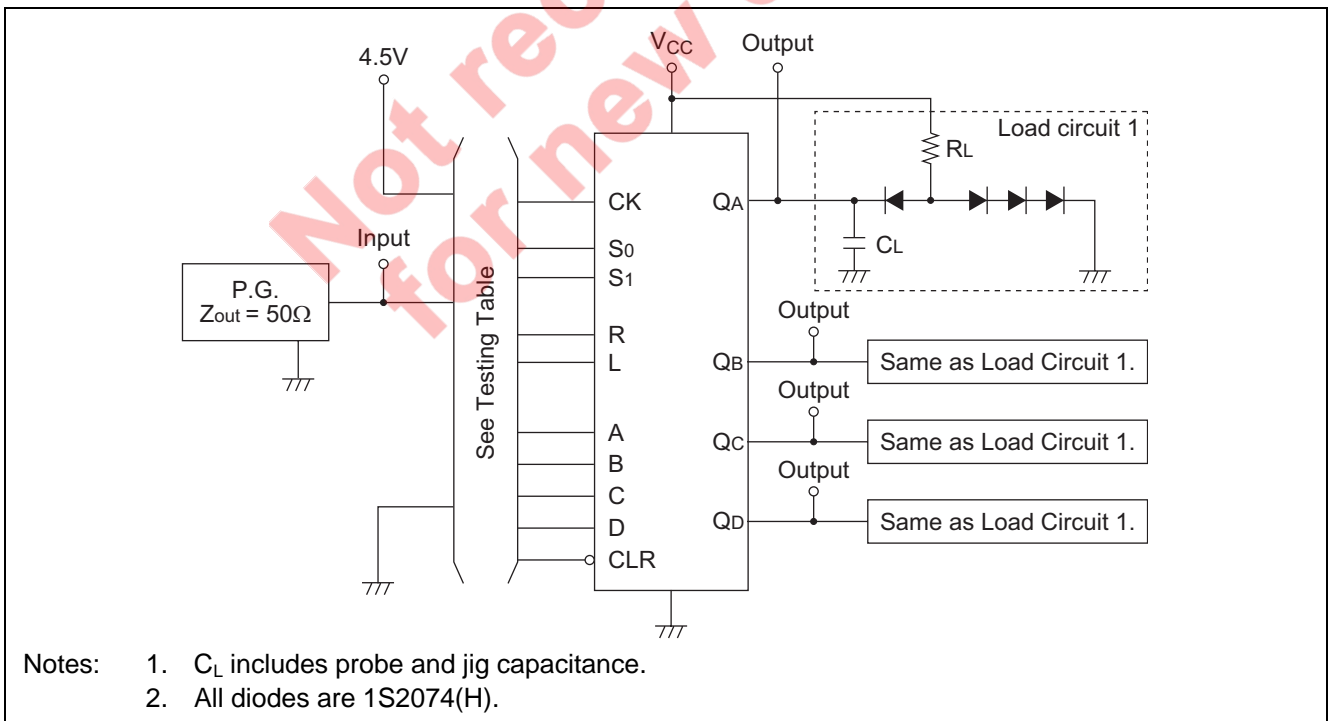
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	36	—	MHz	
Propagation delay time	t_{PHL}	Clear	Q	—	19	30	ns	$C_L = 15$ pF, $R_L = 2$ k Ω
	t_{PLH}	Clock		—	14	22	ns	
	t_{PHL}	Clock		—	17	26	ns	

Count Sequences



Testing Method

Test Circuit



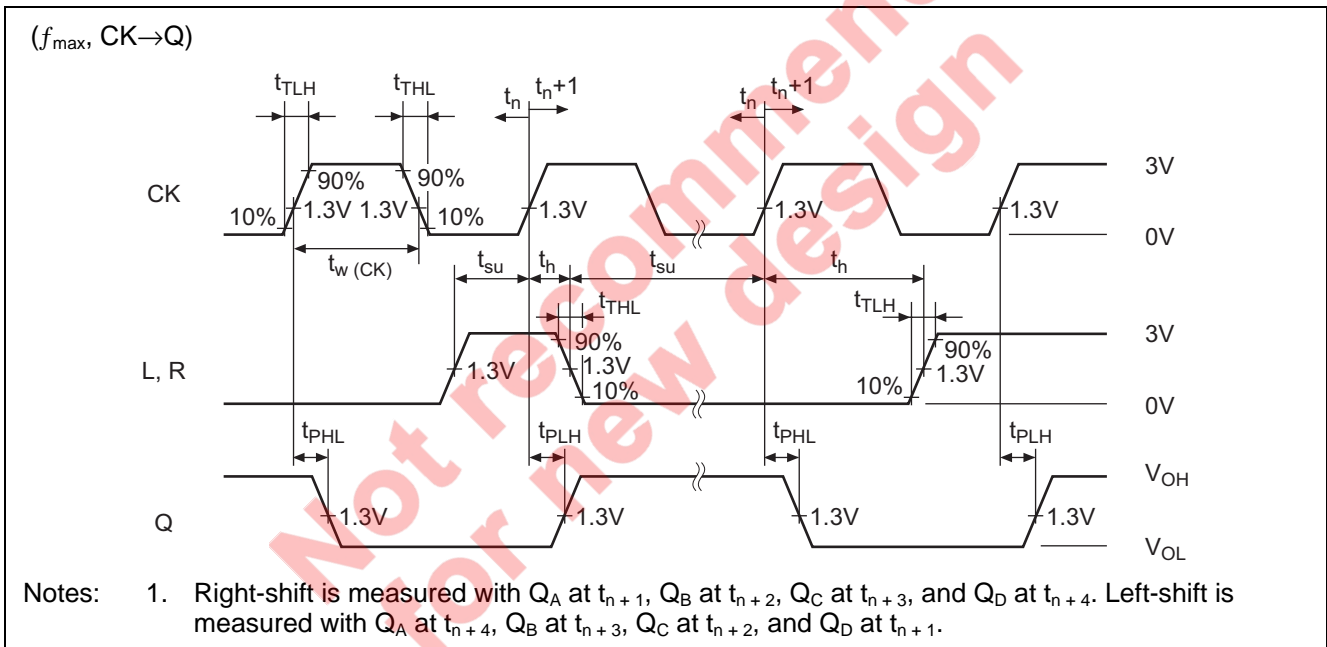
- Notes:
1. C_L includes probe and jig capacitance.
 2. All diodes are 1S2074(H).

Testing Table

Item	From input to output	Inputs									
		CLR	S ₁	S ₀	CK	L	R	A	B	C	D
f _{max}	right-shift	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
	left-shift	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	GND	GND
t _{PLH}	Clear→Q	IN	4.5V	4.5V	IN	GND	GND	4.5V	4.5V	4.5V	4.5V
t _{PHL}	Clock→Q	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
		4.5V	4.5V	GND	IN	IN	4.5V	GND	GND	GND	GND

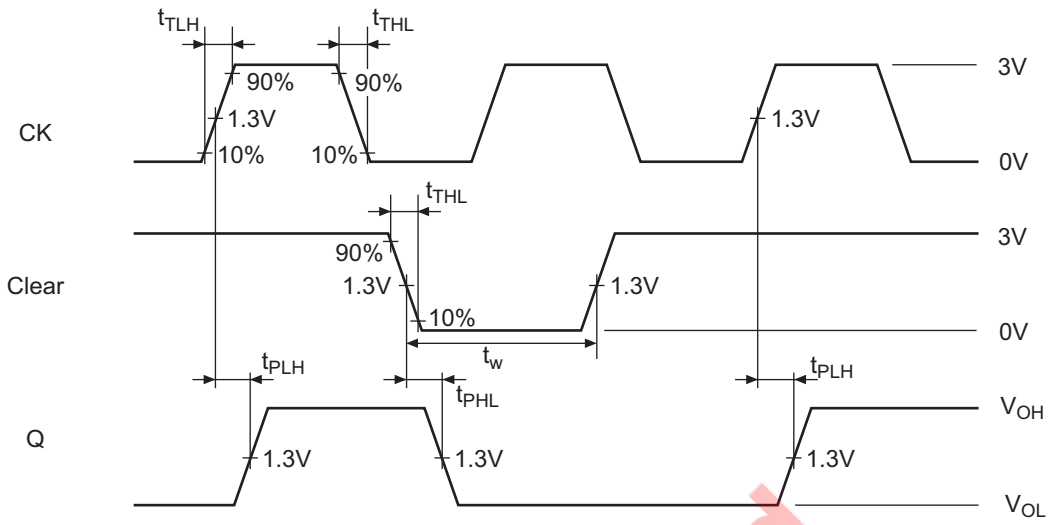
Item	From input to output	Outputs			
		Q _A	Q _B	Q _C	Q _D
f _{max}	right-shift	OUT	OUT	OUT	OUT
	left-shift	OUT	OUT	OUT	OUT
t _{PLH}	Clear→Q	OUT	OUT	OUT	OUT
t _{PHL}	Clock→Q	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT

Waveforms 1



Waveforms 2

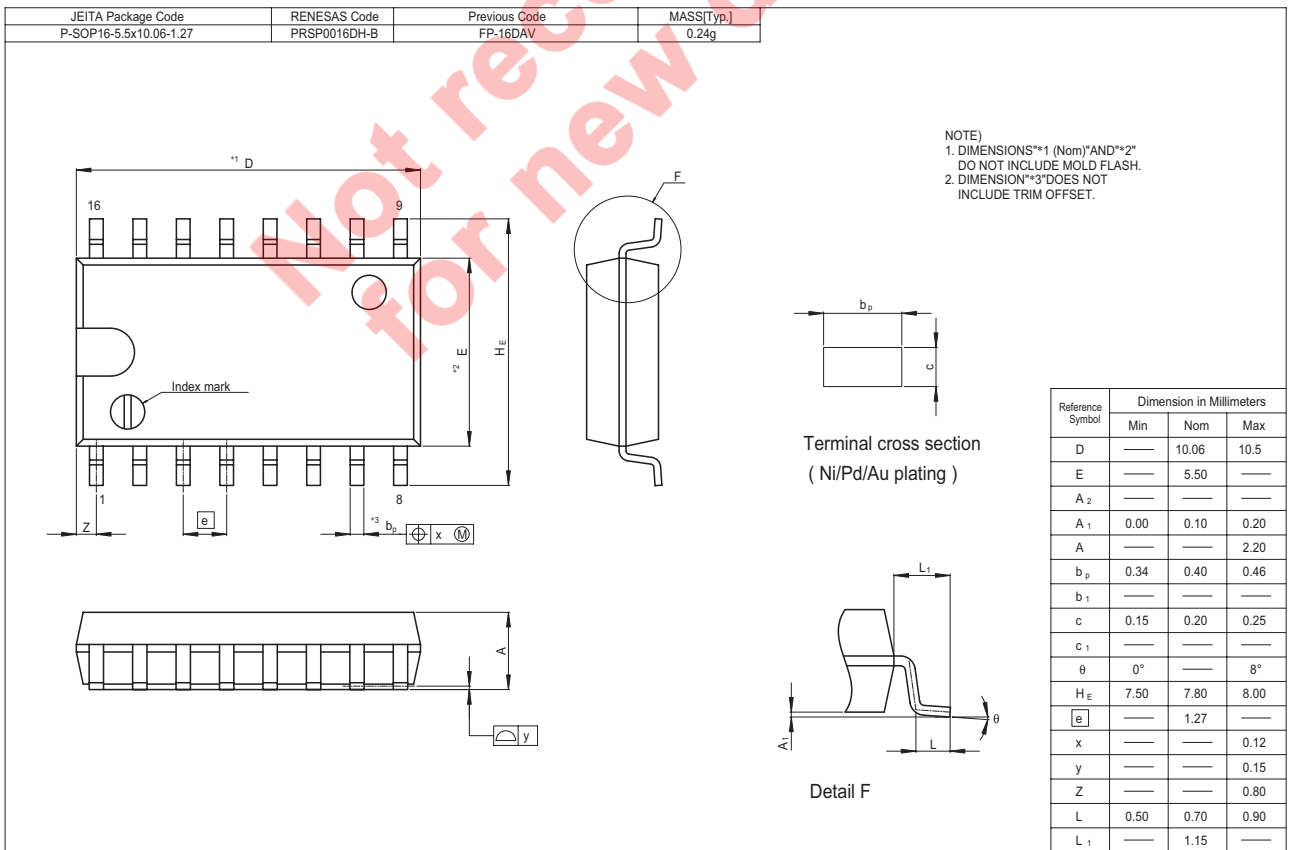
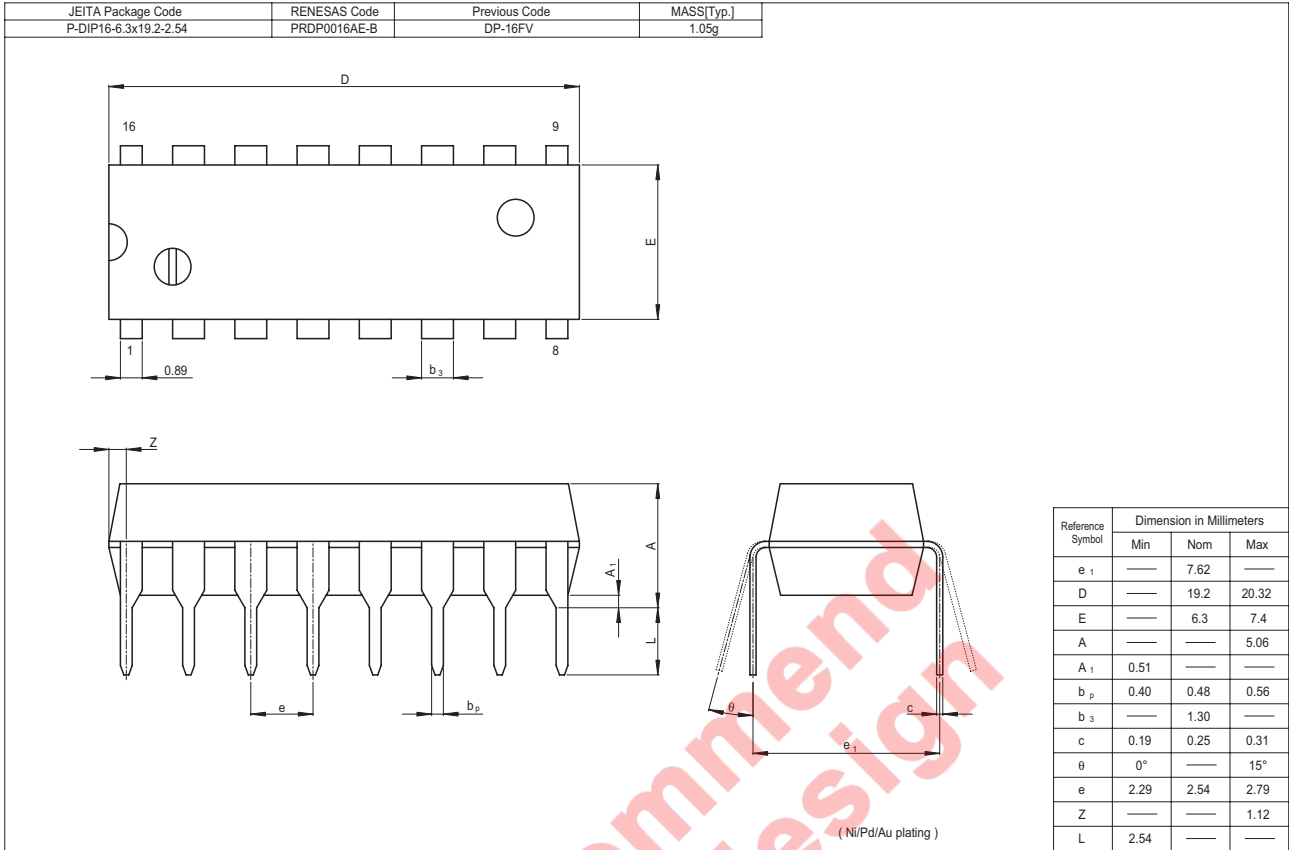
(Clear→Q)



Notes: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns

Not recommended for new design

Package Dimensions



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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510