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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74HC108

## Dual J-K Flip-Flops

(with Preset, Common Clear and Common Clock)

REJ03D0560-0200  
(Previous ADE-205-433)  
Rev.2.00  
Oct 11, 2005

### Description

This flip-flop is edge sensitive to the clock input and change state on the negative transition of the clock pulse. Each flip-flop has independent J, K, and preset inputs and Q and  $\bar{Q}$  outputs. Two flip-flops are controlled by a common clear and a common clock. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

### Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 20 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 2  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC108RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

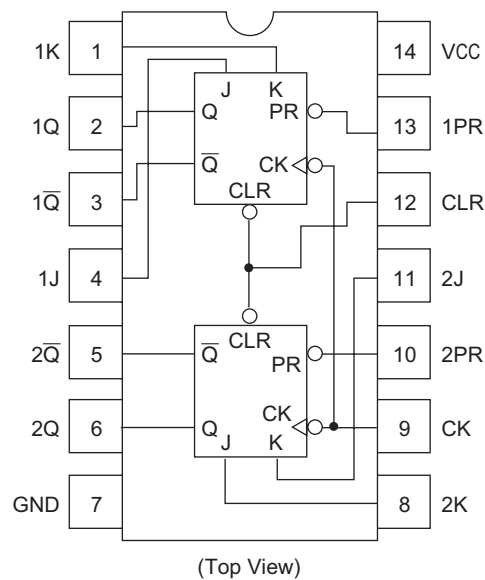
### Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$H^{*1}$	$H^{*1}$
H	H	$\downarrow$	L	L	No change	
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	H	H	Toggle	
H	H	L	X	X	No change	
H	H	H	X	X	No change	
H	H	$\uparrow$	X	X	No change	

Note: 1. Q and  $\bar{Q}$  will remain High as long as preset and Clear are Low, but Q and  $\bar{Q}$  are unpredictable, if Preset and Clear go High simultaneously.

H : High level  
L : Low level  
X : Irrelevant

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{in}, V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_O$	$\pm 25$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0 \text{ V}$
		0 to 500		$V_{CC} = 4.5 \text{ V}$
		0 to 400		$V_{CC} = 6.0 \text{ V}$

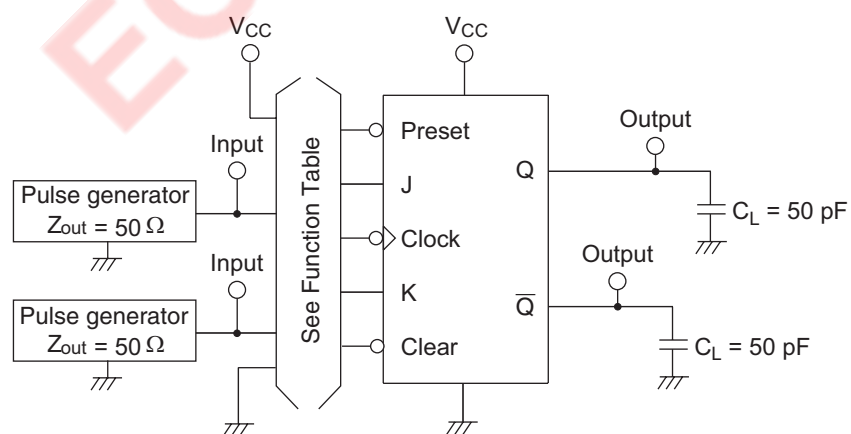
Note: 1. This item guarantees maximum limit when one input switches.  
Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33			I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	µA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	2.0	—	20	µA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 µA	

**Switching Characteristics** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

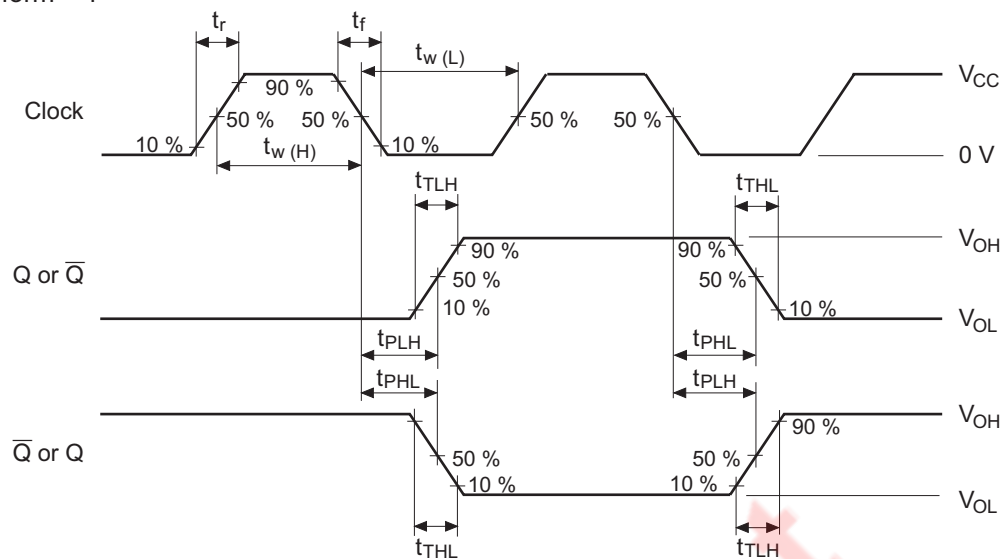
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	$t_{PLH}, t_{PHL}$	2.0	—	—	150	—	190	ns	Clock to Q or $\bar{Q}$
		4.5	—	20	30	—	38		
		6.0	—	—	26	—	33		
		2.0	—	—	140	—	175	ns	Clear to Q or $\bar{Q}$
		4.5	—	18	28	—	35		
		6.0	—	—	24	—	30		
		2.0	—	—	140	—	175	ns	Preset to Q or $\bar{Q}$
		4.5	—	16	28	—	35		
		6.0	—	—	24	—	30		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	
		4.5	20	2	—	25	—		
		6.0	17	—	—	21	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	
		4.5	5	-1	—	5	—		
		6.0	5	—	—	5	—		
Removal time	$t_{rem}$	2.0	100	—	125	—	—	ns	
		4.5	20	-2	25	—	—		
		6.0	17	—	21	—	—		
Output rise/fall time	$t_{TLH}, t_{THL}$	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

**Test Circuit**

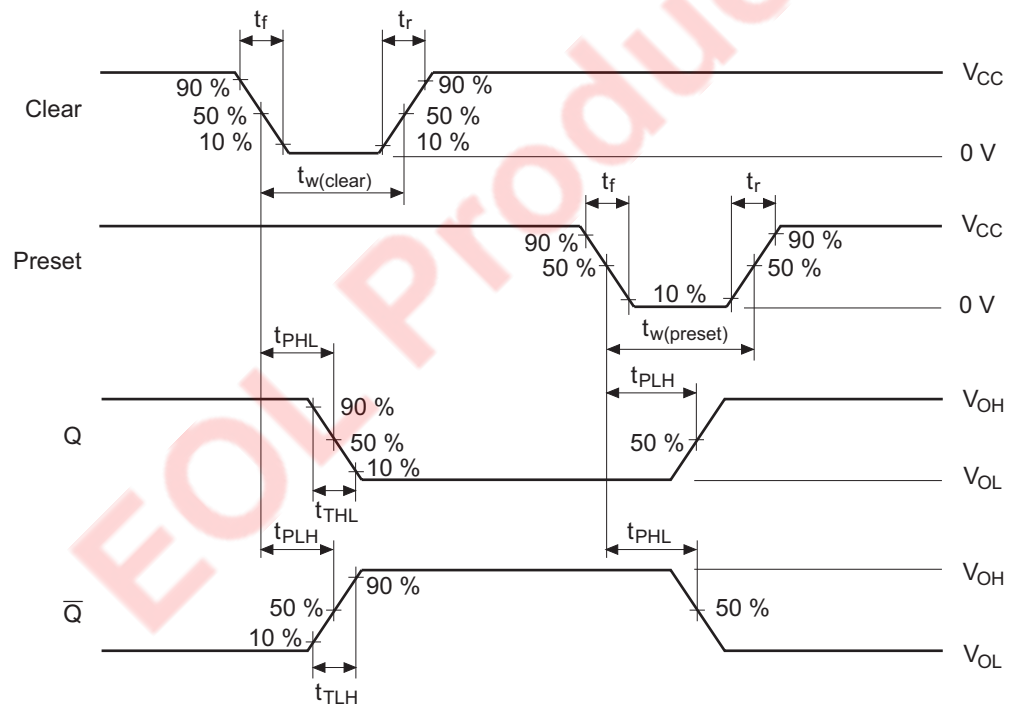
Note:  $C_L$  includes the probe and jig capacitance.

## Waveforms

## • Waveform – 1

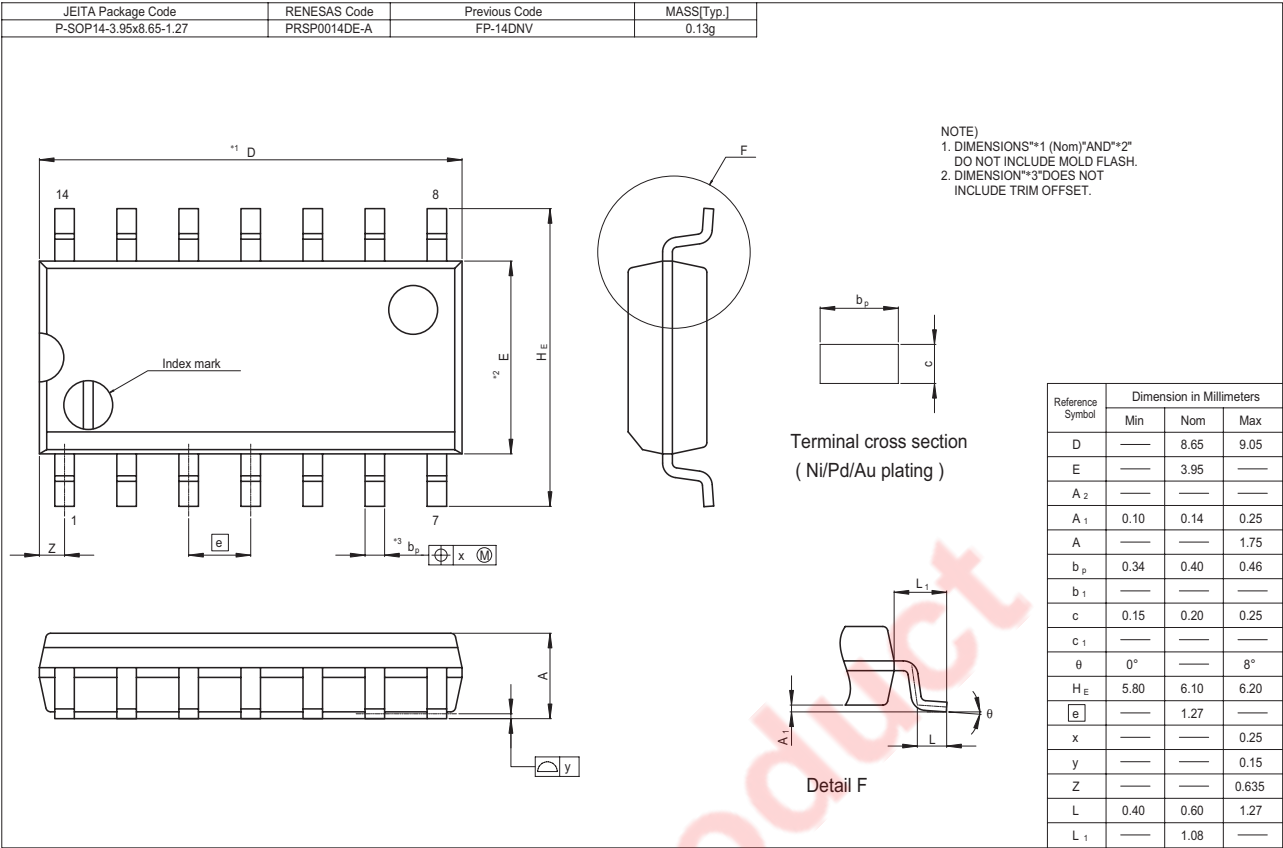


## • Waveform – 2



- Notes: 1. Input waveform:  $\text{PPR} \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$   
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions





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