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# **HD74ALVCH16374**

# 16-bit D-type Flip Flops with 3-state Outputs

REJ03D0037-0500 Rev.5.00 Jan.20.2005

### **Description**

The HD74ALVCH16374 has sixteen edge trigger D type flip flops with three state outputs in a 48 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

#### **Features**

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical  $V_{OL}$  ground bounce < 0.8 V (@ $V_{CC}$  = 3.3 V, Ta = 25°C)
- Typical  $V_{OH}$  undershoot > 2.0 V (@ $V_{CC}$  = 3.3 V, Ta = 25°C)
- High output current  $\pm 24$  mA (@V<sub>CC</sub> = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors.

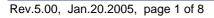
#### **Function Table**

ŌĒ	СК	D	Output Q
Н	X	X	Z
L	<b>↑</b>	L	L
L	<b>↑</b>	Н	Н
L	H or L	X	$Q_0$

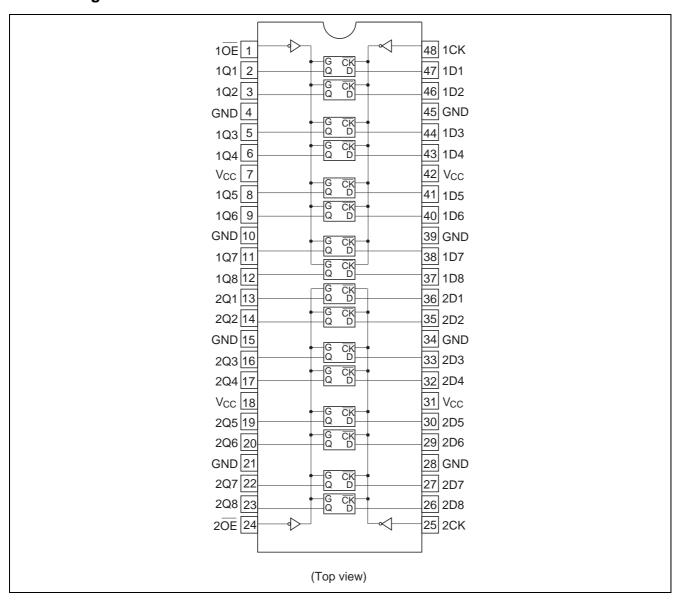
H: High level
L: Low level
X: Immaterial
Z: High impedance

↑: Low to high transition

Q<sub>0</sub>: Level of Q before the indicated steady input conditions were established.



### **Pin Arrangement**



### **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions	
Supply voltage range	V <sub>CC</sub>	-0.5 to 4.6	V		
Input voltage *1	Vı	-0.5 to 4.6	V		
Output voltage *1, 2	Vo	-0.5 to V <sub>CC</sub> +0.5	V		
Input clamp current	I <sub>IK</sub>	-50	mA	V <sub>I</sub> < 0	
Output clamp current	I <sub>OK</sub>	±50	mA	$V_O < 0$ or $V_O > V_{CC}$	
Continuous output current	I <sub>O</sub>	±50	mA	$V_O = 0$ to $V_{CC}$	
V <sub>CC</sub> , GND current / pin	I <sub>CC</sub> or I <sub>GND</sub>	±100	mA		
Maximum power dissipation at Ta = 55°C (in still air) *3	P <sub>T</sub>	0.85	W	TSSOP	
Storage temperature	Tstg	-65 to +150	°C		

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### **Recommended Operating Conditions**

Item Symbol		Ratings	Unit	Conditions	
Supply voltage	V <sub>cc</sub>	2.3 to 3.6	V		
Input / Output voltage	Vı	0 to V <sub>CC</sub>	V	ŌĒ, CK, D	
	Vo	0 to V <sub>CC</sub>	V	Q	
Operating temperature	Та	-40 to 85	°C		
Output current	Іон	-12	mA	V <sub>CC</sub> = 2.3 V	
		-12	mA	V <sub>CC</sub> = 2.7 V	
		-24	mA	V <sub>CC</sub> = 3.0 V	
	I <sub>OL</sub>	12	mA	V <sub>CC</sub> = 2.3 V	
		12	mA	V <sub>CC</sub> = 2.7 V	
		24	mA	V <sub>CC</sub> = 3.0 V	
Input rise / fall time	t <sub>r</sub> , t <sub>f</sub>	10	ns/V		

Note: Unused or floating control pins must be held high or low.

### **Electrical Characteristics**

 $(Ta = -40 \text{ to } 85^{\circ}C)$ 

Item	Symbol	V <sub>cc</sub> (V)*1	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	_	V	
		2.7 to 3.6	2.0	_	V	
	V <sub>IL</sub>	2.3 to 2.7	_	0.7	V	
		2.7 to 3.6	_	0.8	V	
Output voltage	$V_{OH}$	Min to Max	V <sub>CC</sub> -0.2	_	V	$I_{OH} = -100 \ \mu A$
		2.3	2.0	_	V	$I_{OH} = -6 \text{ mA}, V_{IH} = 1.7 \text{ V}$
		2.3	1.7	_	V	$I_{OH} = -12 \text{ mA}, V_{IH} = 1.7 \text{ V}$
		2.7	2.2	_	V	$I_{OH} = -12 \text{ mA}, V_{IH} = 2.0 \text{ V}$
		3.0	2.4	_	V	$I_{OH} = -12 \text{ mA}, V_{IH} = 2.0 \text{ V}$
		3.0	2.0	_	V	$I_{OH} = -24 \text{ mA}, V_{IH} = 2.0 \text{ V}$
	V <sub>OL</sub>	Min to Max	_	0.2	V	$I_{OL} = 100 \mu A$
		2.3	_	0.4	V	$I_{OL} = 6 \text{ mA}, V_{IL} = 0.7 \text{ V}$
		2.3	_	0.7	V	$I_{OL} = 12 \text{ mA}, V_{IL} = 0.7 \text{ V}$
		2.7	_	0.4	V	$I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$
		3.0	_	0.55	V	$I_{OL} = 24 \text{ mA}, V_{IL} = 0.8 \text{ V}$
Input current	I <sub>IN</sub>	3.6	_	±5.0	μA	$V_{IN} = V_{CC}$ or GND
	I <sub>IN(hold)</sub>	2.3	45	_	μA	$V_{IN} = 0.7 \ V$
		2.3	-45	_	μA	$V_{IN} = 1.7 \ V$
		3.0	75	_	μA	$V_{IN} = 0.8 \ V$
		3.0	<del>-</del> 75	_	μA	$V_{IN} = 2.0 \text{ V}$
		3.6	_	±500	μA	$V_{IN} = 0 \text{ to } 3.6 \text{ V}$
Off state output current *2	l <sub>OZ</sub>	3.6	_	±10	μΑ	$V_{OUT} = V_{CC}$ or GND
Quiescent supply current	Icc	3.6		40	μΑ	$V_{IN} = V_{CC}$ or GND
	Δlcc	3.0 to 3.6	_	750	μA	One input at (V <sub>CC</sub> –0.6)V, other inputs at V <sub>CC</sub> or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

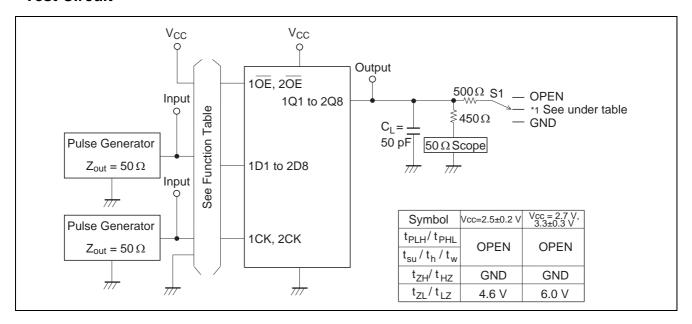
<sup>2.</sup> or I/O ports, the parameter  $I_{\text{OZ}}$  includes the input leakage current.

# **Switching Characteristics**

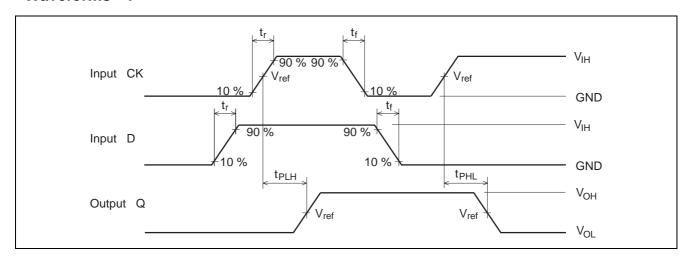
 $(Ta = -40 \text{ to } 85^{\circ}C)$ 

Item	Symbol	V <sub>CC</sub> (V)	Min	Тур	Max	Unit	From (Input)	To (Output)
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	150	_	_	MHz		
		2.7	150	_	_	MHz		
		3.3±0.3	150	_	_	MHz		
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	_	5.3	ns	CK	Q
	t <sub>PHL</sub>	2.7	_	_	4.9	ns		
		3.3±0.3	1.0	_	4.2	ns		
Output enable time	t <sub>zH</sub>	2.5±0.2	1.0	_	6.2	ns	ŌĒ	Q
	$t_{ZL}$	2.7	_	_	5.9	ns		
		3.3±0.3	1.0	_	4.8	ns		
Output disable time	t <sub>HZ</sub>	2.5±0.2	1.7	_	5.3	ns	ŌĒ	Q
	$t_{LZ}$	2.7	_	_	4.7	ns		
		3.3±0.3	1.2	_	4.3	ns		
Setup time	t <sub>su</sub>	2.5±0.2	2.1	_	_	ns		
		2.7	2.2	_	_	ns		
		3.3±0.3	1.9	_	_	ns		
Hold time	t <sub>h</sub>	2.5±0.2	0.6	_	_	ns		
		2.7	0.5	_	_	ns		
		3.3±0.3	0.5	_	_	ns		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	_	_	ns		
		2.7	3.3	_	_	ns		
		3.3±0.3	3.3	_	_	ns		
Input capacitance	C <sub>IN</sub>	3.3	_	3.0	_	pF	Contro	linputs
		3.3	_	6.0	_	pF	Inputs	
Output capacitance	Co	3.3	_	7.0	_	pF		

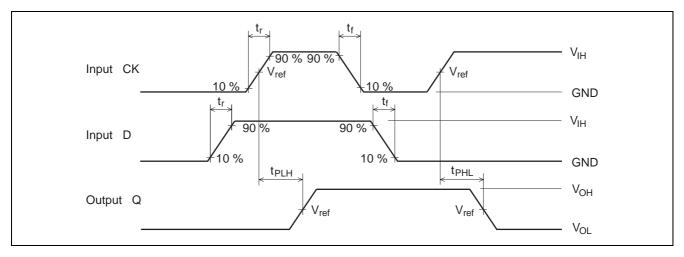
### **Test Circuit**



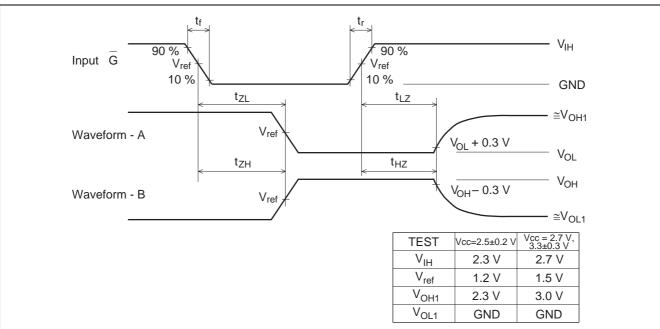
### Waveforms - 1



### Waveforms - 2



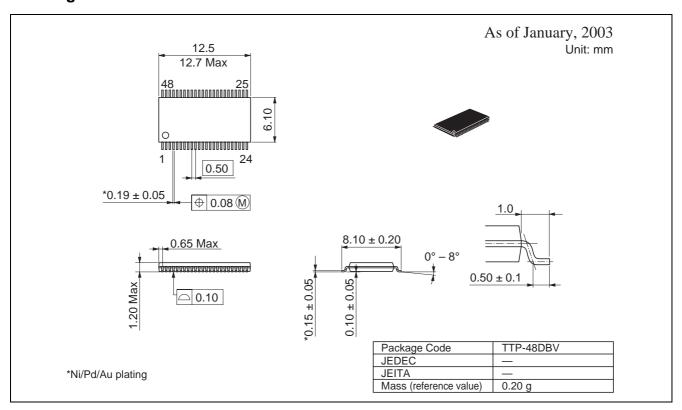
### Waveforms - 3



Notes:

- 1.  $t_r = 2.5 \text{ ns}, t_f = 2.5 \text{ ns}$
- 2. Input waveform: PRR = 10 MHz, duty cycle 50%.
- 3. Waveform—A shows input conditions such that the output is "L" level when enable by the output control.
- 4. Waveform–B shows input conditions such that the output is "H" level when enable by the output control.

## **Package Dimensions**



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Renesas Technology Europe Limited
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Renesas Technology Singapore Pte. Ltd.
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