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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74AC273

Octal D-Type Flip-Flop

REJ03D0265-0200Z
 (Previous ADE-205-386 (Z))
 Rev.2.00
 Jul.16.2004

Description

The HD74AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flops's Q output

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

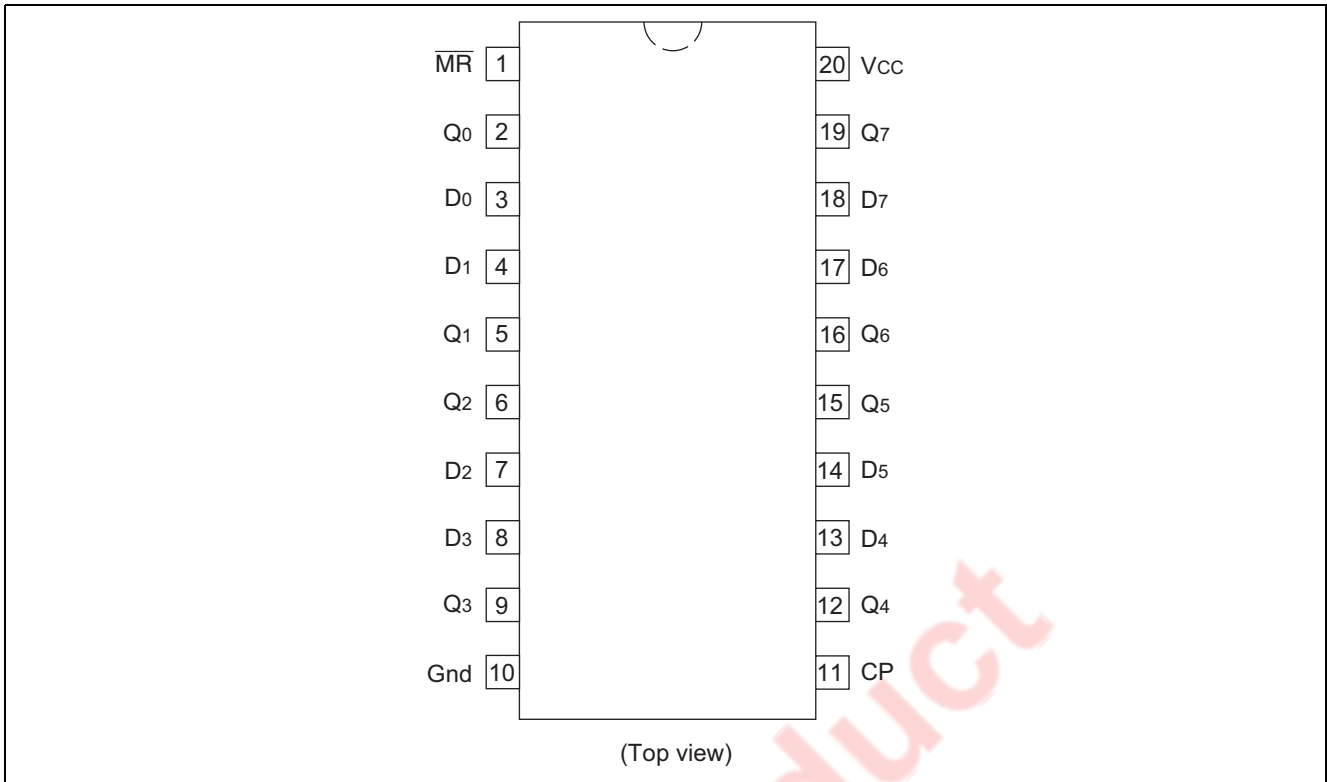
- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See HD74AC373 for Transparent Latch Version
- See HD74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC273P	DIP-20 pin	DP-20N	P	—
HD74AC273FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74AC273RPEL	SOP-20 pin (JEDEC)	FP-20DBV	RP	EL (1,000 pcs/reel)

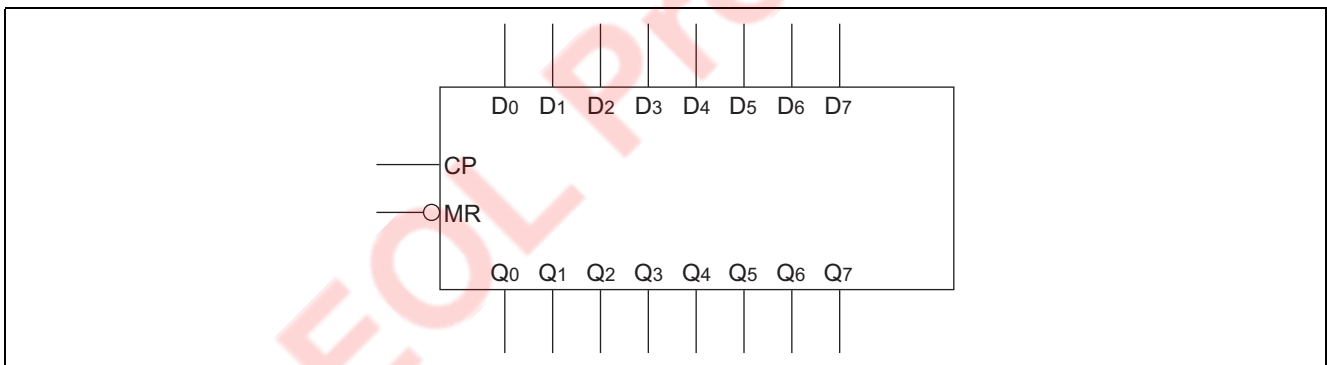
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



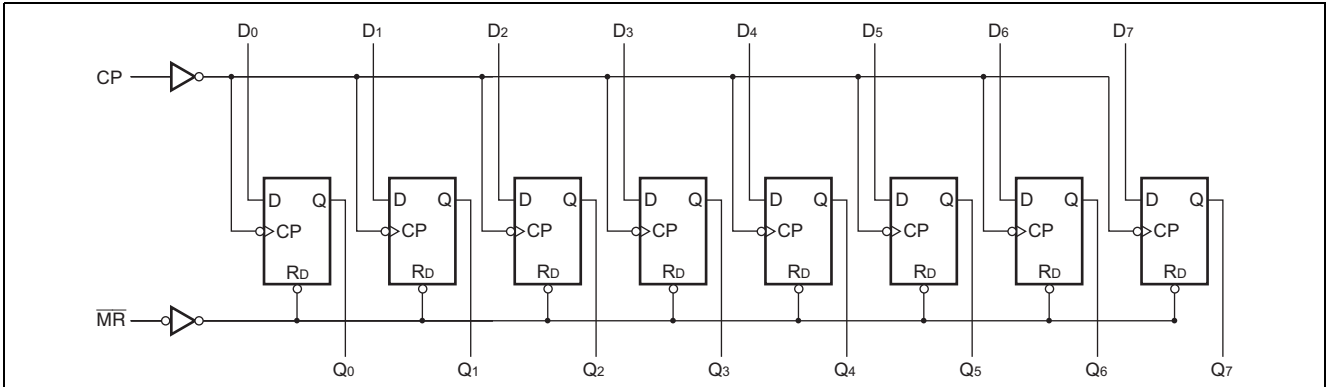
Logic Symbol



Pin Names

- $D_0 - D_7$ Data Inputs
- \overline{MR} Master Reset
- CP Clock Pulse Input
- $Q_0 - Q_7$ Data Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Mode Select-Truth Table

Operating Mode	Inputs			Outputs
	\overline{MR}	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load "1"	H		H	H
Load "0"	H		L	L

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial
- : Low-to-High Clock Transition

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	$^{\circ}C$	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5 V$
				$V_{CC} = 5.5 V$

DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition		
			min.	typ.	max.	min.	max.				
Input Voltage	V _{IH}	3.0	2.1	1.5	—	2.1	—	V	V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	3.15	2.25	—	3.15	—				
		5.5	3.85	2.75	—	3.85	—				
	V _{IL}	3.0	—	1.50	0.9	—	0.9		V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	—	2.25	1.35	—	1.35				
		5.5	—	2.75	1.65	—	1.65				
Output voltage	V _{OH}	3.0	2.9	2.99	—	2.9	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA		
		4.5	4.4	4.49	—	4.4	—				
		5.5	5.4	5.49	—	5.4	—				
		3.0	2.58	—	—	2.48	—			V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA	
		4.5	3.94	—	—	3.80	—				I _{OH} = -24 mA
		5.5	4.94	—	—	4.80	—				I _{OH} = -24 mA
	V _{OL}	3.0	—	0.002	0.1	—	0.1		V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 μA		
		4.5	—	0.001	0.1	—	0.1				
		5.5	—	0.001	0.1	—	0.1				
		3.0	—	—	0.32	—	0.37			V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA	
		4.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
		5.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
Input leakage current	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND		
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V		
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V		
Quiescent supply current	I _{CC}	5.5	—	—	8.0	—	80	μA	V _{IN} = V _{CC} or ground		

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	90	125	—	75	—	MHz
		5.0	140	175	—	125	—	
Propagation delay Clock to output	t _{PLH}	3.3	1.0	7.0	12.5	1.0	14.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay Clock to output	t _{PHL}	3.3	1.0	7.0	13.0	1.0	14.5	ns
		5.0	1.0	5.0	10.0	1.0	11.0	
Propagation delay MR to output	t _{PHL}	3.3	1.0	7.0	13.0	1.0	14.0	ns
		5.0	1.0	5.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW Data to CP	t _{SU}	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
Hold time, HIGH or LOW Data to CP	t _H	3.3	-2.0	0.0	0.0	ns
		5.0	-1.0	1.0	1.0	
Clock pulse width HIGH or LOW	t _w	3.3	3.5	5.5	6.0	ns
		5.0	2.5	4.0	4.5	
MR Pulse width HIGH or LOW	t _w	3.3	2.0	5.5	6.0	ns
		5.0	1.5	4.0	4.5	
Recovery time MR to CP	t _{REC}	3.3	1.5	3.5	4.5	ns
		5.0	1.0	2.0	3.0	

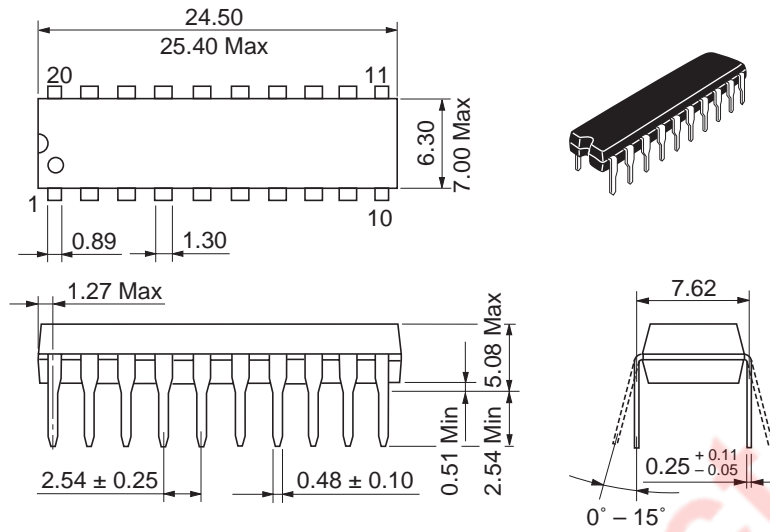
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	50.0	pF	V _{CC} = 5.0 V

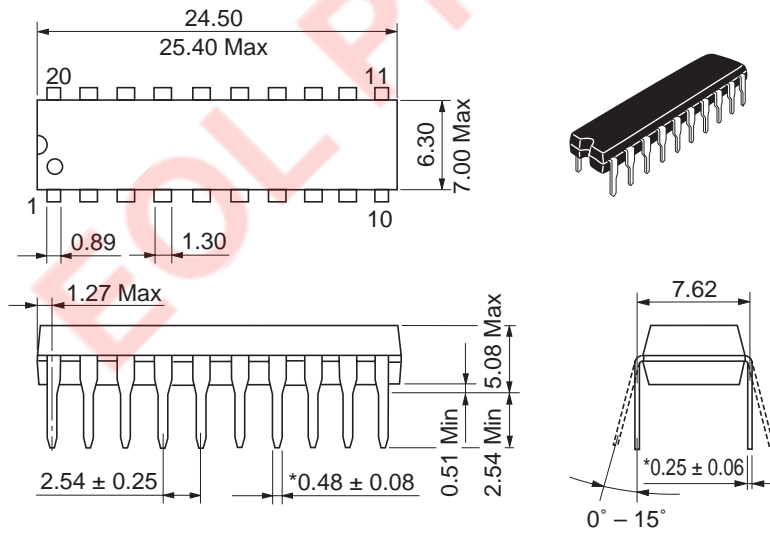
Package Dimensions

As of January, 2003
Unit: mm



Package Code	DP-20N
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

Unit: mm

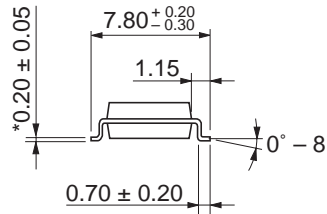
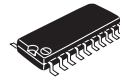
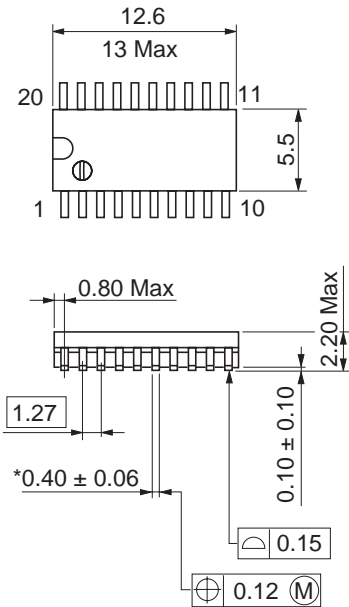


*Ni/Pd/AU Plating

Package Code	DP-20NEV
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

As of January, 2003

Unit: mm

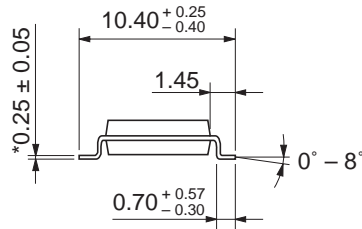
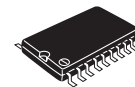
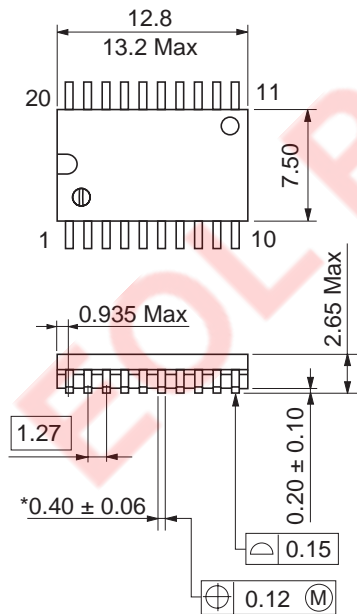


*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

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