

## GENERAL DESCRIPTION

This document describes the specification for the IDTF1370 **D**igital **P**re-**D**istortion Demodulator for PA linearization. This series of devices is offered in 2 variants to cover common UTRA bands. See part number matrix below for additional detail.

## COMPETITIVE ADVANTAGE

In typical basestation transmitters digital pre-distortion is employed to improve the Transmitter performance. The signal coming out of the PA is sampled and the incoming Tx chain I&Q data is pre-distorted to counteract the distortion inherent in the PA. The PA signal is adjusted via a digital step attenuator to a lower level and then sub-sampled at an IF frequency of ~200 MHz which necessitates the need for a highly linear demodulator to downmix to quadrature IF from the Transmit frequency. By sampling IF\_I and IF\_Q independently and then digitally combining these signals, an effective doubling of the sample rate can be achieved. Any distortion in this path will degrade the performance of the DPD algorithm. By utilizing an ultra-linear demodulator w/integrated DSA such as the IDTF1370, the ACLR and/or power consumption of the full Tx system can be improved significantly.

- ✓ DPD full path ACLR: ↓ **1 dB**
- ✓ I<sub>cc</sub>: DPD function Power Consumption ↓ **40%**
- ✓ **Zero-Distortion™ Demod** eliminates **2 IF amps**
- ✓ **Integrates 2 BPFs, 2 Baluns, SPDT RF switch**
- ✓ Glitch-Free™ gain control



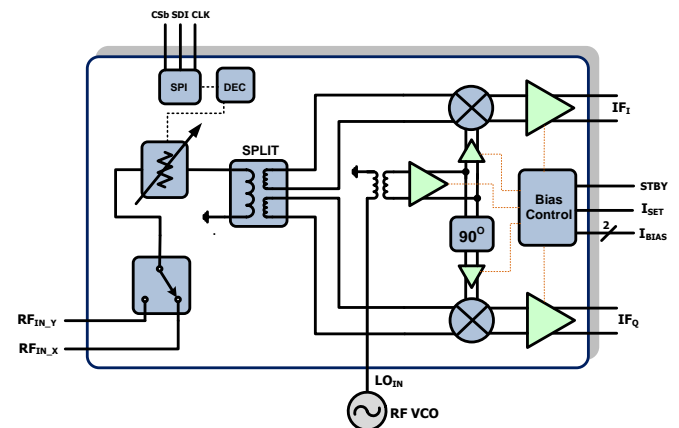
## PART# MATRIX

| Part# | RF range    | UTRA bands                | IF freq range | Typ. Gain | Injection             |
|-------|-------------|---------------------------|---------------|-----------|-----------------------|
| F1320 | 550 - 1150  | 5,6,8,12,13,14,17         | 20 - 350      | 12.5      | High Side or Low Side |
| F1370 | 1300 - 2900 | 1,2,3,4,9,10,7,21, 24, 38 | 20 - 500      | 12.5      | High Side or Low Side |

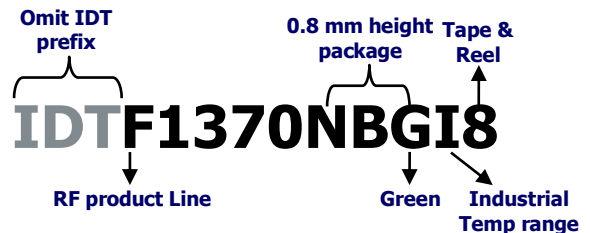
## FEATURES (I OR Q PATH)

- Wide flat performance IF BW
- Wide RF and LO BWs (~ 1.6 GHz)
- Ideal for Multi-Carrier Systems
- **Drives ADC directly**
- Ultra linear **+41 dBm IP<sub>3o</sub>**
- Low Noise Figure
- Excellent ACLR performance
- **200 Ω** output impedance
- Fully integrated DPD demodulator
- **6x6 36 pin package**
- Standby Mode w/Fast Recovery
- I<sub>cc</sub>: **275 mA**

## DEVICE BLOCK DIAGRAM



## ORDERING INFORMATION



## ABSOLUTE MAXIMUM RATINGS

|   |                                  |
|---|----------------------------------|
| V <sub>CC</sub> to GND  | -0.3V to +5.5V                   |
| SW_Latch, DATA, CSb, CLK  | 0V to 3.6V                       |
| STBY  | 0V to V <sub>CC</sub>            |
| IF_I+, IF_I-, IF_Q+, IF_Q-  | 1V to (V <sub>CC</sub> + 0.3V)   |
| LO_IN   | -0.3V to +0.3V                   |
| RF_INX, RF_INY  | -0.3V to +0.3V                   |
| IF_BiasI, IF_BiasQ to GND   | -0.3V to +1.2V                   |
| LO_ADJ to GND   | 2.1V to 4.0V                     |
| RF Input Power (Into RFIN_X or RFIN_Y)                                      | <b>+27 dBm</b>                   |
| Continuous Power Dissipation  | 2.5W                             |
| θ <sub>JA</sub> (Junction – Ambient)  | +40°C/W                          |
| θ <sub>JC</sub> (Junction – Case) The Case is defined as the exposed paddle | +3°C/W                           |
| Operating Temperature Range (Case Temperature)                              | T <sub>C</sub> = -40°C to +105°C |
| Maximum Junction Temperature  | 150°C                            |
| Storage Temperature Range   | -65°C to +150°C                  |
| Moisture Sensitivity Level  | <b>1</b>                         |
| Lead Temperature (soldering, 10s)   | +260°C                           |

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### ESD Caution

*This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.*



## IDTF1370 SPECIFICATION

Specifications apply at  $V_{CC} = +5.0V$ ,  $T_C = 25C$ ,  $F_{RF} = 2100 \text{ MHz}$ ,  $F_{LO} = 2300 \text{ MHz}$ , Gain =  $G_{MAX}$ ,  $P_{LO} = 0 \text{ dBm}$ ,  $T_C = +25^\circ C$ , STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF input trace losses de-embedded.

| Parameter                       | Comment   | Symbol              | min                     | typ          | max         | units    |
|---------------------------------|---|---------------------|-------------------------|--------------|-------------|----------|
| Logic Input High                | FOR STBY, DATA, CSb, CLK, SW_Latch  | $V_{IH}$            | <b>2.3</b>              |              |             | V        |
| Logic Input Low                 | FOR STBY, DATA, CSb, CLK, SW_Latch  | $V_{IL}$            |                         |              | <b>0.5</b>  | V        |
| Logic Current                   | $V_H = 2.3V$ , $V_L = 0V$   | $I_{IH}$ , $I_{IL}$ | <b>-120</b>             |              | <b>+100</b> | $\mu A$  |
| Supply Voltage(s)               | All $V_{CC}$ (operating range)  | $V_{CC}$            |                         | 4.75 to 5.25 |             | V        |
| Temperature Range               | Operating Range   | $T_{CASE}$          | -40                     |              | +105        | degC     |
| Supply Current                  | Total $V_{CC}$  | $I_{SUPP}$          |                         | <b>275</b>   | <b>325</b>  | mA       |
| Supply Current                  | Standby Mode: STBY > $V_{IH}$   | $I_{STBY}$          |                         | <b>30</b>    | <b>40</b>   | mA       |
| RF Freq Range                   | Sets LO freq range  | $F_{RF}$            | 1450                    |              | 2700        | MHz      |
| IF center Freq Range            | Sets LO freq range  | $F_{IF}$            | 100                     |              | 300         | MHz      |
| Oversample RF Range             | <ul style="list-style-type: none"> <li>▪ Measure Gain at I&amp;Q</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> <li>▪ <math>F_{LO} = 1800 \text{ MHz}</math>, <math>2920 \text{ MHz}</math></li> <li>▪ Gain Delta &lt; 2.5 dB</li> </ul> | $F_{RFD}$           | <b>1300</b>             |              | <b>2900</b> | MHz      |
| Oversample IF Range             | <ul style="list-style-type: none"> <li>▪ Measure Gain at I&amp;Q</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> <li>▪ <math>F_{LO} = 1800 \text{ MHz}</math>, <math>2920 \text{ MHz}</math></li> <li>▪ Gain Delta &lt; 2.5 dB</li> </ul> | $F_{IFD}$           | <b>20</b>               |              | <b>500</b>  | MHz      |
| IF Linearity BW                 | <ul style="list-style-type: none"> <li>▪ RF Freq = 2100 MHz</li> <li>▪ IP3O &gt; +38 dBm</li> <li>▪ From RF_INX to I+,I- &amp; Q+,Q-</li> <li>▪ Pin = -11 dBm/Tone;</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> </ul>                 | $IF_{LIN}$          | 100                     |              | 300         | MHz      |
| RF Linearity BW                 | <ul style="list-style-type: none"> <li>▪ IF Freq = 200 MHz</li> <li>▪ IP3O &gt; +39 dBm</li> <li>▪ From RF_INX to I+,I- &amp; Q+,Q-</li> <li>▪ Pin = -11 dBm/Tone</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> </ul>                   | $RF_{LIN}$          | 1600                    |              | 2700        | MHz      |
| LO Freq Range                   | <ul style="list-style-type: none"> <li>▪ Operating Range</li> </ul>   | $F_{LO}$            | 1400                    |              | 2900        | MHz      |
| LO Power                        |   | $P_{LO}$            |                         | -3 to +3     |             | dBm      |
| RF Input Impedance              | Single Ended (RL > 10 dB)   | $Z_{RF}$            |                         | 50           |             | $\Omega$ |
| IF Output Impedance             | Differential (RL > 10 dB)   | $Z_{IF}$            |                         | 200          |             | $\Omega$ |
| LO port Impedance               | Single Ended (RL > 10 dB)   | $Z_{LO}$            |                         | 50           |             | $\Omega$ |
| Gain maximum                    | <ul style="list-style-type: none"> <li>▪ From RF_INX to I+,I- &amp; Q+,Q-</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> <li>▪ Pin = -11 dBm</li> </ul>  | $G_{MAX}$           | <b>10.8<sup>1</sup></b> | <b>12.5</b>  | <b>13.8</b> | dB       |
| Gain maximum Low Side Injection | <ul style="list-style-type: none"> <li>▪ From RF_INX to I+,I- &amp; Q+,Q-</li> <li>▪ Gain setting = <math>G_{MAX}</math></li> <li>▪ Pin = -11 dBm</li> <li>▪ RF = 2000MHz</li> <li>▪ LO = 1800MHz</li> </ul>                                  | $G_{MAX\_LSLO}$     |                         | 12.7         |             | dB       |
| Gain minimum                    | <ul style="list-style-type: none"> <li>▪ From RF_INX to I+,I- &amp; Q+,Q-</li> <li>▪ Gain setting = <math>G_{MIN}</math></li> <li>▪ Pin = +14 dBm</li> </ul>  | $G_{MIN}$           | <b>-13.5</b>            | <b>-12.8</b> | <b>-12</b>  | dB       |

## IDTF1370 SPECIFICATION - CONTINUED

Specifications apply at  $V_{CC} = +5.0V$ ,  $T_C = 25C$ ,  $F_{RF} = 2100\text{ MHz}$ ,  $F_{LO} = 2300\text{ MHz}$ , Gain =  $G_{MAX}$ ,  $P_{LO} = 0\text{ dBm}$ ,  $T_C = +25^\circ C$ , STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF input trace losses de-embedded.

| Parameter                                    | Comment  | Symbol             | min         | typ        | max        | units   |
|--|--|--------------------|-------------|------------|------------|---------|
| Noise Figure                                 | <ul style="list-style-type: none"> <li>From RF_INX to I+,I- &amp; Q+,Q-</li> <li>Gain setting = <math>G_{MAX}</math></li> </ul>  | NF                 |             | 17.4       |            | dB      |
| Output IP3 – $G_{MAX}$                       | <ul style="list-style-type: none"> <li>Measured at I+,I- and Q+,Q-</li> <li><math>P_{IN} = -11\text{ dBm}</math> per tone</li> <li>5 MHz Tone Separation</li> <li>Gain setting = <math>G_{MAX}</math></li> </ul> | $IP3_{MAX}$        | <b>36</b>   | <b>41</b>  |            | dBm     |
| Output IP3 – $G_{-20}$                       | <ul style="list-style-type: none"> <li>Measured at I+,I- and Q+,Q-</li> <li><math>P_{IN} = +9\text{ dBm}</math> per tone</li> <li>5 MHz Tone Separation</li> <li>Gain setting = <math>G_{-20}</math></li> </ul>  | $IP3_{-20}$        | $38^2$      | 40         |            | dBm     |
| 2 <sup>nd</sup> Harmonic                     | <ul style="list-style-type: none"> <li>Measured at I+,I- and Q+,Q-</li> <li><math>P_{IN} = -11\text{ dBm}</math></li> <li>Gain setting = <math>G_{MAX}</math></li> </ul>   | H2                 | -68         | -75        |            | dBc     |
| Output IP2                                   | <ul style="list-style-type: none"> <li>Measured at I+,I- and Q+,Q-</li> <li><math>P_{IN} = -11\text{ dBm}</math> per tone</li> <li>5 MHz Tone Separation</li> <li>Gain setting = <math>G_{MAX}</math></li> </ul> | $IP2_O$            | 63          | 69         |            | dBm     |
| Output compression                           | <ul style="list-style-type: none"> <li>Measured at I+,I- and Q+,Q-</li> <li><math>P_{IN} = +4\text{ dBm}</math></li> <li>Gain setting = <math>G_{MAX}</math></li> </ul>  | C                  |             | <b>0.2</b> | <b>1</b>   | dB      |
| Gain Ripple                                  | <ul style="list-style-type: none"> <li>Fixed LO = 2300 MHz</li> <li>RF = 1800 to 2280 MHz</li> <li>IF = 20 to 500 MHz</li> </ul>   | Ripple             |             | 0.8        | 1.3        | dB      |
| Group Delay Distortion                       | <ul style="list-style-type: none"> <li>Fixed LO = 2300</li> <li>RF = 1800 to 2280 MHz</li> <li>IF = 20 to 500 MHz</li> </ul>   | GDD                |             | 5          |            | nsec    |
| Quadrature Amplitude Balance                 | Calculated from Data from Oversample RF range Tests  | $BAL_G$            | <b>-0.3</b> |            | <b>0.3</b> | dB      |
| Quadrature Phase Balance                     | Measure with 20 GSa/sec scope  | $BAL_\phi$         | -2.6        | -1.5       | 0          | degrees |
| Amplitude Balance over environmentals        | <ul style="list-style-type: none"> <li><math>T_C = -40C</math> to <math>105C</math></li> <li>LO drive = -3 dBm to +3 dBm</li> <li>Measure with 20 GSa/sec scope</li> </ul>                                       | $BAL_{G\Delta}$    | -0.5        |            | +0.4       | dB      |
| Quadrature Phase Balance over environmentals | <ul style="list-style-type: none"> <li><math>T_C = -40C</math> to <math>105C</math></li> <li>LO drive = -3 dBm to +3 dBm</li> <li>Measure with 20 GSa/sec scope</li> </ul>                                       | $BAL_{\phi\Delta}$ | -3          |            | +2         | degrees |
| LO to IF leakage                             | Output balun not de-embedded   | $ISO_{LI}$         |             | -33        | -28        | dBm     |
| LO to RF leakage                             |  | $ISO_{LR}$         |             | -42        |            | dBm     |
| RF to IF isolation                           | Output balun not de-embedded   | $ISO_{RI}$         |             | -54        | -46        | dBc     |
| Attenuator Range                             |  | Range              |             | 25.5       |            | dB      |

## IDTF1370 SPECIFICATION - CONTINUED

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| Parameter  | Comment   | Symbol       | min | typ        | max         | units |  |
|--|---|--------------|-----|------------|-------------|-------|--|
| Attenuator Glitching                                       | <ul style="list-style-type: none"> <li>▪ Step from 15.5 to 16 dB</li> <li>▪ Step from 16 to 15.5 dB</li> <li>▪ Measure maximum excursion</li> </ul> | $ATTN_G$     |     | 0.7        |             | dB    |  |
| Attenuator Step Accuracy                                   |   | DNL          |     | 0.2        |             | dB    |  |
| Attenuator Abs. Accuracy                                   |   | INL          |     | <b>0.2</b> | <b>0.75</b> | dB    |  |
| Attenuator Resolution                                      |   | LSB          |     | 0.5        |             | dB    |  |
| Serial Clock Speed   | SPI 3 wire bus  | $F_{CLOCK}$  |     | <b>20</b>  | <b>50</b>   | MHz   |  |
| Data to Clock Setup  | SPI 3 wire bus  | $T_S$        | 3   |            |             | ns    |  |
| Data to Clock Hold   | SPI 3 wire bus  | $T_H$        | 3   |            |             | ns    |  |
| Clock to CS Setup  | SPI 3 wire bus  | $T_{EN}$     | 3   |            |             | ns    |  |
| Clock Pulse Width  | SPI 3 wire bus  | $T_W$        | 5   |            |             | ns    |  |
| RF Switch Isolation  | $F_{RF} < 2.0\text{ GHz}$   | $ISO_{RFSW}$ |     | -41        |             | dBc   |  |
| <b>RF Switch and attenuator settling times<sup>3</sup></b> |   |              |     |            |             |       |  |
| EN bit on  | <ul style="list-style-type: none"> <li>• LO_INA: 2300MHz, 0dBm</li> <li>• RF_INX: 2100MHz, -11dBm</li> </ul>  | $EN_{ON}$    |     | 100        |             | nsec  |  |
| EN bit off   |   | $EN_{OFF}$   |     | 50         |             |       |  |
| RF switched X to Y (no Y signal)                           |   | $RF_{SWXY}$  |     | 150        |             |       |  |
| RF switched Y to X (no Y signal)                           |   | $RF_{SWYX}$  |     | 200        |             |       |  |
| Attenuator switched 0dB to 25.5dB (max)                    |   | $ATT_{SETL}$ |     |            | 300         |       |  |
| Attenuator switched 25.5dB (max) to 0dB                    |   |              |     |            | 300         |       |  |
| Attenuator switched 15.5dB to 16dB                         |   |              |     |            | 250         |       |  |
| Attenuator switched 16dB to 15.5dB                         |   |              |     |            | 250         |       |  |

### SPECIFICATION NOTES:

- 1 – Items in min/max columns in **bold italics** are Guaranteed by Test
- 2 – All other Items in min/max columns are Guaranteed by Design Characterization
- 3 – Excludes SPI write time

## POWER-ON SEQUENCE

The power-on sequence ensures F1370 works in default mode once powered on. If the F1370 is programmed after applying DC power, the following power-on sequence is not needed. Note: To use power on sequence, SW\_LATCH cannot be grounded permanently.

The power-on sequence should be:

1. CSb & SW\_LATCH must be set low at power-on
2. Once powered on, first set SW\_LATCH high, then set CSb high
3. Proceed with normal programming.

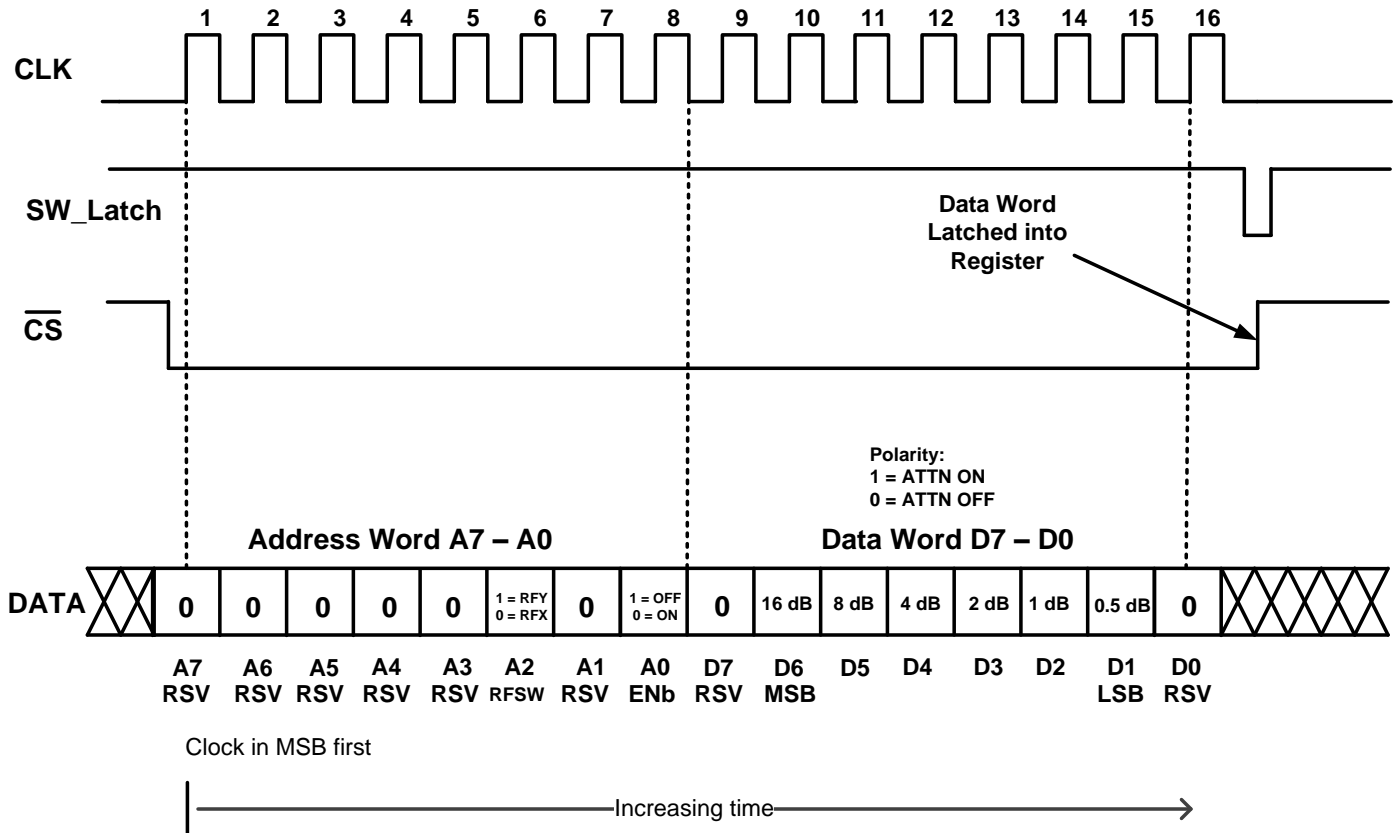
The default state after using power-on sequence:

- Maximum attenuation
- RF\_INX selected
- Normal operation (not Standby Mode)

## SERIAL PROGRAMMING

The device is programmed via the serial port by asserting Chip Select (CSb). Note: Most-Significant-Bit first, where the Address Word is the Most-Significant-Byte.

### Serial mode timing diagram high level:

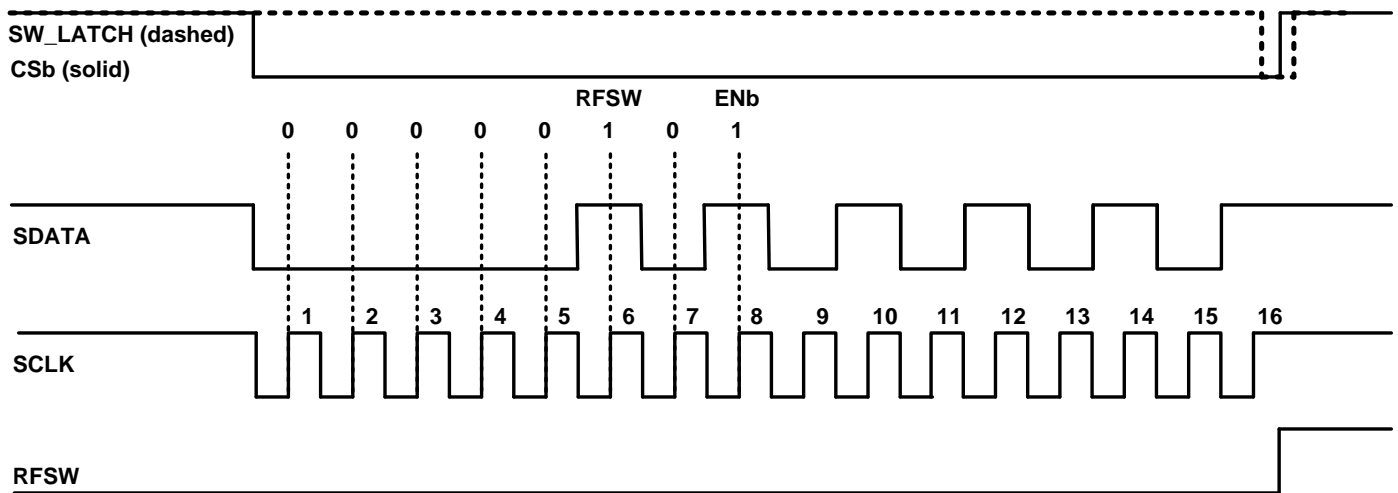


## TO PROGRAM THE SERIAL INTERFACE:

If CSb is de-asserted (set to high), the serial interface will ignore the CLK line. Once CSb is asserted (set to low), the serial interface will recognize the CLK and any data present on DATA will be clocked into the registers with each rising CLK edge. After the 16<sup>th</sup> CLK cycle, and before the 17<sup>th</sup> CLK cycle, CSb must be de-asserted to successfully program the part with the desired bytes. If CSb is de-asserted before the 16<sup>th</sup> CLK cycle, or after the 17<sup>th</sup> CLK cycle, there is no guarantee that the correct bytes will be programmed and the user will have to re-program the interface in accordance with the aforementioned procedure.

## SW\_LATCH PROGRAMMING SEQUENCE

- When SW\_LATCH is pinned high during the programming sequence, “RFSW” and “ENb” registers cannot be programmed and therefore will not toggle.
- If SW\_LATCH is pinned low during the programming sequence, the “RFSW” and “ENb” register will toggle. This can be prevented with the “Programming Sequence” below.



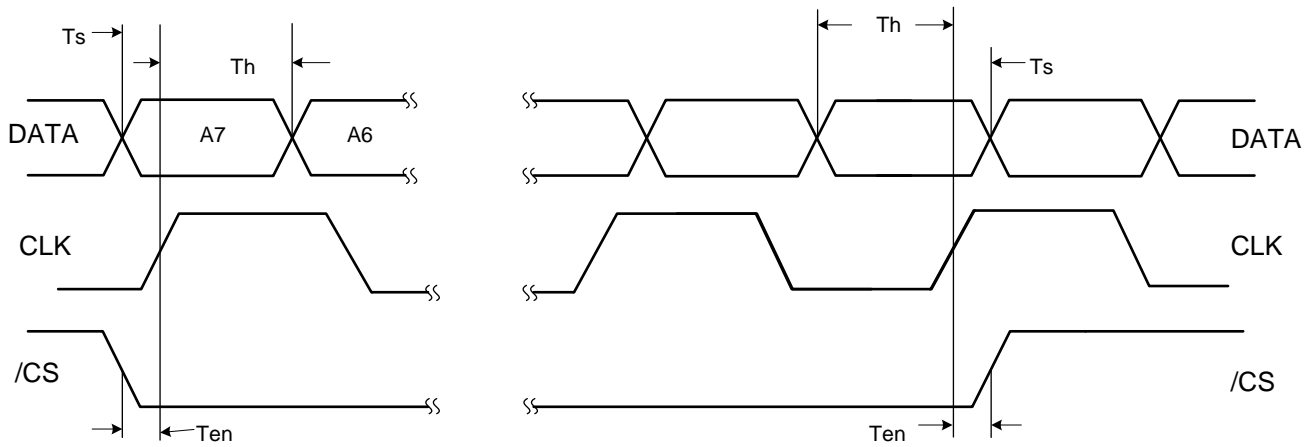
## SEQUENCE FOR PROGRAMMING REGISTERS A<2>:A<0>

- 1) SW\_Latch = 1; CSb = 0
- 2) CLK in 8- or 16-bit word, *do not de-assert (pull high) CSb*
- 3) Set SW\_LATCH = 0 while CSb = 0 remains)
- 4) With SW\_Latch = 0, set CSb = 1
- 5) Set SW\_Latch = 1
- 6) Program complete

## SPECIAL NOTE REGARDING PHASE OF I & Q:

- When LO is high-side injected, IF\_I leads IF\_Q by 90 degrees
- When LO is low-side injected, IF\_Q leads IF\_I by 90 degrees

## SERIAL MODE TIMING DIAGRAM ZOOM:



- Data is shifted with the rising edge of CLK when /CS is low
- The rising edge of /CS latches data into the device

## LOGIC TRUTH TABLE:

| STBY | SW_LATCH | MODE           | WRITE ACCESS                  |
|------|----------|----------------|-------------------------------|
| 0    | 0        | Operating Mode | A2:A0 Enabled, D7:D0 Enabled  |
| 0    | 1        | Operating Mode | A2:A0 Disabled, D7:D0 Enabled |
| 1    | 0        | Off            | A2:A0 Enabled, D7:D0 Enabled  |
| 1    | 1        | Off            | A2:A0 Disabled, D7:D0 Enabled |



### F1370 ATTENUATION TABLE

The F1370 gain/attenuation setting is controlled by 6 bits in the data word. The device provides an added attenuation range from 0 dB to 25.5 dB in 0.5 dB steps. A “high” or “1” bit corresponds to attenuation stepped IN, while a “low” or “0” bit corresponds to attenuation stepped OUT.

| F1370 DPD Demodulator - Attenuation Table (Data Word D7-D0) |     |                  |  |          |     |                  |
|---|-----|------------------|--|----------|-----|------------------|
| BINARY  | HEX | Added Atten (dB) |  | BINARY   | HEX | Added Atten (dB) |
| 00000000  | 00  | 0                |  | 00110100 | 34  | 13               |
| 00000010  | 02  | 0.5              |  | 00110110 | 36  | 13.5             |
| 00000100  | 04  | 1                |  | 00111000 | 38  | 14               |
| 00000110  | 06  | 1.5              |  | 00111010 | 3A  | 14.5             |
| 00001000  | 08  | 2                |  | 00111100 | 3C  | 15               |
| 00001010  | 0A  | 2.5              |  | 00111110 | 3E  | 15.5             |
| 00001100  | 0C  | 3                |  | 01000000 | 40  | 16               |
| 00001110  | 0E  | 3.5              |  | 01000010 | 42  | 16.5             |
| 00010000  | 10  | 4                |  | 01000100 | 44  | 17               |
| 00010010  | 12  | 4.5              |  | 01000110 | 46  | 17.5             |
| 00010100  | 14  | 5                |  | 01001000 | 48  | 18               |
| 00010110  | 16  | 5.5              |  | 01001010 | 4A  | 18.5             |
| 00011000  | 18  | 6                |  | 01001100 | 4C  | 19               |
| 00011010  | 1A  | 6.5              |  | 01001110 | 4E  | 19.5             |
| 00011100  | 1C  | 7                |  | 01010000 | 50  | 20               |
| 00011110  | 1E  | 7.5              |  | 01010010 | 52  | 20.5             |
| 00100000  | 20  | 8                |  | 01010100 | 54  | 21               |
| 00100010  | 22  | 8.5              |  | 01010110 | 56  | 21.5             |
| 00100100  | 24  | 9                |  | 01011000 | 58  | 22               |
| 00100110  | 26  | 9.5              |  | 01011010 | 5A  | 22.5             |
| 00101000  | 28  | 10               |  | 01011100 | 5C  | 23               |
| 00101010  | 2A  | 10.5             |  | 01011110 | 5E  | 23.5             |
| 00101100  | 2C  | 11               |  | 01100000 | 60  | 24               |
| 00101110  | 2E  | 11.5             |  | 01100010 | 62  | 24.5             |
| 00110000  | 30  | 12               |  | 01100100 | 64  | 25               |
| 00110010  | 32  | 12.5             |  | 01100110 | 66  | 25.5             |

Because the first and last bits of the Data Word are not presently used by the F1370, two additional hex character pairs exists for each of those in this table. For example, data words of either H00, H80, or H01 (binary “00000000,” “10000000,” or 00000001) will place the F1370 in its minimum attenuation state. Likewise, data words of either H66, HE6, or H67 (binary “01100110” or “11100110” or “01100111”) will place the F1370 in its maximum attenuation state of 25.5 added attenuation.

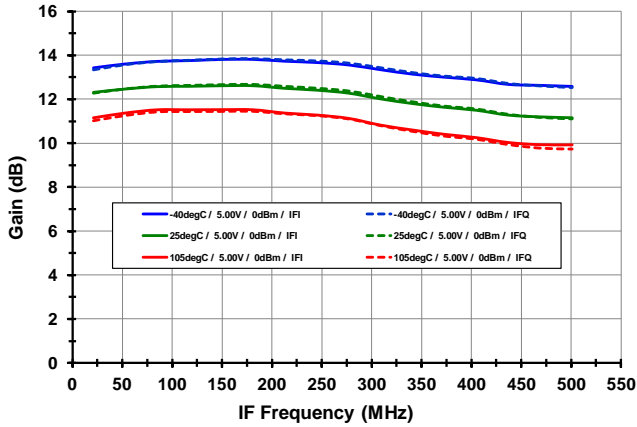
## TYPICAL OPERATING CONDITIONS

Unless otherwise noted for the TOC graphs, the following conditions apply

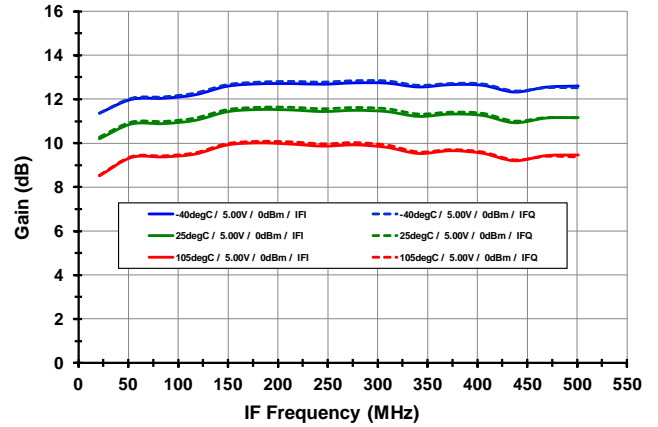
- IF = 200 MHz
- Tone spacing = 5 MHz
- Pin = - 11 dBm / Tone
- Pout ~ 1 dBm / Tone
- RF\_X, IF\_Q selected
- Minimum Attenuation selected (0 dB ATTN)
- V<sub>CC</sub> = 5.00 V
- LO level = 0 dBm
- Case Temperature = 25C
- All Temperatures are Case Temperature (T<sub>CASE</sub>)
- Output Transformers are de-embedded
- Input RF trace losses are de-embedded

## TOCs F1370 [FIXED LO vs TEMP] (-1-)

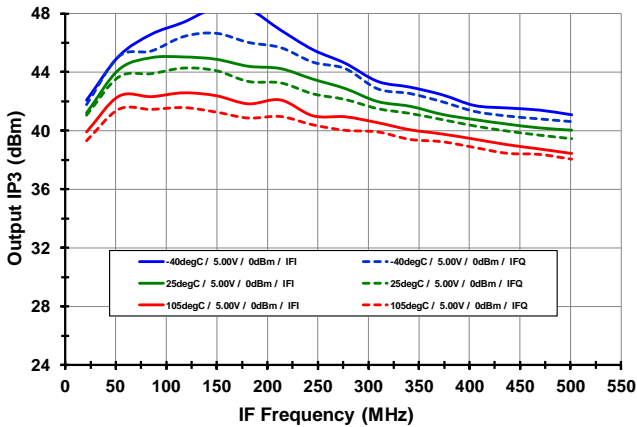
### GAIN [LO = 1.80 GHz, LOW SIDE INJECTION]



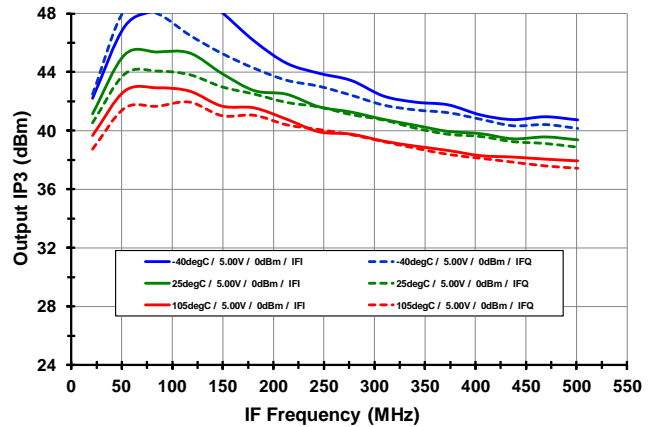
### GAIN [LO = 2.92 GHz, HIGH SIDE INJECTION]



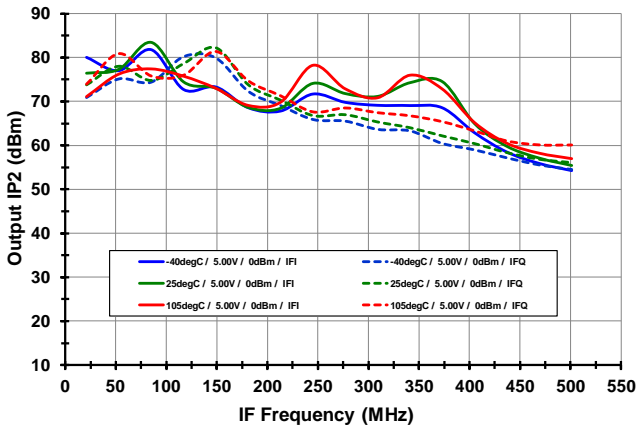
### IP3<sub>O</sub> [LO = 1.80 GHz, LOW SIDE INJECTION]



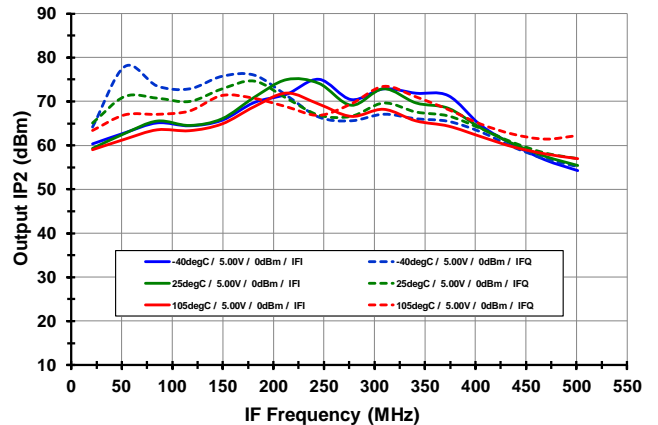
### IP3<sub>O</sub> [LO = 2.92 GHz, HIGH SIDE INJECTION]



### IP2<sub>O</sub> [LO = 1.80 GHz, LOW SIDE INJECTION]

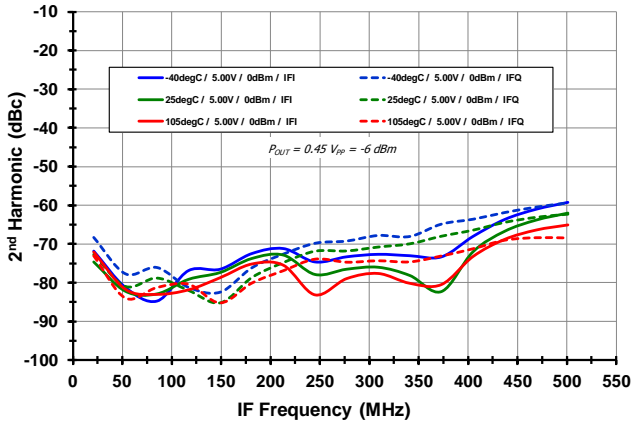


### IP2<sub>O</sub> [LO = 2.92 GHz, HIGH SIDE INJECTION]

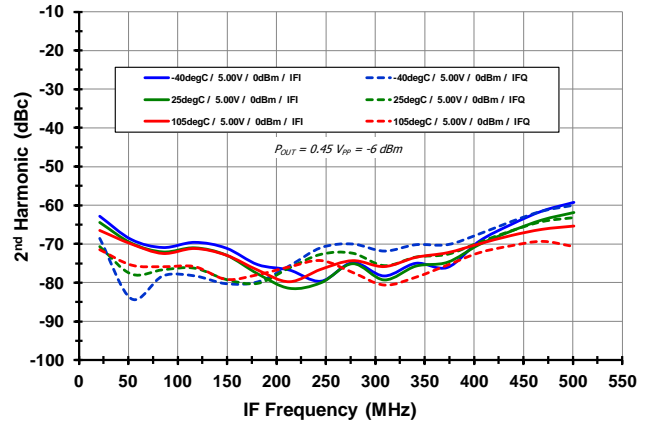


## TOCs F1370 [FIXED LO vs TEMP] (-2-)

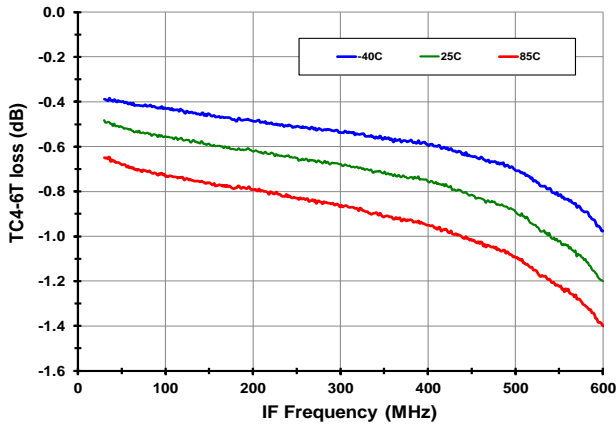
### H2 [LO = 1.8 GHz, LOW SIDE INJECTION]



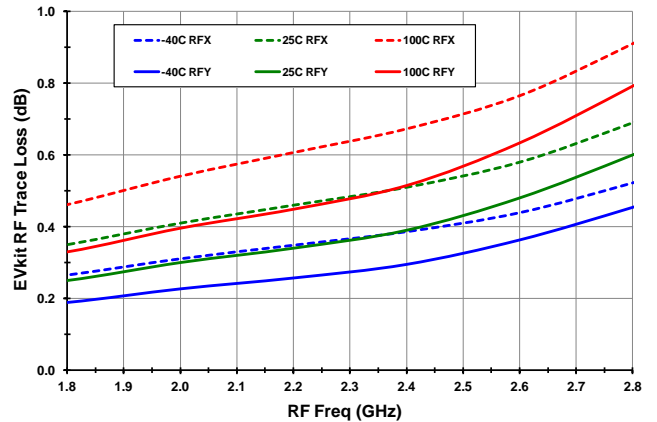
### H2 [LO = 2.92 GHz, HIGH SIDE INJECTION]



### IF TRANSFORMER LOSS

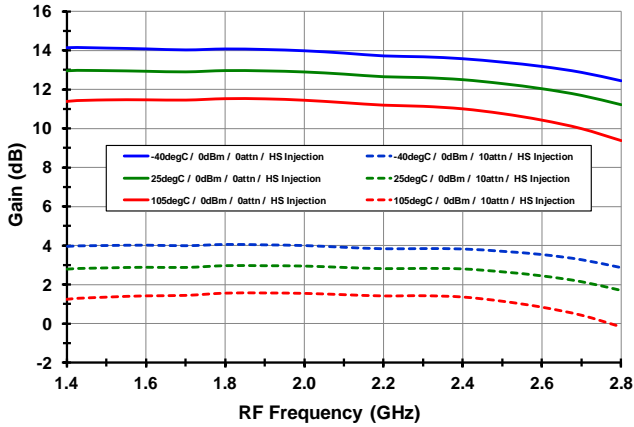


### EVKIT RF TRACE LOSS

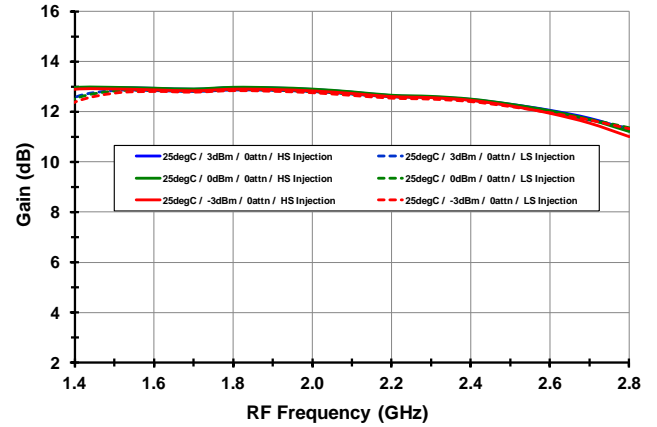


## TOCs F1370 [FIXED IF = 200MHz] (-3-)

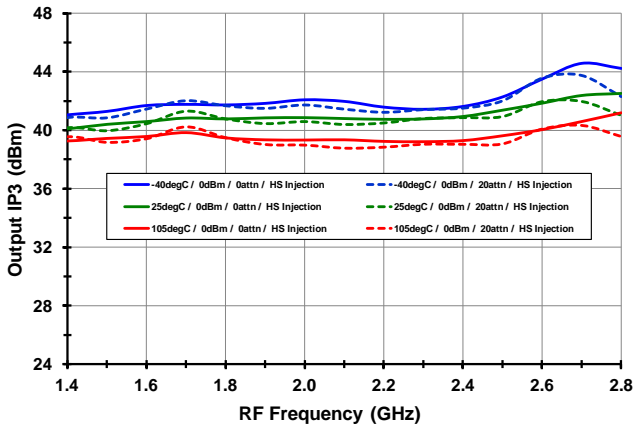
### GAIN [VS. T<sub>CASE</sub>]



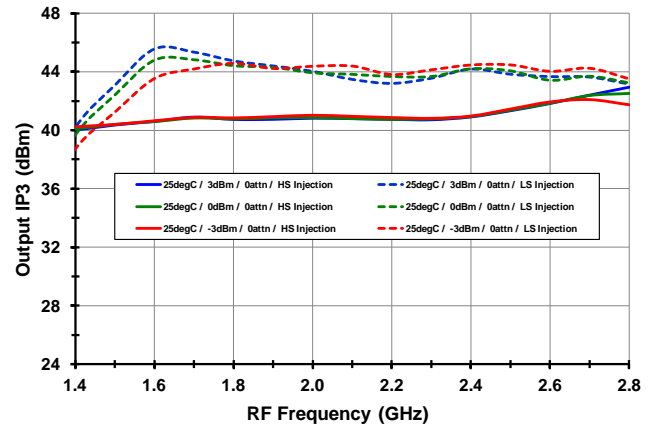
### GAIN [VS. LO LEVEL]



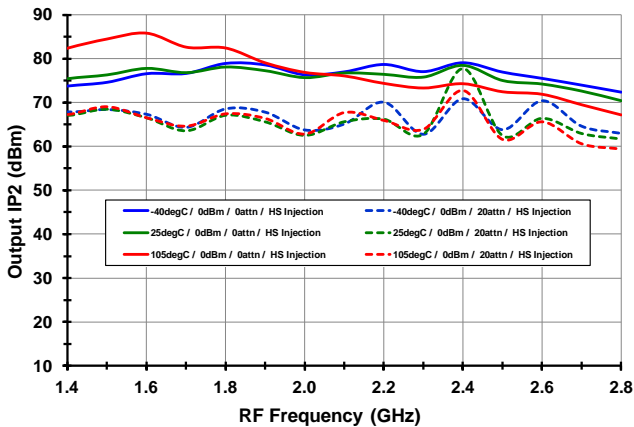
### IP<sub>3O</sub> [VS. T<sub>CASE</sub>]



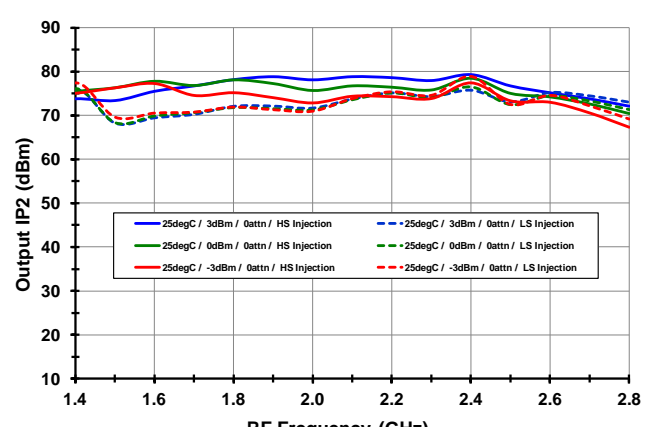
### IP<sub>3O</sub> [VS. LO LEVEL]



### IP<sub>2O</sub> [VS. T<sub>CASE</sub>]

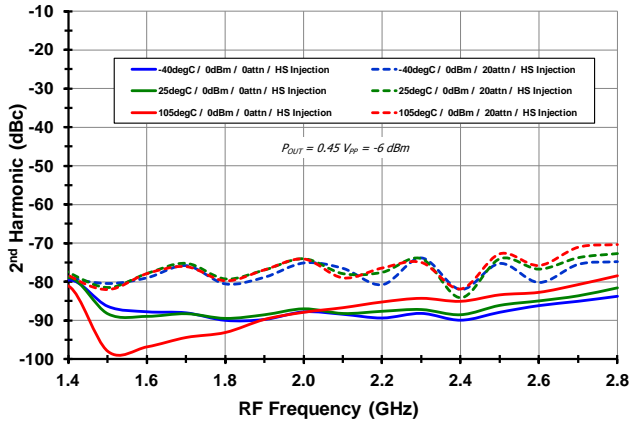


### IP<sub>2O</sub> [VS. LO LEVEL]

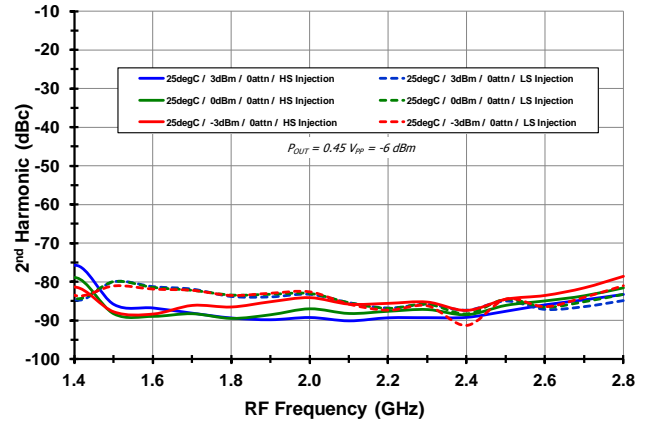


## TOCs F1370 [FIXED IF = 200MHz] (-4-)

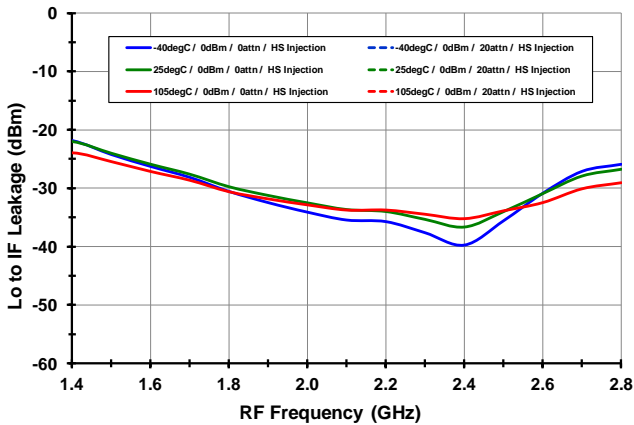
### H2 [vs. TCASE]



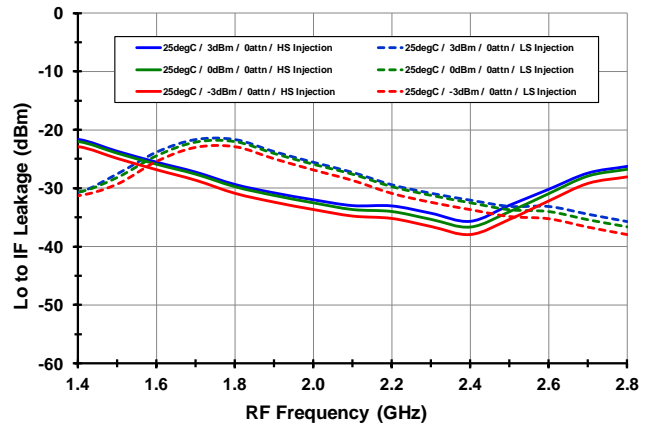
### H2 [vs. LO LEVEL]



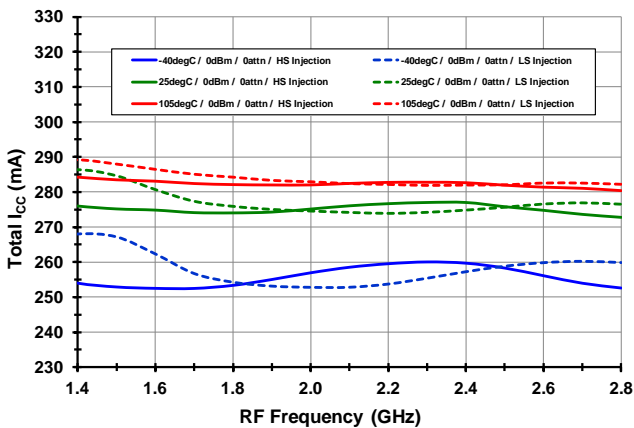
### LO - IF [vs. TCASE]



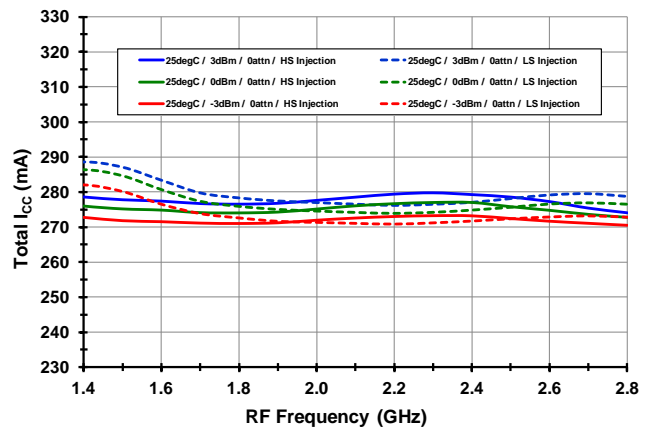
### LO - IF [vs. LO LEVEL]



### I<sub>CC</sub> [vs. TCASE]

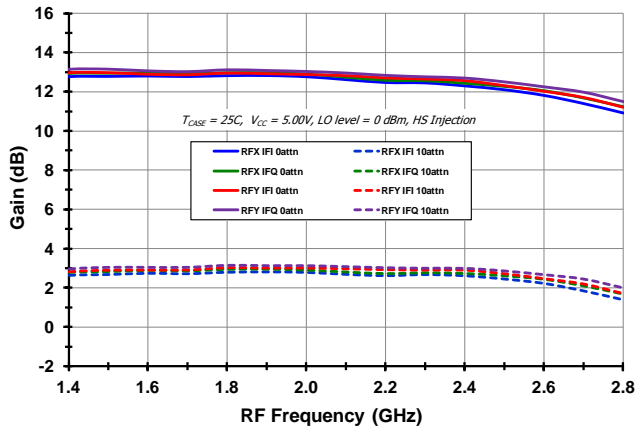


### I<sub>CC</sub> [vs. LO LEVEL]

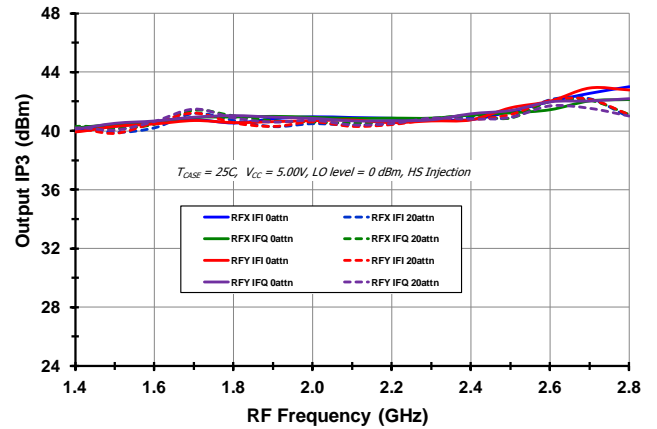


## TOCs F1370 [FIXED IF = 200MHz vs. CONFIGURATION] (-5-)

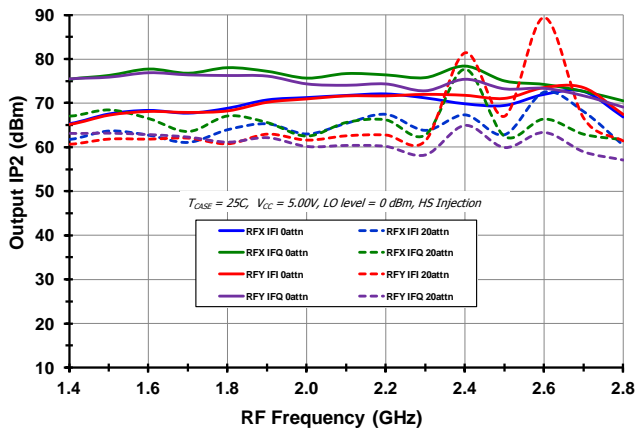
### GAIN



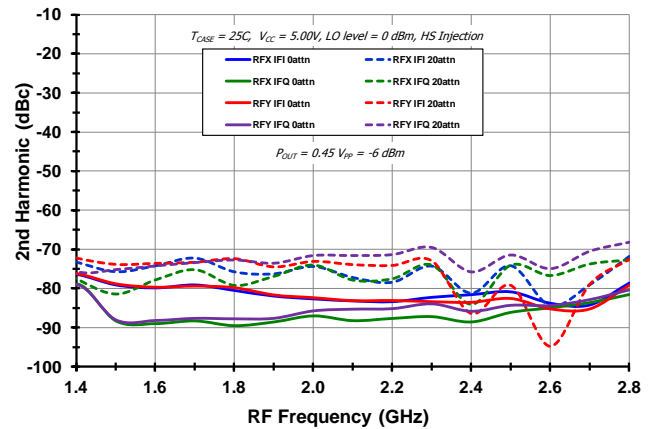
### IP3<sub>o</sub>



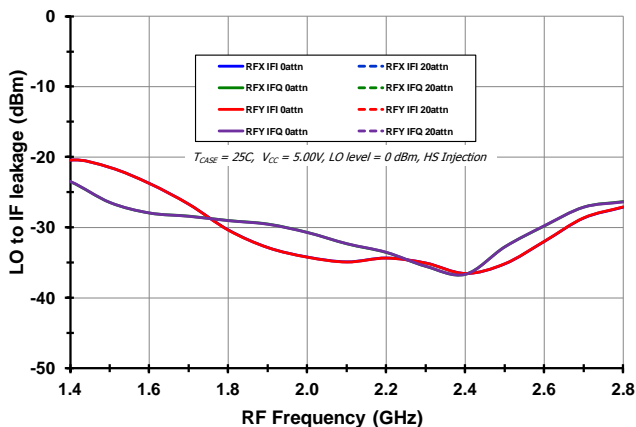
### IP2<sub>o</sub>



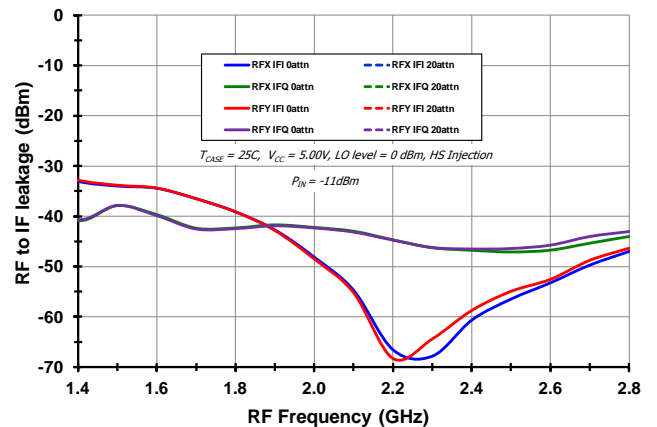
### H2



### LO - IF

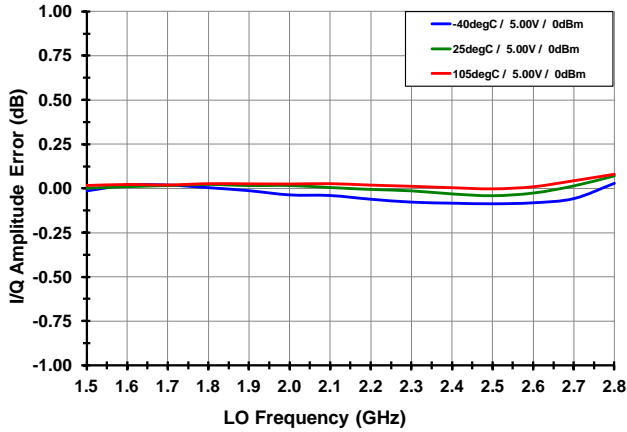


### RF - IF

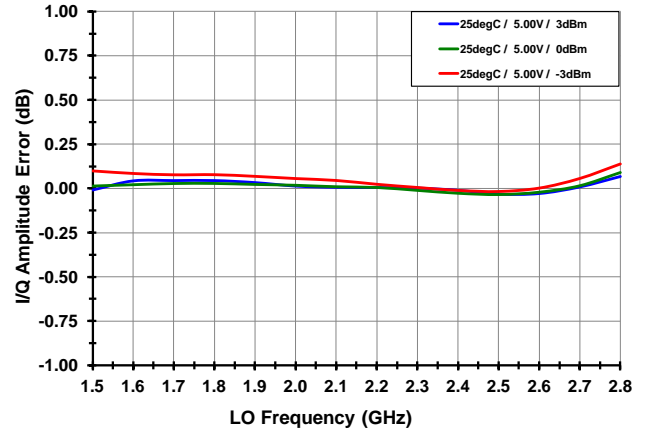


## TOCs F1370 [QUADRATURE, P1dB] (-6-)

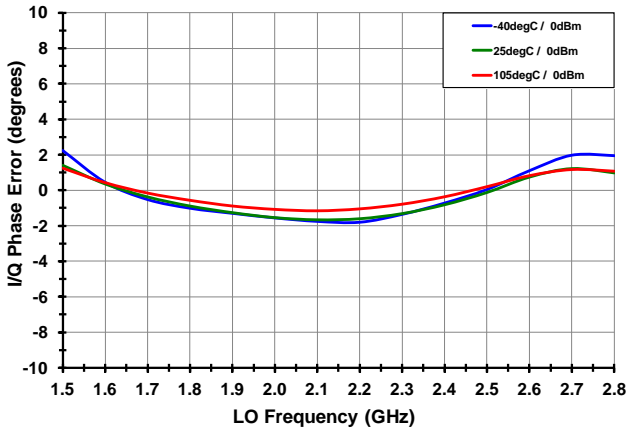
### I/Q AMPLITUDE [vs. TCASE]



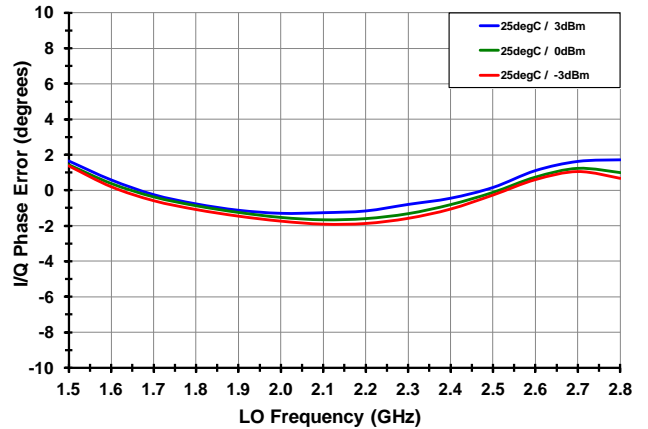
### I/Q AMPLITUDE [vs. LO LEVEL]



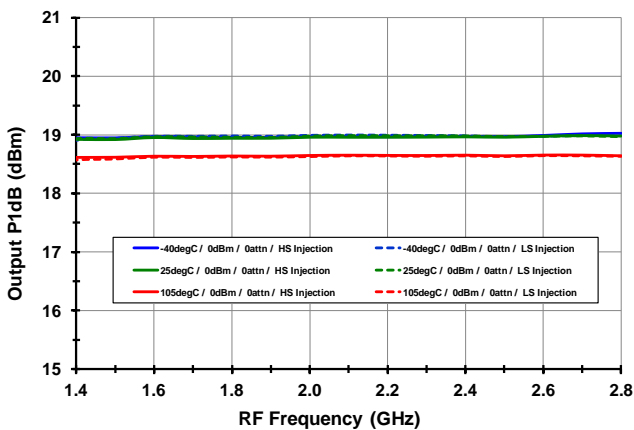
### I/Q PHASE [vs. TCASE]



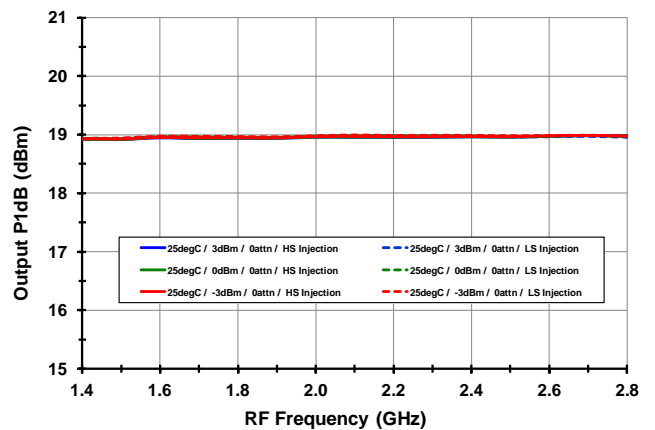
### I/Q PHASE [vs. LO LEVEL]



### OUTPUT P1dB [vs. TCASE]



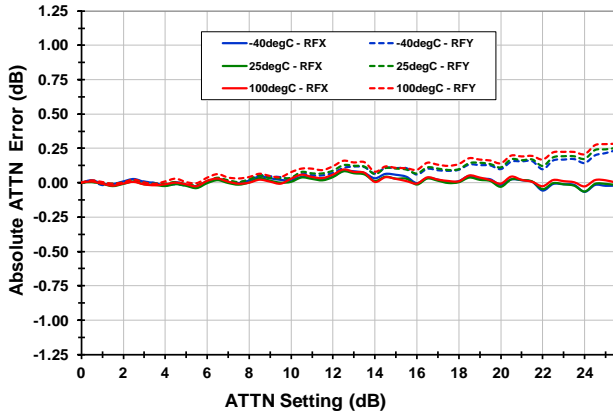
### OUTPUT P1dB [vs. LO LEVEL]



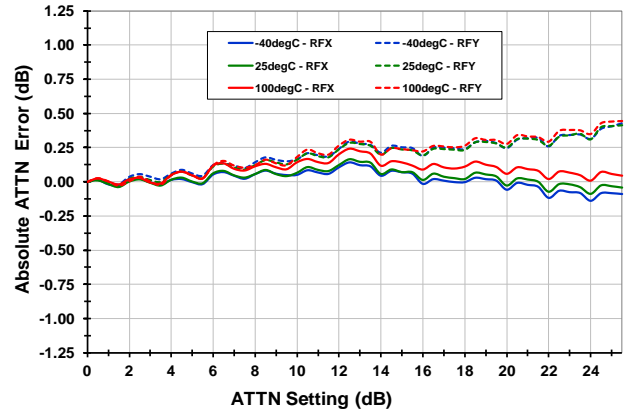


## TOCs F1370 [ATTN ACCURACY, NOISE FIGURE] (-7-)

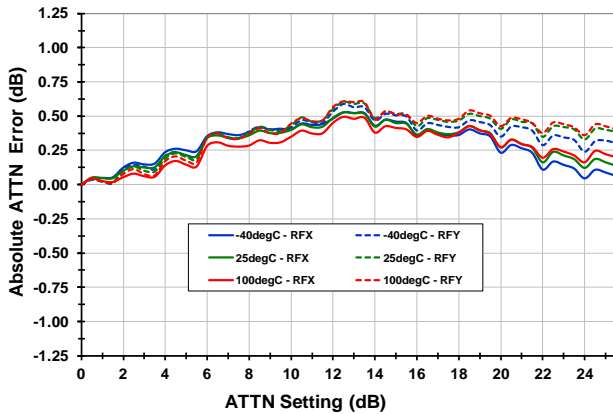
### ATTENUATION ACCURACY [1.7 GHz]



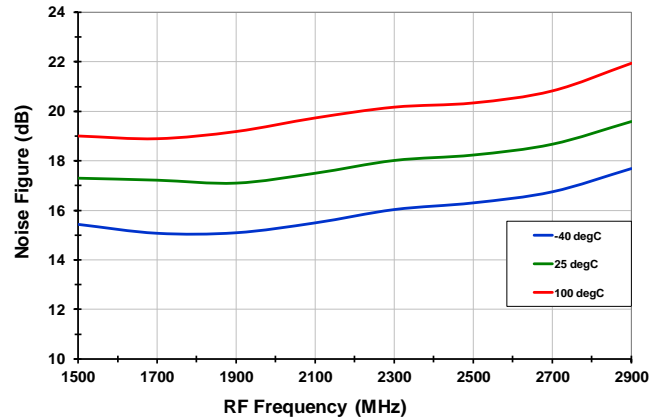
### ATTENUATION ACCURACY [2.1 GHz]



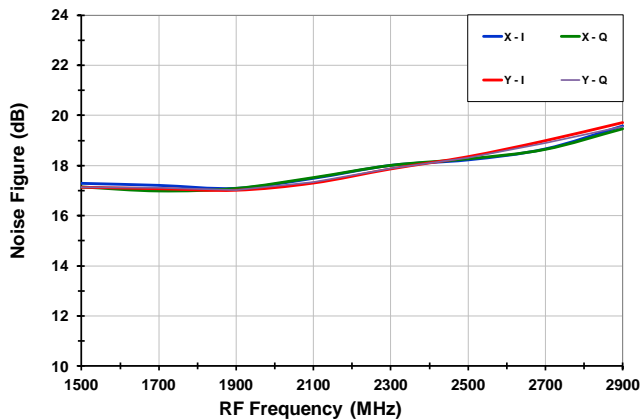
### ATTENUATION ACCURACY [2.7 GHz]



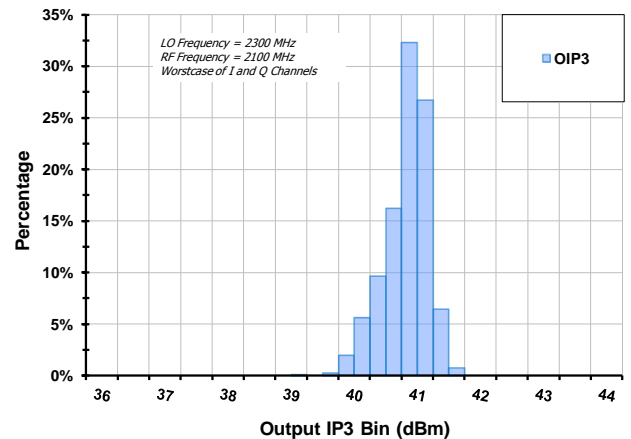
### NOISE FIGURE [VS. T<sub>CASE</sub>, MEASURED RFX TO IFI]



### NOISE FIGURE [25C, VS. CONFIGURATION]

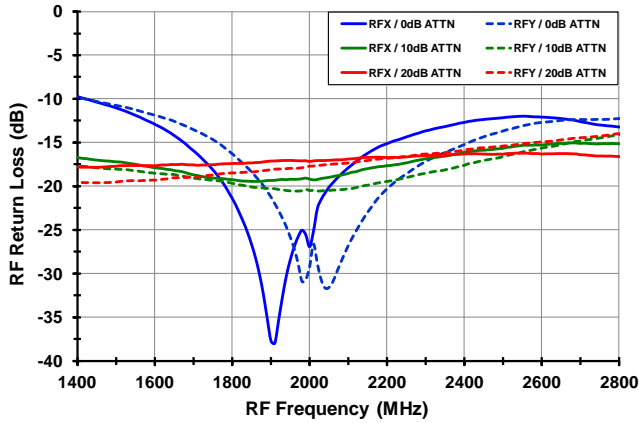


### OIP3 HISTOGRAM [N=820]

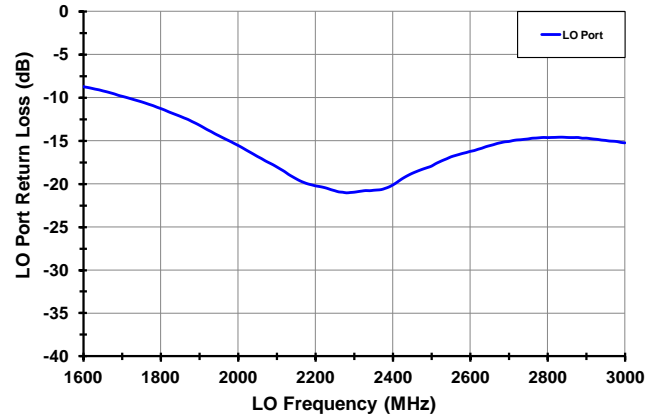


## TOCs F1370 [ISOLATION, RETURN LOSS, HISTOGRAMS] (-8-)

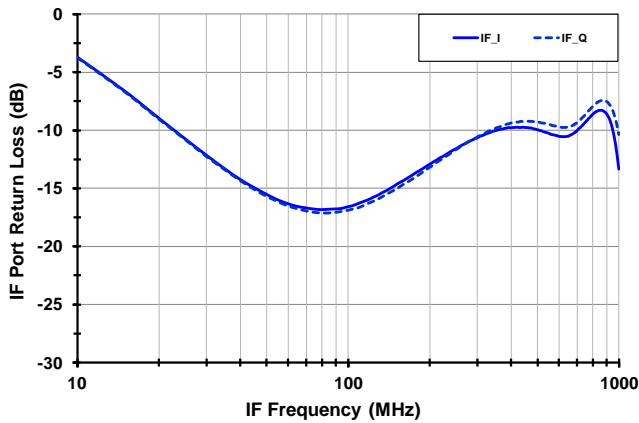
### RF PORT RETURN LOSS



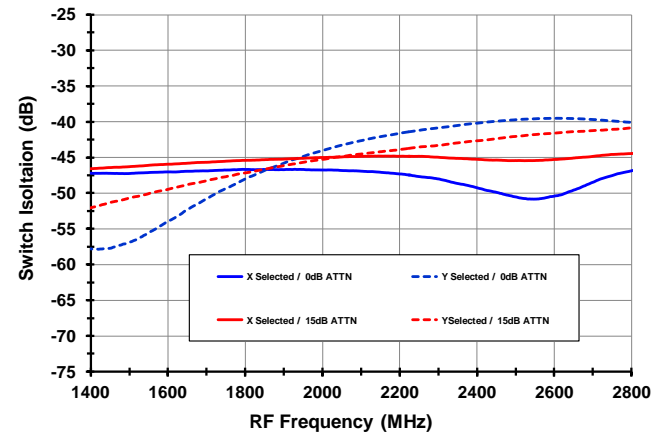
### LO PORT RETURN LOSS



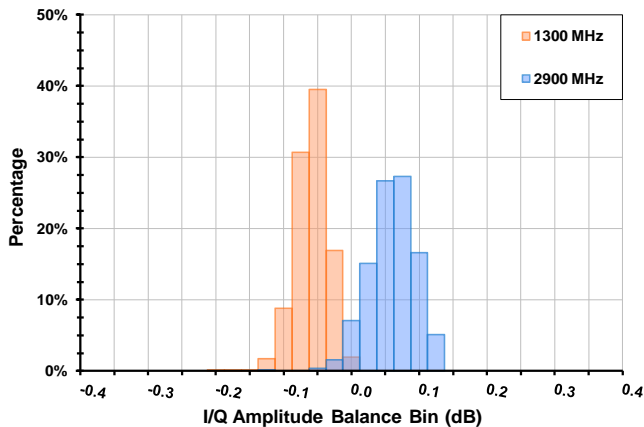
### IF PORT RETURN LOSS



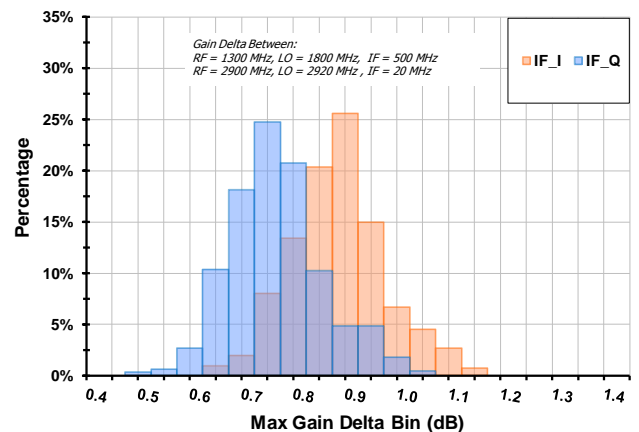
### RF SP2T ISOLATION



### I/Q ERROR HISTOGRAM [N = 820]



### BAND EDGE GAIN DELTA [N = 820]

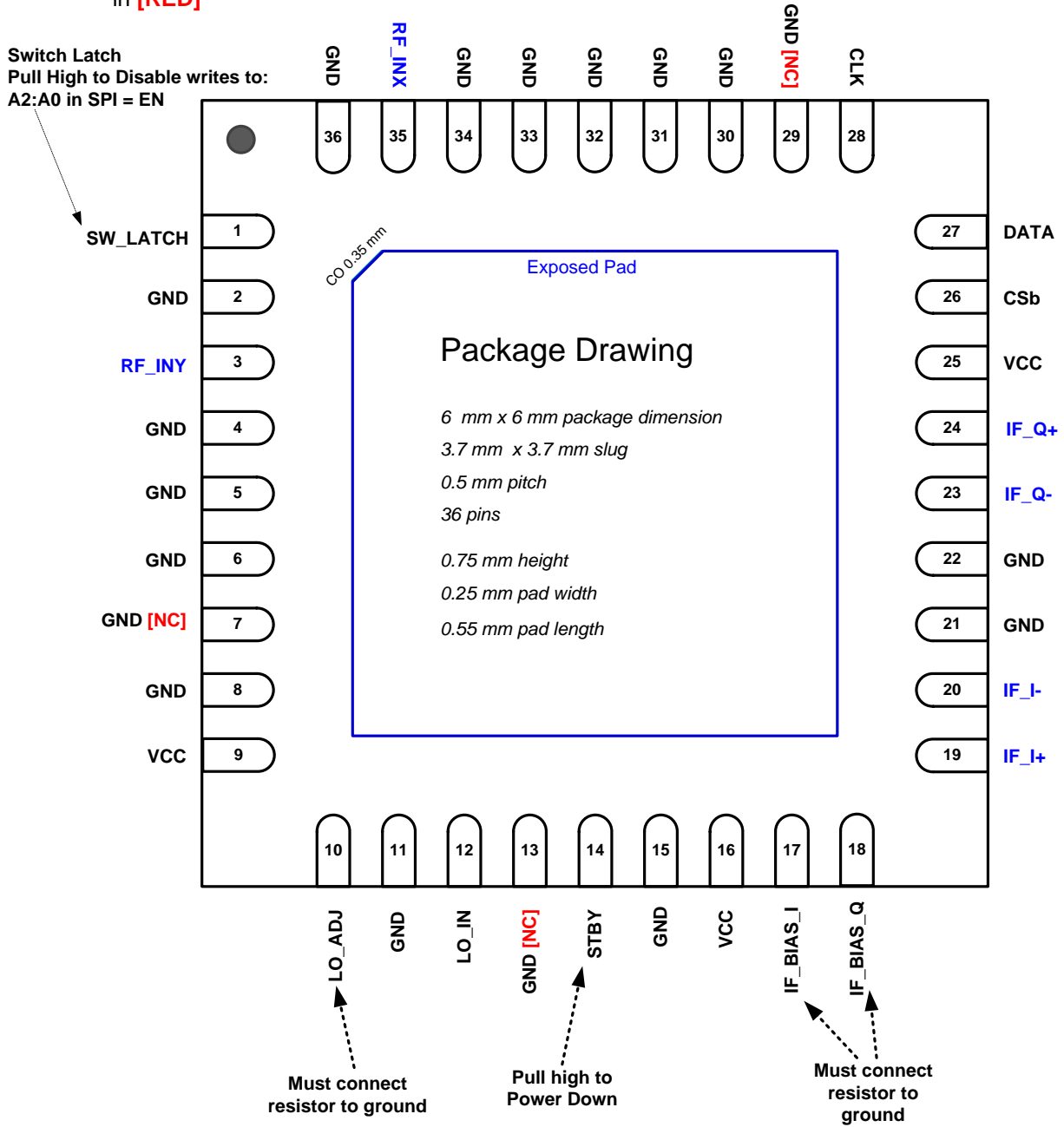




## PIN DIAGRAM

Signal Path Inputs & Outputs in **BLUE**

Internal Connections in **[RED]**



## PIN DESCRIPTIONS

| Pins  | Name                   | Function   |
|---|------------------------|--|
| 1   | SW_LATCH               | Stand-by latch. Pull Low or Ground for Normal Operation. If left floating, this input will be internally pulled high, disabling SPI writes to ENb (Standby) and RF SW bits (A0, A2).   |
| 2, 4, 5, 6, 8, 11, 15, 21, 22, 30, 31, 32, 33, 34, 36 | GND                    | Ground these Pins.   |
| 3   | RF_INY                 | Alternate RF Input. Separated from RF_INX by internal SP2T. AC couple to this pin. Internally matched to 50 ohms   |
| 9, 16, 25   | VCC                    | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.  |
| 10  | LO_ADJ                 | Connect the specified resistor from this pin to ground to set the LO path I <sub>CC</sub> . This IS a current setting resistor   |
| 12  | LO_IN                  | LO Input. AC couple to this pin. Internally matched to 50 ohms   |
| 7, 13, 29   | N.C.                   | No Connection. Not internally connected. OK to connect to V <sub>CC</sub> . Recommended Connection is Ground   |
| 14  | STBY                   | STBY Mode. Pull this pin high for Standby mode (30mA). Pull low or Ground for normal Operation   |
| 17, 18  | IF_BIAS_I<br>IF_BIAS_Q | Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor  |
| 19, 20  | IF_I+, IF_I-           | <i>In-Phase</i> Mixer Differential IF Output. Connect pullup inductors from each of these pins to V <sub>CC</sub> (see the Typical Application Circuit).   |
| 23, 24  | IF_Q-, IF_Q+           | <i>Quadrature</i> Mixer Differential IF Output. Connect pullup inductors from each of these pins to V <sub>CC</sub> (see the Typical Application Circuit).   |
| 26  | CSb                    | Chip Select Bar. The falling edge initiates a programming cycle and the rising edge latches the programmed shift register data into the active register.   |
| 27  | DATA                   | Serial Data Input  |
| 28  | CLK                    | Serial Clock Input   |
| 35  | RF_INX                 | Main RF Input. Separated from RF_INY by internal SP2T. AC couple to this pin. Internally matched to 50 ohms  |
|   | — EP                   | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. |
|   |                        |  |

### CONTROL PIN VOLTAGE & RESISTANCE VALUES

The following table provides open-circuit DC voltage and resistance values referenced to ground for each of the control pins listed.

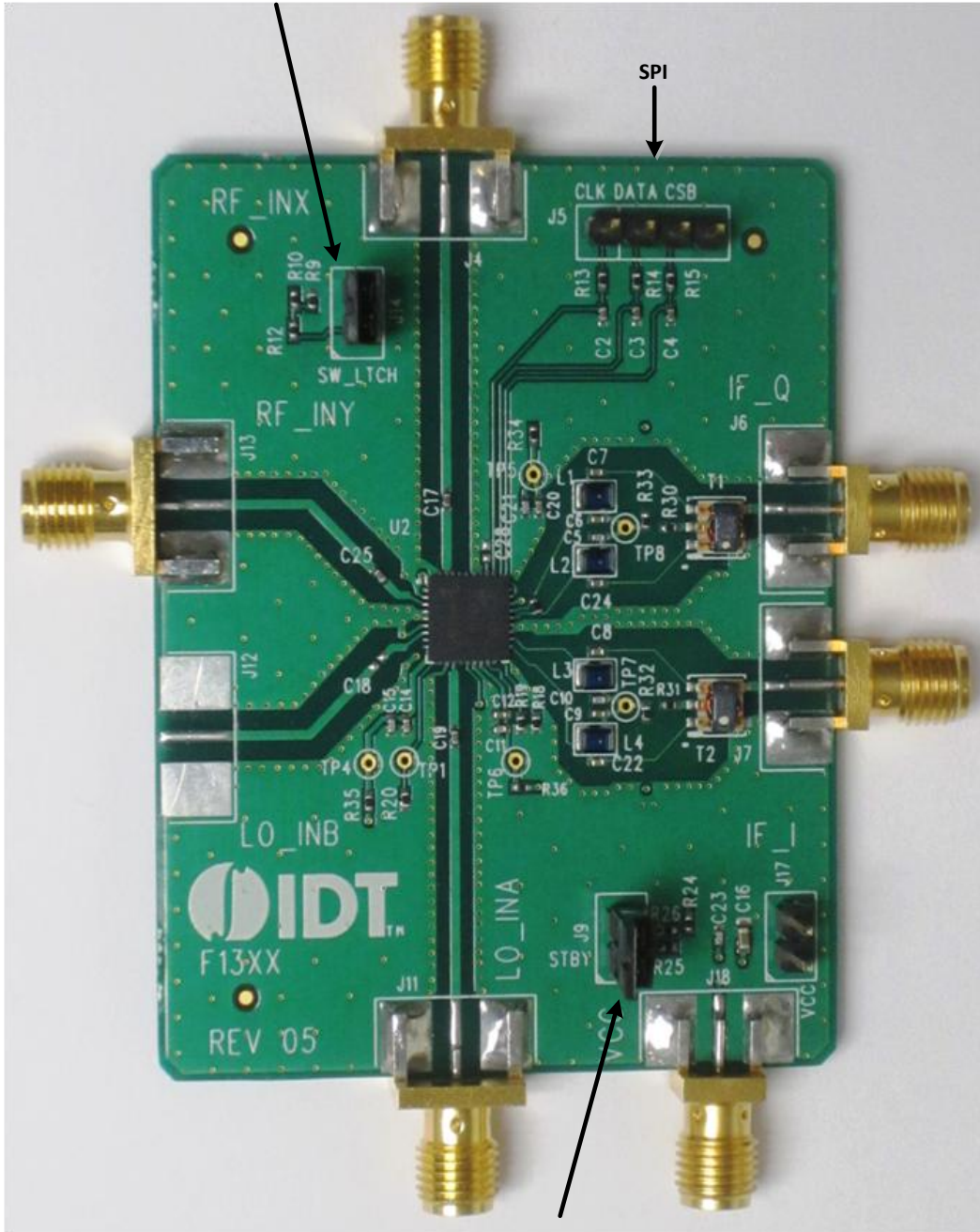
| Pin | Name     | DC voltage (volts) | Resistance (ohms) |
|-----|----------|--------------------|-------------------|
| 1   | SW_LATCH | 1.75               | 1.6M              |
| 14  | STBY     | 5                  | 50k               |
| 26  | CSb      | 1.75               | 1.6M              |
| 27  | DATA     | 1.75               | 1.6M              |
| 28  | CLK      | 1.75               | 1.6M              |

### POWER SUPPLIES

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V/20\mu S$ . In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

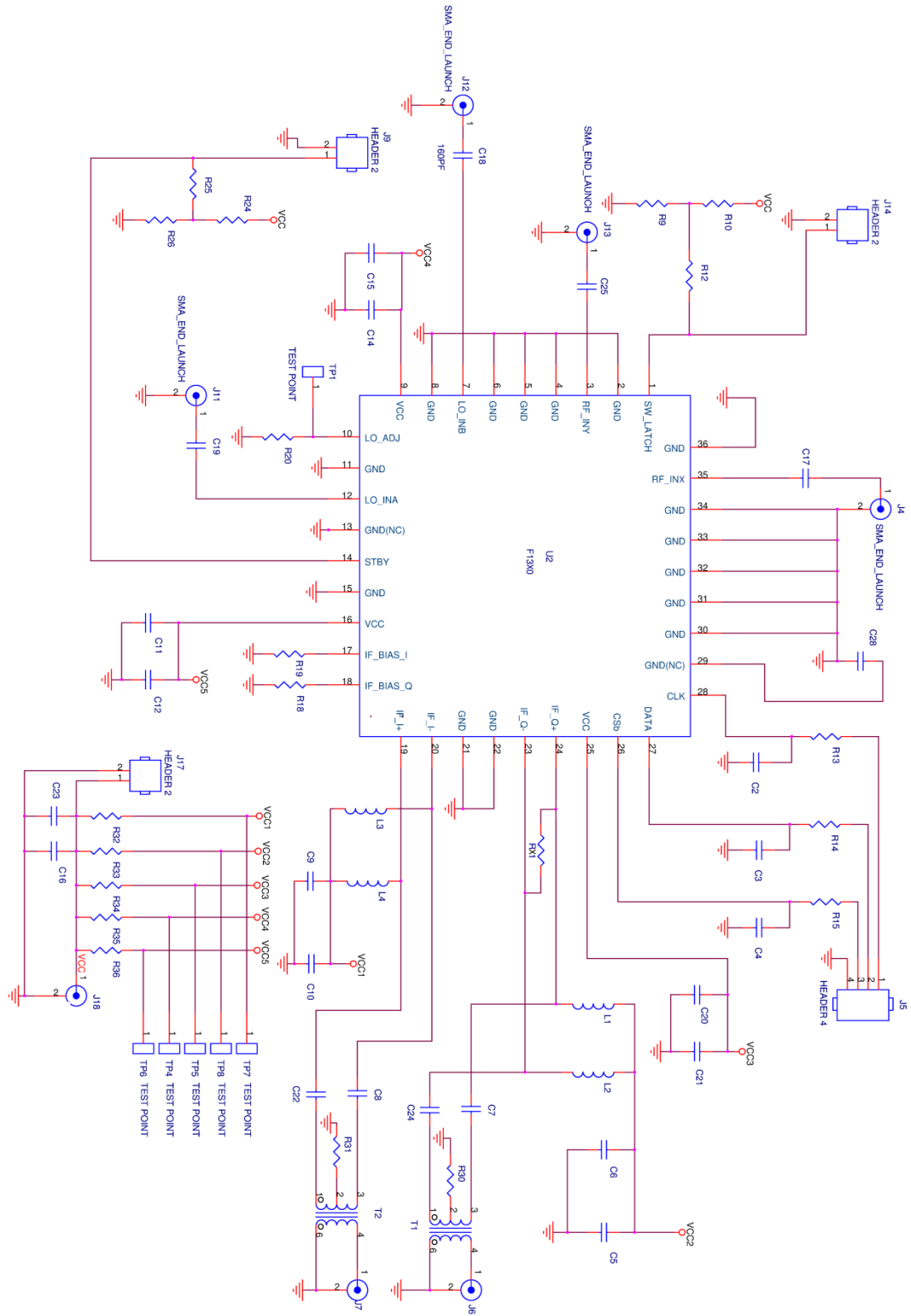
## EVKIT PICTURE / LAYOUT / OPERATION

Close to program  
Open to disable SPI Address Word (A7-A0) writes



Close to turn device ON  
Open to turn device OFF

## EVKIT / APPLICATIONS CIRCUIT





## EVKIT BOM

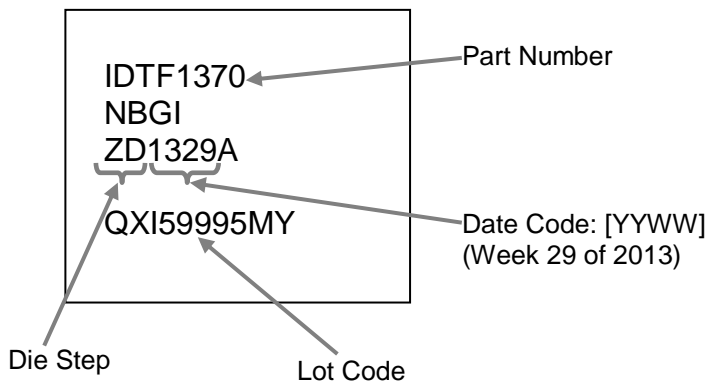
F1370 BOM  
8/27/2013

| Item # | Value          | Size/Rev | Desc                                | Mfr. Part #         | Mfr.            | Supplier Part #  | Supplier      | Part Reference          | Qty |
|--------|----------------|----------|-------------------------------------|---------------------|-----------------|------------------|---------------|-------------------------|-----|
| 1      | 100pF          | 0402     | CAP CER 100PF 50V 5% NP0 0402       | GRM1555C1H101JZ01D  | MURATA          | 490-3458-1-ND    | Digikey       | C2-C4                   | 3   |
| 2      | 10nF           | 0402     | CAP CER 10000PF 16V 10% X7R 0402    | GRM1555R71C103KA01D | MURATA          | 490-1313-1-ND    | Digikey       | C6,7,8,9,12,14,21,22,24 | 9   |
| 3      | 1000pF         | 0402     | CAP CER 1000PF 50V C0G 0402         | GRM1555C1H102JA01D  | MURATA          | 490-3244-1-ND    | Digikey       | C5,10,11,15,20,23       | 6   |
| 4      | 39pF           | 0402     | CAP CER 39PF 50V 5% C0G 0402        | GRM1555C1H390JZ010  | MURATA          | 490-1286-1-ND    | Digikey       | C17,19,25               | 3   |
| 5      | 10uF           | 0603     | CAP CER 10UF 6.3V X5R 0603          | GRM188R60J106ME47D  | MURATA          | 490-3896-1-ND    | Digikey       | C16                     | 1   |
| 6      | Header 2 Pin   | TH 2     | CONN HEADER VERT SGL 2POS GOLD      | 961102-6404-AR      | 3M              | 3M9447-ND        | Digikey       | J9,14,17                | 3   |
| 7      | Header 4 Pin   | TH 4     | CONN HEADER VERT SGL 4POS GOLD      | 961104-6404-AR      | 3M              | 3M9449-ND        | Digikey       | J5                      | 1   |
| 8      | SMA_END_LAUNCH | .062     | SMA_END_LAUNCH (Small)              | 142-0711-821        | Emerson Johnson | 530-142-0711-821 | Mouser        | J6,7,18                 | 3   |
| 9      | SMA_END_LAUNCH | .062     | SMA_END_LAUNCH (Big)                | 142-0701-851        | Emerson Johnson | 530-142-0701-851 | Mouser        | J4,11,13                | 3   |
| 10     | 1uH            | 0805     | 0805LS (2012) Ceramic Chip Inductor | 0805LS-102XJLB      | COILCRAFT       | 0805LS-102XJLB   | COILCRAFT     | L1,2,3,4                | 4   |
| 11     | 43K            | 0402     | RES 43K OHM 1/10W 1% 0402 SMD       | ERJ-2RKF4302X       | Panasonic       | P43.0KLCT-ND     | Digikey       | R10,24                  | 2   |
| 12     | 75K            | 0402     | RES 75K OHM 1/10W 1% 0402 SMD       | ERJ-2RKF7502X       | Panasonic       | P75.0KLCT-ND     | Digikey       | R9,26                   | 2   |
| 13     | 2.37K          | 0402     | RES 2.37K OHM 1/10W 1% 0402 SMD     | ERJ-2RKF2371X       | Panasonic       | P2.37KLCT-ND     | Digikey       | R20                     | 1   |
| 14     | 226            | 0402     | RES 226 OHM 1/10W 1% 0402 SMD       | ERJ-2RKF2260X       | Panasonic       | P226LCT-ND       | Digikey       | R18,19                  | 2   |
| 15     | 47K            | 0402     | RES 47.0K OHM 1/16W 1% 0402 SMD     | RC0402FR-0747KL     | Yageo           | 311-47.0KLRCT-ND | Digikey       | R12,25                  | 2   |
| 16     | 100            | 0402     | RES 100 OHM 1/10W 1% 0402 SMD       | ERJ-2RKF1000X       | Panasonic       | P100LCT-ND       | Digikey       | R13-15                  | 3   |
| 17     | 0              | 0402     | RES 0.0 OHM 1/10W 0402 SMD          | ERJ-2GE0R00X        | Panasonic       | P0.0JCT-ND       | Digikey       | R30,31,32,33,34,35,36   | 7   |
| 18     | 5.11K          | 0402     | RES 5.11K OHM 1/10W 0402 SMD        | ERJ-2RKF5111X       | Panasonic       | P5.11KLCT-ND     | Digikey       | RX1                     | 1   |
| 19     | 1:4 Balun      | SM-22    | 4:1 Center Tap Balun                | TC4-6TG2+           | Mini Circuits   | TC4-6TG2+        | Mini Circuits | T1,2                    | 2   |
| 20     | F1370          | QFN-36   | DPD Demodulator                     | F1370               | IDT             | F1370            | IDT           | U1                      | 1   |
| 21     | PCB            | 05       | Printed Circuit Board               | F13XX REV 05        |                 |                  | SBC           |                         | 1   |
| 22     | BOM            | 03       | Bill Of Material                    |                     |                 |                  |               | Total                   | 60  |

Rev 04:

Add RX1 (5.11K) across IF\_Q+ and IF\_Q- outputs

## TOP MARKINGS



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