6-Channel High Efficiency PMIC for 2-Cell Systems

General Description

The DA6102 is a highly integrated multi-channel PMIC designed for 2-cell lithium-ion battery powered systems. The wide input voltage range allows direct battery connection for each channel to maximize battery life. The PMIC also includes a highly accurate input current sense with circuit breaker control for battery current sensing and over-current shutdown. The DA6102 integrates two buck regulators, a BuckBoost regulator, a high current buck controller, and two always-on LDOs. This high level of integration combined with high frequency operation (up to 3 MHz) minimizes both PCB size and external component count for the smallest possible solution size. The DA6102 uses extremely low RDSon FETs to enable very high efficiency buck and BuckBoost regulation. Additional features include two external load switches, two LDO controllers, external clock synchronization, global enable pin, and configurable PGOOD pin. An I^2C interface enables flexibility and easy configuration of each regulator's output voltage, switching frequency, power sequencing, and fault protection. Most features are configurable by OTP, allowing simplified setting of output voltages and start-up sequence. Each channel has dedicated current limit, over-voltage, and under-voltage protection, with programmable masking and shutdown timer options. The DA6102 is available in a 56-ball 2.975 mm x 3.375 mm, 0.4 mm pitch WLCSP package.

Key Features

- 4.5 V to 11.5 V input range
- Input current sense with circuit breaker
  - +/- 1% accuracy monitoring
- Programmable internal switching frequency
  - 1.0 MHz, 1.5 MHz, 2.0 MHz, and 3.0 MHz
  - +/- 2 % accuracy
- External sync clock input
  - 1.5 MHz to 3 MHz range
- Programmable sequencing and soft-start
- 2 Always-on LDOs with integrated load switches
- 2 Integrated buck converters
- 1 Integrated BuckBoost converter
- 1 High current buck controller
- 2 Load switch controllers
- 2 External LDO monitors
- Power Good flag
- Global enable input
- Smallest total solution size
- 2.975 mm x 3.375 mm WLCSP package
- CH1: BuckBoost regulator
  - 700 mA max
  - 5.1 V to 5.8 V output range
- CH2: Buck regulator
  - 2.2A max
  - 3.0 V to 4.55 V output range
- CH3: Buck controller
  - Synchronous NFET drivers
  - 3.0 V to 3.75 V output range
- CH4: Buck regulator
  - 600 mA max
  - 3.2 V to 4.2 V output range
- LDO1: 300 mA, always-on
- LDO2: 200 mA, always-on
- Protection features on each channel
  - Current limit
  - Short circuit
  - Over-voltage
  - Output discharge

Applications

- DSLR cameras
- MILC cameras

System Diagram

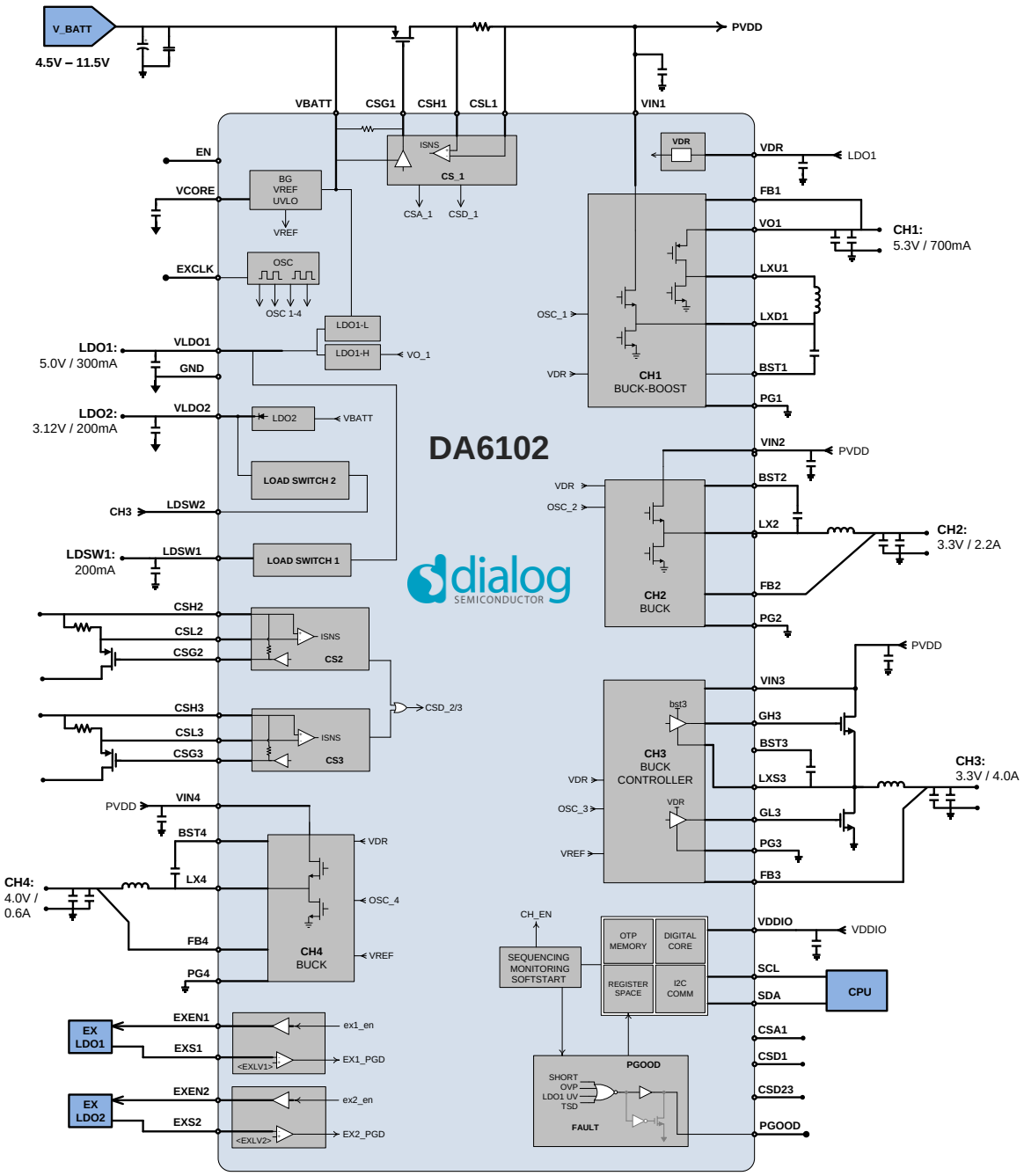


Figure 1: System Diagram

Contents

Figures

Tables

1 Pinout

	1	2	3	4	5	6	7
A	PG4	EXS1	EXEN2	BST2	VIN2	LX2	PG2
B	LX4	EXEN1	FB2	EXS2	VIN2	LX2	PG3
C	VIN4	FB4	CSD23	CSL2	CSH2	LXS3	GL3
D	BST4	VDDIO	GND	EXCLK	CSG2	CSG3	GH3
E	BST1	SDA	VDR	VCORE	CSA1	FB3	VIN3
F	VIN1	SCL	PGOOD	CSD1	CSH3	CSL3	BST3
G	LXD1	EN	FB1	CSG1	CSH1	CSL1	LDSW2
H	PG1	LXU1	VO1	LDSW1	VLDO1	VBATT	VLDO2

COLOR KEY:

CH1 | CH2 | CH3 | CH4 | LDOs | Digital

Current Sense | External LDOs | Load Switches | Supply Rails

Figure 2: Connection Diagram (Top View)

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
Voltage Rails			
H6	VBATT	PS	Supply voltage battery connection and LDO input supply
E3	VDR	PS	Driver voltage input. Connect to VLDO1 and bypass with a 10 µF capacitor
E4	VCORE	PS	1.5 V internal supply voltage, bypass with a 1 µF capacitor
D2	VDDIO	PS	I/O voltage supply
D3	GND	GND	Analog ground connection
System Digital			
G2	EN	DI	Enable input
F2	SCL	DI	I^2C clock input
E2	SDA	DIO	I^2C data I/O
D4	EXCLK	DI	External clock sync input
F3	PGOOD	DO	Power Good flag (open drain or cmos configurable)
LDOs and Load Switches			
H5	VLDO1	AO	LDO1 output
H7	VLDO2	AO	LDO2 output
H4	LDSW1	AO	Load Switch 1 output
G7	LDSW2	AI	Load Switch 2 input
CHANNEL 1			
F1	VIN1	PS	Channel 1, power supply input
E1	BST1	AI	Channel 1 bootstrap connection, connect a 100 nF capacitor from this pin to LXD1
G1	LXD1	AO	Channel 1, buck side switch node
H2	LXU1	AO	Channel 1, boost side switch node
H3	VO1	AO	Channel 1 output voltage
G3	FB1	AI	Channel 1, output voltage sense
H1	PG1	GND	Channel 1 power ground
CHANNEL 2			
A5	VIN2	PS	Channel 2, power supply input
B5	VIN2	PS	Channel 2, power supply input
A4	BST2	AI	Channel 2 bootstrap connection, connect a 100 nF capacitor from this pin to LX2
A6	LX2	AO	Channel 2, switch node
B6	LX2	AO	Channel 2, switch node
B3	FB2	AI	Channel 2, output voltage sense
A7	PG2	GND	Channel 2 power ground

Pin No.	Pin Name	Type (Table 2)	Description
CHANNEL 3			
E7	VIN3	AI	Channel 3, power supply input
F7	BST3	AI	Channel 3 bootstrap connection, connect a 100 nF capacitor from this pin to LXS3
D7	GH3	AO	Channel 3, high side gate drive
C6	LXS3	AI	Channel 3, switch node sense connection
C7	GL3	AO	Channel 3, low side gate drive
E6	FB3	AI	Channel 3, output voltage feedback
B7	PG3	GND	Global power ground, connect to GND plane
CHANNEL 4			
C1	VIN4	PS	Channel 4, power supply input
D1	BST4	AI	Channel 4 bootstrap connection, connect a 100 nF capacitor from this pin to LX4
B1	LX4	AO	Channel 4, switch node
C2	FB4	AI	Channel 4, output voltage feedback
A1	PG4	GND	Channel 4 power ground
CURRENT SENSE 1			
G4	CSG1	AO	Current Sense 1, circuit breaker gate drive
G5	CSH1	AI	Current Sense 1, high side sense
G6	CSL1	AI	Current Sense 1, low side sense
E5	CSA1	AO	Current Sense 1 analog output voltage
F4	CSD1	DO	Current Sense 1, current limit flag
CURRENT SENSE 2 and 3			
D5	CSG2	AO	Current Sense 2, gate drive output
C5	CSH2	AI	Current Sense 2, high side sense
C4	CSL2	AI	Current Sense 2, low side sense
D6	CSG3	AO	Current Sense 3, gate drive output
F5	CSH3	AI	Current Sense 3, high side sense
F6	CSL3	AI	Current Sense 3, low side sense
C3	CSD23	DO	Current Sense 2 and 3, open drain current limit flag
EXTERNAL LDOs			
B2	EXEN1	DO	External LDO1 enable output
A2	EXS1	AI	External LDO1 voltage sense input
A3	EXEN2	DO	External LDO2 enable output
B4	EXS2	AI	External LDO2 voltage sense input

Table 2: Pin Type Definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
GND	Ground	PS	Power Supply Voltage

2 Absolute Maximum Ratings

Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_A	Operating ambient temperature		-40	+85	°C
T_S	Storage temperature		-60	+150	°C
V_{BATT}	Supply battery voltage (VBATT pin)		-0.3	12.0	V
V_{IN}	VINx, LXx, CSL1-2, CSH1-2, CSG1-2		-0.3	VBATT + 0.3	V
V_{BST}	BSTx, GH3		LX_X - 0.3	LX_X + 5.5	V
V_{VO1}	VO1, LXU1, FB1		-0.3	6.5	V
V_{VCORE}	VCORE		-0.3	1.8	V
V_{DDIO}	VDDIO (Note 2)		-0.3	5.5	V
V_{LOGIC}	SDA, SCL, CSD1, CSD23, EXENx		-0.3	VDDIO + 0.3	V
V_{SIGNAL}	FBx, GL3, VDR, EXSx, VLDO1, VLDO2, EN, PGOOD, LDSW1, LDSW2, CSA1, CSL3, CSH3, CSG3, EXCLK		-0.3	5.5	V
GND	PGx		-0.3	+0.3	V
V_{ESD}	ESD susceptibility (Note 3)	HBM (VIN3 – LXS3)	±1.0		kV
		HBM (Others)	±1.5		kV
		CDM	±500		V

Note 1 All voltages are referenced to the GND pin.

Note 2 VDDIO is not allowed to be higher than VBATT.

Note 3 Compliance with ESD-HBM as defined in ANSI/ESDA/JEDEC JS-001-2014. Compliance with ESD-CDM as defined in JEDEC JESD22-C101

3 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BATT}	Battery supply voltage		4.5		11.5	V
V_{DDIO}	I/O supply voltage		1.5		5.0	V
V_{IN1}, V_{IN3}	Channel 1 and 3 supply voltage		4.5		11.5	V
V_{IN2}, V_{IN4}	Channel 2 and 4 supply voltage		5.0		11.5	V

4 Electrical Characteristics

Table 5: DC Characteristics

(Unless otherwise noted, VBATT = 7.4 V, VDDIO = 1.8 V, TA = -40 °C to +85 °C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
System Specifications						
IQ_{STBY}	Standby quiescent current	EN=Low, CS1 disabled (-40°C to 60°C)		6	12	uA
IQ_{STBY}	Standby quiescent current	EN=Low, CS1 disabled (85°C)			20	uA
IQ_{EN}	Non-switching quiescent current	EN=HIGH CH1 to 4 disabled CS1 enabled		695		uA
IQ_{VDDIO}	VDDIO quiescent current			0.14		uA
V_{UVLO_BATT}	VBATT under-voltage lockout	VBATT falling		2.9		V
		VBATT rising		3.8	4.0	V
V_{UVLO_VDR}	VDR under-voltage threshold	VDR falling (VD5 fault) EN=high		3.55	3.60	V
V_{VCORE}	VCORE voltage			1.5		V
F_{OSC}	Switching frequency range		1		3	MHz
F_{OSC_ACC}	Switching frequency accuracy	All frequency settings <EX_OSC> = low	-2		+2	%
F_{EX_OSC}	External sync oscillator frequency range		1.4		3	MHz
D_{EX_OSC}	External sync oscillator duty cycle range		40		60	%
T_{SS}	Soft-start time accuracy	CH1 to 4, all SS settings	-5		+5	%
T_{I2C}	I^2C start-up time	From UVLO release			10	ms
LDOs						
V_{LDO1_L}	LDO1 standby output voltage (LDO1-L)	EN=low 5.0 V < VBATT < 11.5 V	4.7	4.8	4.9	V
V_{LDO1_H}	LDO1 operating output voltage (LDO1-H)	CH1 > 5.3 V	4.9	5.0	5.1	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{TH\_IN\_LDO1}$	LDO1 input switch threshold	VO1 rising			5.1	V
		VO1 falling		5.0		V
$V_{DO\_1\_L}$	LDO1_L dropout voltage	VBATT = 4.8 V, 25 mA		0.13		V
$V_{DO\_1\_H}$	LDO1_H dropout voltage	CH1 = 5.1 V, 100 mA		0.11		V
ΔV_{LDO1_L}	LDO1_L load regulation	VBATT = 7.4 V 0 mA to 25 mA		0.024		%/mA
ΔV_{LDO1_H}	LDO1_H load regulation	CH1 = 5.3 V 0 mA to100 mA		4.4		%/A
I_{LDO1_H}	LDO1_H current limit	CH1 > 5.2 V	300	510		mA
I_{LDO1_L}	LDO1_L current limit	CH1 < 5.2 V	70	110		mA
V_{LDO2}	LDO2 output voltage range		3.12		3.27	V
V_{VLDO2}	LDO2 output voltage accuracy	Default value = 3.12 V 3.3 V < VBATT (or LDSW2) <11.5 V	-2		+2	%
ΔV_{LDO2}	LDO2 load regulation	0 A to 100 mA		11		%/A
I_{LDO2}	LDO2 current limit		200	270		mA
Current Sense, Load Switches, and Circuit Breaker						
VCM_{CS_1}	CSH1 and CSL1 input voltage range	Common mode			11.5	V
VDM_{CS_1}	CSH1 and CSL1 input voltage range	Differential mode			150	mV
A_{CS1_2}	Current sense 1 amplifier gain	setting 1		20		V/V
A_{CS1_3}	Current sense 1 amplifier gain	setting 2		40		V/V
A_{CS1_4}	Current sense 1 amplifier gain	setting 3		100		V/V
V_{CSA1}	CSA1, current sense output accuracy	CSA1 > 2.0 V setting 1, 2	-1		+1	%
V_{CSA1_3}	CSA1, current sense output accuracy	CSA1 > 2.0 V setting 3	-2.5		+2.5	%
V_{CSA1}	CSA1, current sense output accuracy	CSA1 < 2.0 V setting 1, 2	-20		+20	mV
V_{CSA1_3}	CSA1, current sense output accuracy	CSA1 < 2.0 V setting 3	-50		+50	mV
V_{CSG1}	CSG1 PGATE drive voltage	CSG1 gate drive low referenced to VBATT		–4.5	-4.0	V
R_{ON_CS1}	CSG1 sink resistance	CSG1 gate drive low		0.7	1	kΩ
R_{CSG1}	CSG1 pull-up resistance	CSG1 gate drive high		0.7		MΩ
V_{OC_CS1}	Current Sense 1 Over-Current threshold	CSH1-CSL1 register programmable	-2		+2	%
T_{S_CS1}	Current Sense 1 settling time	At CSA1		5		us

Parameter	Description	Conditions	Min	Typ	Max	Unit
A_{CS2_1}	Current Sense 2 Amplifier gain	setting 1		20		V/V
A_{CS2_2}	Current Sense 2 Amplifier gain	setting 2		40		V/V
V_{CSG2}	Current Sense 2 PGATE drive voltage	CSG2 gate drive low referenced to CSL2		-4.5	-4.0	V
R_{ON_CS2}	CSG2 sink resistance	CSG2 gate drive low		0.7	1	kΩ
R_{CSG2}	CSG2 pull-up resistance	CSG2 gate drive high		700		kΩ
V_{OC_CS2}	Current Sense 2 Over-Current threshold	CSH2-CSL2, register programmable	-2		+2	%
A_{CS3_1}	Current sense 3 Amplifier gain	setting 1		20		V/V
A_{CS3_2}	Current sense 3 Amplifier gain	setting 2		40		V/V
V_{CSG3}	Current Sense 3 PGATE drive voltage	CSG3 gate drive low referenced to CSL3	0		0.3	V
R_{ON_CS3}	CSG3 sink resistance	CSG3 gate drive low		0.5	1	kΩ
R_{CSG3}	CSG3 pull-up resistance	CSG3 gate drive high		700		kΩ
V_{OC_CS3}	Current Sense 3 Over-Current threshold	CSH3-CSL3, register programmable	-2		+2	%
R_{ON_LDSW1}	Load switch 1 Rds_on	LDSW1F (0x22) = 0 LDO1 > 4.5 V		0.55	0.85	Ω
$R_{ON\_LDSW1\_F}$	Load switch 1 Rds_on Force-On mode	LDSW1F (0x22) = 1		0.10	0.23	Ω
V_{LIM_LDSW1}	Load switch 1 input limit voltage	Falling voltage at LDO1_H increases LDSW1 Rds_on	4.4	4.5		V
T_{SS_LDSW1}	Load switch 1 soft-start period	I_{SS_LDSW1} current limited		1		ms
I_{SS_LDSW1}	Load switch 1 soft-start current limit		45	70	150	mA
R_{DIS_LDSW1}	Load switch 1 discharge resistance	EN5 = low DISC5 (0x18) = 0	70	100	130	Ω
R_{ON_LDSW2}	Load switch 2 Rds_on				0.24	Ω
I_{LIM_LDSW2}	Load switch 2 start-up limit			50	100	mA
T_{SS_LDSW2}	Load switch 2 start-up time			1		ms
Channel 1						
V_{CH1}	Channel 1 output voltage range	Register programmable in 50 mV steps	5.1		5.8	V
V_{VO1}	Channel 1 output voltage accuracy	Default setting = 5.3 V 5.0 V < VIN1 < 11.5 V	-2.5		+2.5	%
ΔV_{VO1_LOAD}	Channel 1 load regulation	Default setting 0 A to 400 mA		0.1		%/A
I_{LIM_1}	Channel 1 current limit threshold	Peak inductor current	2.0	2.6		A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$T_{OFF\_MIN\_A1}$	Channel 1 buck minimum off time	At LXD1 (LXU1 boost turn-on threshold)		83		ns
$T_{ON\_MIN\_A1}$	Channel 1 buck minimum on time	At LXD1		100		ns
$R_{DS\_ON\_A1H}$	Channel 1 buck high side on resistance			154		mΩ
$R_{DS\_ON\_A1L}$	Channel 1 buck low side on resistance			183		mΩ
$R_{DS\_ON\_B1H}$	Channel 1 boost high side on resistance			121		mΩ
$R_{DS\_ON\_B1L}$	Channel 1 boost low side on resistance			147		mΩ
R_{DISC1}	Channel 1 output discharge resistance	EN=low, NDISC1 (0x18)=0	70	100	130	Ω
Channel 2						
V_{CH2}	Channel 2 output voltage range	Register programmable in 50 mV steps	3.00		4.55	V
V_{VO2}	Channel 2 output voltage accuracy	Default setting: 3.3 V 5.0 V < VIN1 < 11.5 V	-2.5		+2.5	%
ΔV_{VO2_LOAD}	Channel 2 load regulation	Default setting: 0 A to 2.2 A		0.02		%/A
I_{LIM_2}	Channel 2 current limit threshold	Peak inductor current	3.6	5.0		A
$T_{OFF\_MIN\_2}$	Channel 2 minimum off time	At LX2		83		ns
$T_{ON\_MIN\_2}$	Channel 2 minimum on time	At LX2		100		ns
$R_{DS\_ON\_2H}$	Channel 2 high side on resistance			107		mΩ
$R_{DS\_ON\_2L}$	Channel 2 low side on resistance			123		mΩ
R_{DISC2}	Channel 2 output discharge resistance	EN=low NDISC2 (0x18)=0	70	100	130	Ω
Channel 3						
V_{CH3}	Channel 3 output voltage range	Register programmable in 50 mV steps	3.00		3.75	V
V_{VO3}	Channel 3 output voltage accuracy	Default setting: 3.3 V 4.5 V < VIN1 < 11.5 V	-2.5		+2.5	%
ΔV_{VO3_LOAD}	Channel 3 load regulation	Default setting: 0 A to 4 A		0.02		%/A
$V_{ILIM\_3\_0}$	Channel 3 current limit threshold voltage	EXTFET (0x21) = 0 VIN3-LXS3	240	270	300	mV
$V_{ILIM\_3\_1}$	Channel 3 current limit threshold voltage	EXTFET (0x21) = 1 VIN3-LXS3	120	135	150	mV
$T_{OFF\_MIN\_3}$	Channel 3 minimum off time	At GH3		83		ns
$T_{ON\_MIN\_3}$	Channel 3 minimum on time	At GH3		100		ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{SO3_H}	Channel 3 high side driver source resistance			1.1		Ω
R_{SK3_H}	Channel 3 high side driver sink resistance			0.9		Ω
R_{SO3_L}	Channel 3 low side driver source resistance			1.1		Ω
R_{SK3_L}	Channel 3 low side driver sink resistance			0.9		Ω
R_{DISC3}	Channel 3 output discharge resistance	EN=low, NDISC3 (0x18)=0	70	100	130	Ω
Channel 4						
V_{CH4}	Channel 4 output voltage range	Register programmable in 50 mV steps	3.20		4.20	V
V_{VO4}	Channel 4 output voltage accuracy	Default setting: 4.0 V 5.0 V < VIN1 < 11.5 V	-2.5		+2.5	%
ΔV_{VO4_LOAD}	Channel 4 load regulation	Default setting: 0 A to 0.6 A		0.08		%/A
I_{LIM_4}	Channel 4 current limit threshold	Peak inductor current	2.0	2.6		A
$T_{OFF\_MIN\_4}$	Channel 4 minimum off time	At LX4		83		ns
$T_{ON\_MIN\_4}$	Channel 4 minimum on time	At LX4		100		ns
$R_{DS\_ON\_4H}$	Channel 4 high side on resistance			342		mΩ
$R_{DS\_ON\_4L}$	Channel 4 low side on resistance			342		mΩ
R_{DISC4}	Channel 4 output discharge resistance	EN=low NDISC4 (0x18)=0	70	100	130	Ω
Fault Detection						
V_{PGOOD_H}	Power good rising threshold	CH1 to 4 VOx rising		90		%
V_{PGOOD_L}	Power good falling threshold	CH1 to 4 VOx falling		85		%
SCP	Short Circuit Protection threshold	CH1 to 4 and LDSW1, falling		70		%
OVP	Over-Voltage Protection threshold	CH2 to 4 VOx rising		120		%
OVP_1	CH1 Over-Voltage Protection threshold	VO1 rising		110		%
V_{PGOOD_EX}	EXS1-2 power good accuracy			TBD		+/-mV
V_{PGOOD_EXL}	EXS1-2 power good hysteresis	PG7 and PG8 status low		-100		mV
TSD	Thermal Shut Down threshold			150		°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
Digital						
V_{IH}	Input High Voltage	EXCLK, EN	1.2			V
V_{IL}	Input Low Voltage	EXCLK, EN			0.3	V
V_{IH_I2C}	Input High Voltage	SCL, SDA	VDDIO x 0.7			V
V_{IL_I2C}	Input Low Voltage	SCL, SDA			0.3 x VDDIO	V
V_{OH}	Output High Voltage	CSD1, EXEN1-2, PGOOD (cmos mode) 1 mA source	VDDIO x 0.7			V
V_{OL}	Output Low Voltage	CSD1, EXEN1-2 PGOOD (cmos mode) 1 mA sink			0.3 x VDDIO	V
V_{OL}	Output Low Voltage	SDA at < 3 mA sink current			0.4	V
R_{PGOOD}	Power Good pulldown resistance	Open drain mode			100	Ω

Table 6: AC Characteristics

External components are as shown in Figure 25, VBATT = 7.4 V, TA = 25 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
VTR_{LO_1A}	CH1 load transient response	Io=0 A to 400 mA 50 mA/µs Fsw = 2MHz			85	+/-mV
VTR_{LO_1B}	CH1 load transient response	Io= 0 A to 300 mA 1 mA/µs Fsw = 2 MHz			85	+/-mV
VTR_{LI_1}	CH1 line transient response	VBATT = 5.5 V to 10.5 V 0.1 V/µs Fsw = 2 MHz Io = 200 mA			150	+/-mV
VTR_{LO_2A}	CH2 load transient response	Io = 0 A to 2.2 A 250 mA/µs Fsw = 2 MHz			400	+/-mV
VTR_{LO_2B}	CH2 60% load transient response	Io = 0 A to 1.3 A 4 mA/µs Fsw = 2 MHz			80	+/-mV
VTR_{LI_2}	CH2 line transient response	VBATT = 5.5 V to 10.5 V 0.1 V/µs Fsw = 2 MHz Io = 1 A			150	+/-mV
VTR_{LO_3A}	CH3 load transient response	Io = 0 A to 1 A 55 mA/µs Fsw = 1 MHz			90	+/-mV
VTR_{LO_3B}	CH3 60% load transient response	Io = 0 A to 660 mA 55 mA/µs Fsw = 1 MHz			80	+/-mV
VTR_{LI_3}	CH3 line transient response	VBATT = 5.5 V to 10.5 V 0.1 V/µs Fsw = 1 MHz Io = 1 A			70	+/-mV
VTR_{LO_4A}	CH4 load transient response	Io =0 A to 600 mA 50 mA/µs Fsw = 2 MHz			150	+/-mV
VTR_{LO_4B}	CH4 60% load transient response	Io = 100 mA to 450 mA 50 mA/µs Fsw = 2 MHz			85	+/-mV
VTR_{LI_4}	CH4 line transient response	VBATT = 5.5 V to 10.5 V 0.1 V/µs Fsw = 2 MHz Io = 300 mA			100	+/-mV

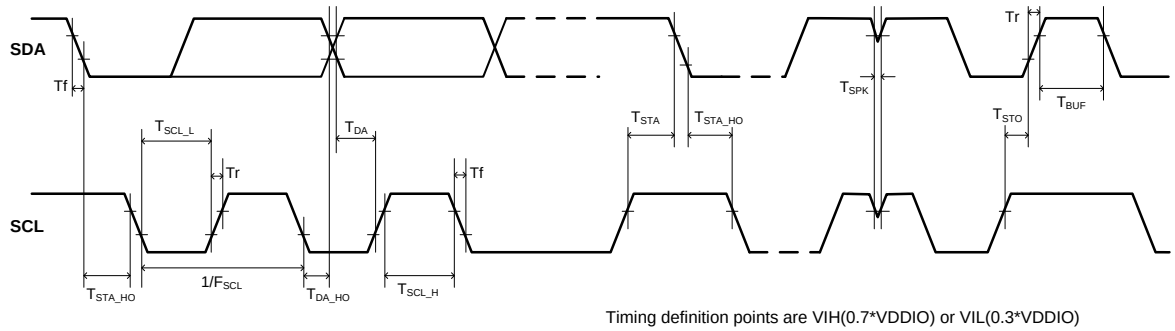


Figure 3: I²C Timing

5 Timing Characteristics

Table 7: I²C Timing Characteristics

(VBATT = 7.4 V, VDDIO = 1.8 V, TA = -40 °C to +85 °C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{BUS}	Bus line capacitive load				400	pF
T_{SPK}	Spike suppression	SDA and SCL input filters suppress spikes < 50 ns			50	ns
F_{SCL}	SCL frequency				400	kHz
T_{STA}	Start condition set-up time		0.6			µs
T_{STA_HO}	Start condition hold time		0.6			µs
T_{STO}	Stop condition set-up time		0.6			µs
T_{BUF}	Bus free time	Between STOP and START	1.3			µs
T_{SCL_L}	SCL clock low time		0.6			µs
T_{SCL_H}	SCL clock high time		0.6			µs
T_r	SCL, SDA rise time	(input requirement)			300	ns
T_f	SCL, SDA fall time	(input requirement)			300	ns
T_{DA}	Data set-up time		100			ns
T_{DA_HO}	Data hold-time		0			ns

6 Thermal Characteristics

Table 8: Thermal Characteristics

Parameter	Description	Conditions (Note 1)	Typ	Unit
θ_{JA_J}	Junction to ambient thermal resistance	JEDEC standard, 2s4p	30	°C/W
θ_{JA_E}	Junction to ambient thermal resistance	Evaluation board, 6-layer	34	°C/W
θ_{JB}	Junction to board thermal resistance	1 mm from IC edge, evaluation board	9.5	°C/W

Note 1 Based on simulation with no air flow and 2.0 W power dissipation.

7 Typical Performance

Unless otherwise noted, VBATT = 7.4 V, TA = 25 °C, external components as shown in Figure 25.

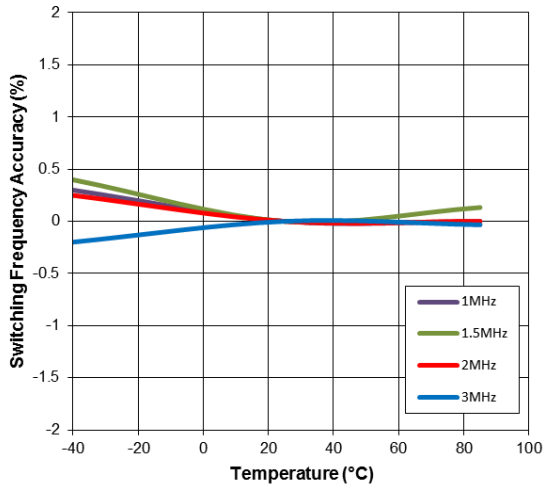


Figure 4: Frequency vs Temperature

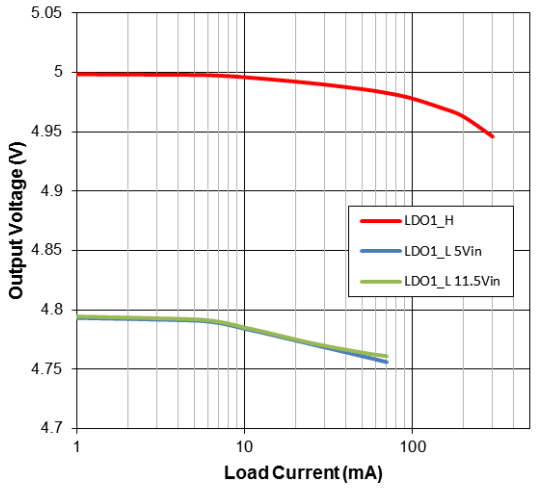


Figure 6: LDO1 Load Regulation

(LDO1 input is Vo1: 5.3 V)

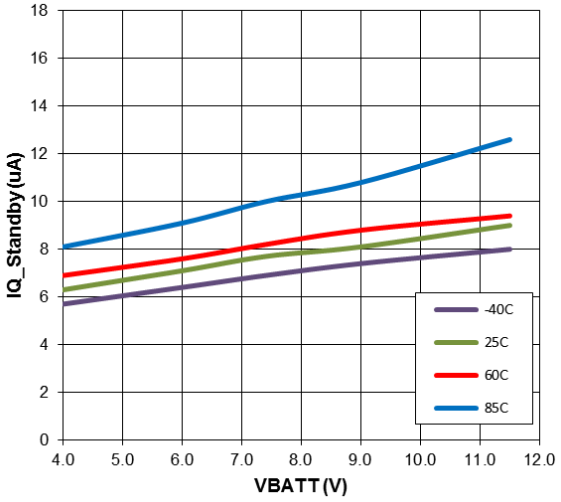


Figure 5: IQ_Standby vs VBATT

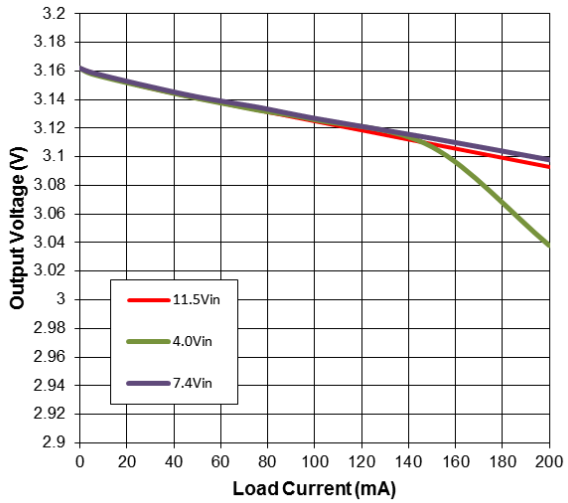


Figure 7: LDO2 Load Regulation

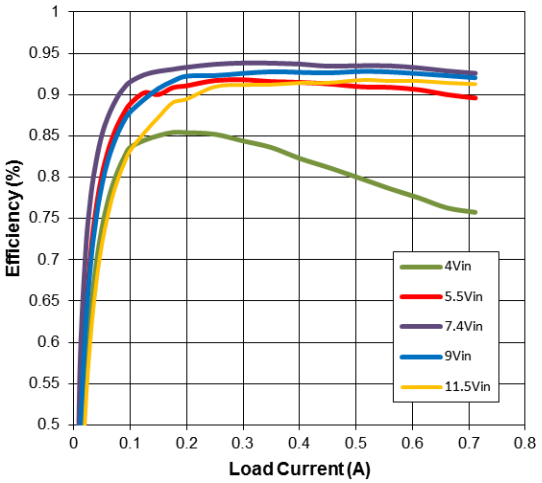


Figure 8: Ch 1 Efficiency (Vout = 5.3 V)

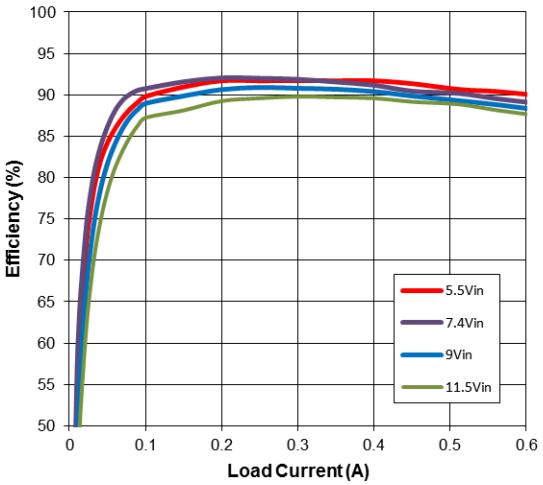


Figure 11: Ch 4 Efficiency (Vout = 4.0 V)

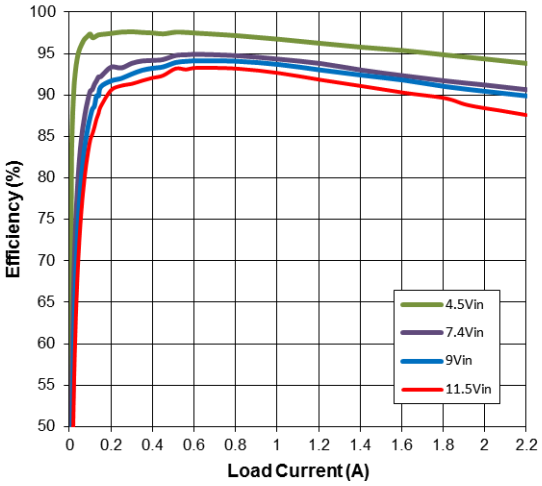


Figure 9: Ch 2 Efficiency (Vout = 4.25 V)

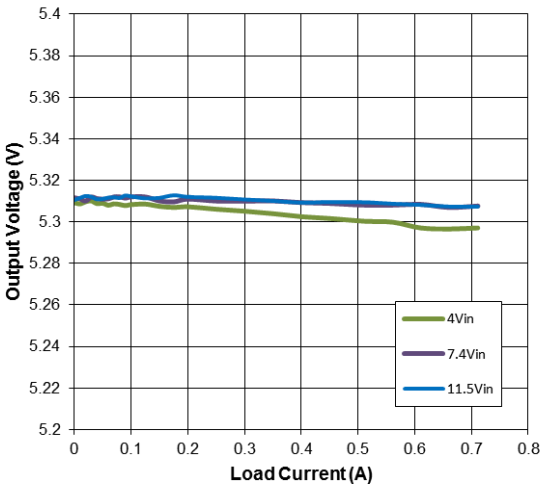


Figure 12: Ch 1 Load Regulation

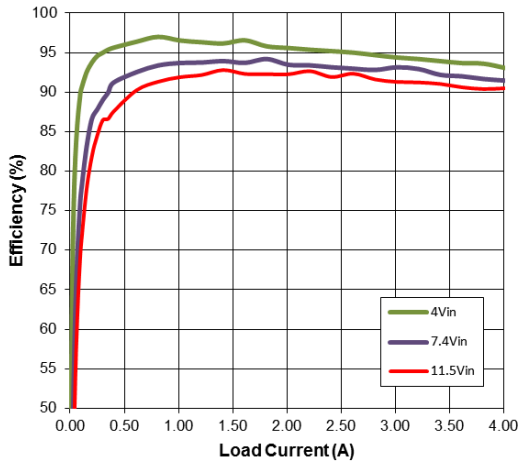


Figure 10: Ch 3 Efficiency (Vout = 3.3 V)

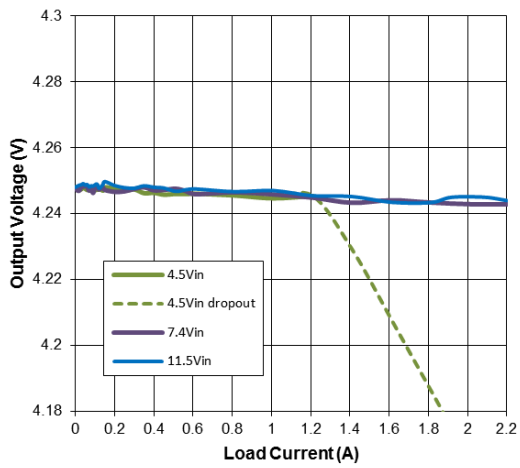


Figure 13: Ch 2 Load Regulation

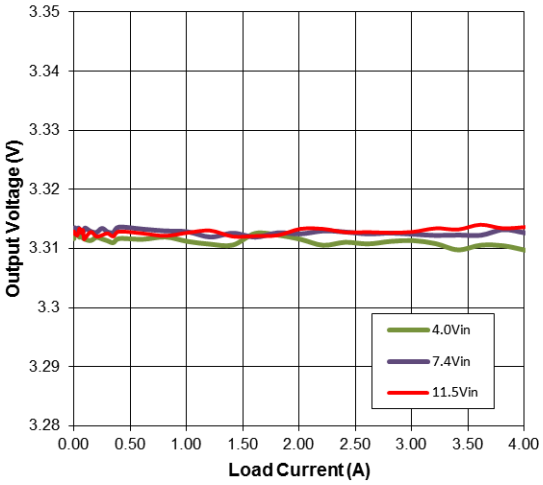


Figure 14: Ch 3 Load Regulation

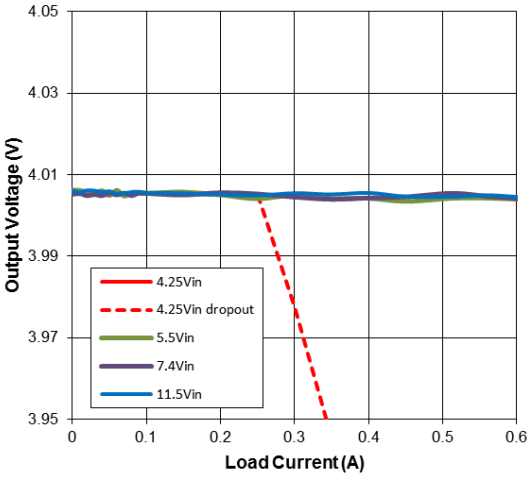


Figure 15: Ch 4 Load Regulation

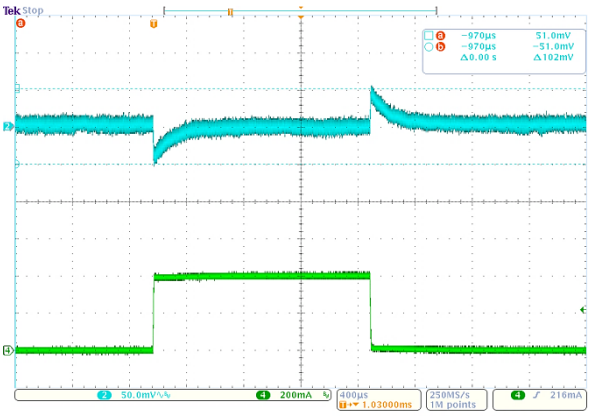


Figure 16: Ch 1 Load Transient Response

(0 A to 0.4 A, 50 mA/µs)

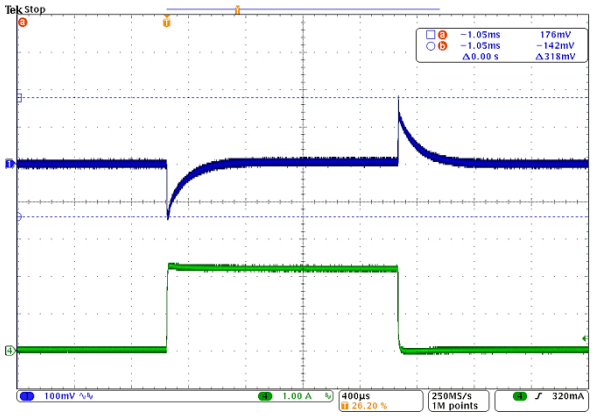


Figure 17: Ch 2 Load Transient Response

(0 A to 2.2 A, 250 mA/µs)

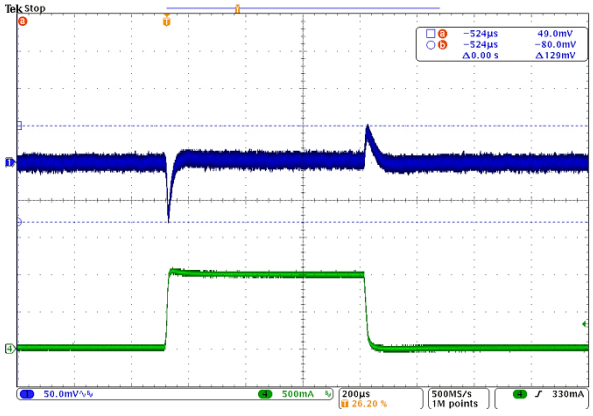


Figure 18: Ch 3 Load Transient Response

(0 A to 1.0 A, 55 mA/µs)

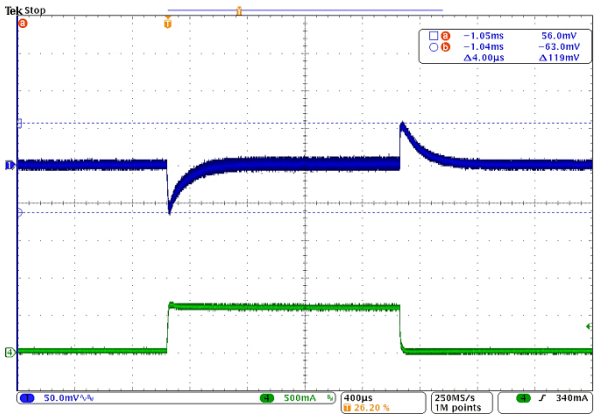


Figure 19: Ch 4 Load Transient Response

(0 A to 0.6 A, 50 mA/µs)

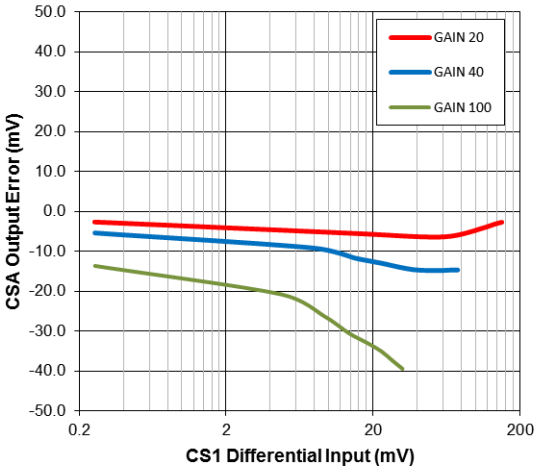


Figure 20: CS1 Accuracy

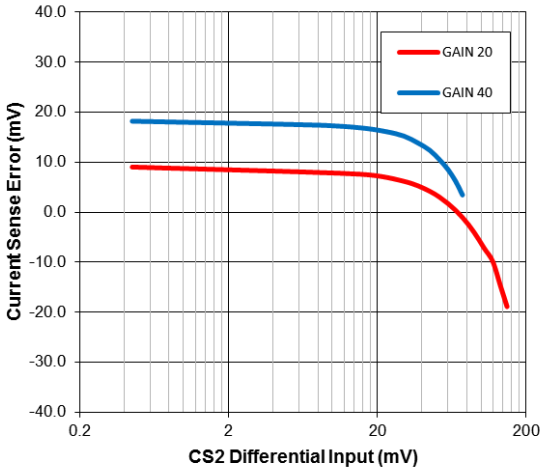


Figure 21: CS2 Accuracy

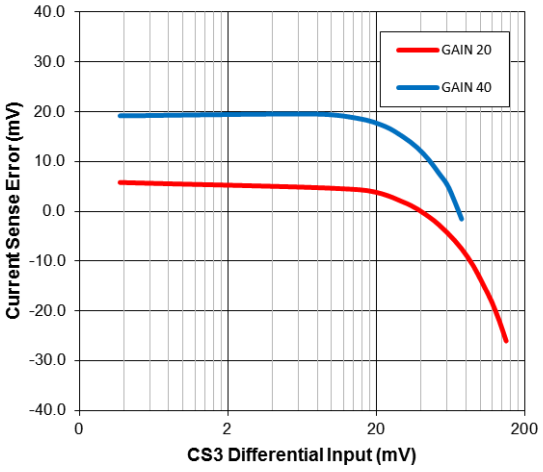


Figure 22: CS3 Accuracy

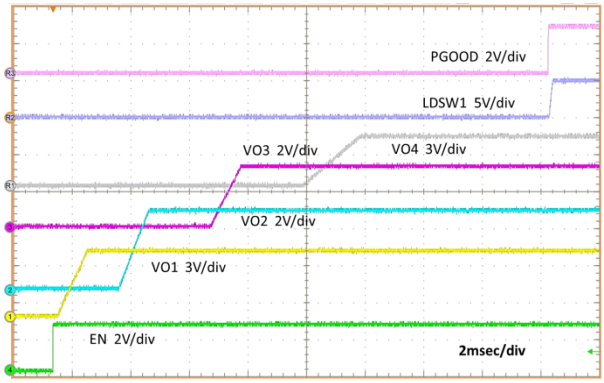


Figure 23: Example Start-up Sequence

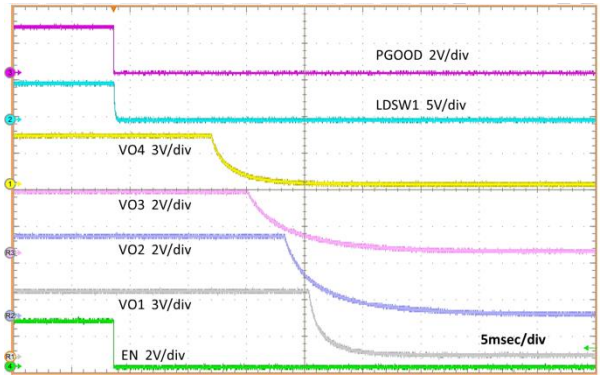


Figure 24: Shutdown Sequence

(Reverse mode, all channels discharge on)

8 Typical Schematic

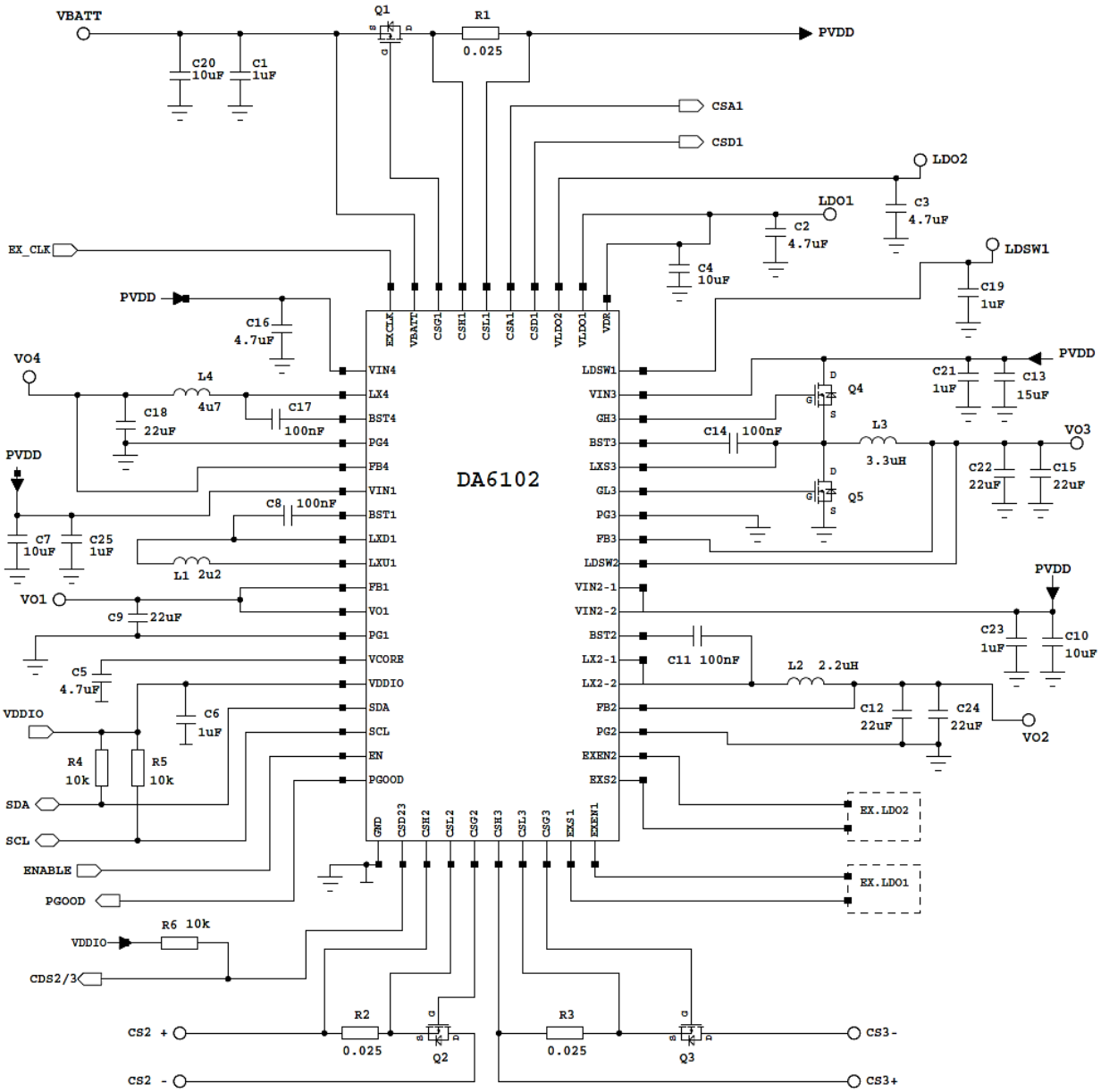


Figure 25: Typical Application Schematic

9 Functional Description

9.1 General

The DA6102 is a multi-channel Power Management Integrated Circuit (PMIC) designed to operate from a widely varying input supply to regulate multiple high efficiency outputs. As a system power block, the DA6102 provides two always-on LDOs, a battery side current sense and circuit breaker, and fully configurable sequencing and fault protection. The PMIC also includes two integrated buck converters, an integrated BuckBoost converter, a buck controller, and two external voltage monitors. Default register values are set by One Time Programmable (OTP) for output voltages, fault behavior, switching frequency, start-up sequence, and many other functions. All register settings can also be programmed directly via the I^2C interface.

Complete device functionality is described in detail below, where all component references refer to the Figure 25 schematic and register references refer to the register map in Table 13.

9.2 Always-on LDOs and Internal Load Switches

LDO1 and LDO2 are always enabled regardless of battery voltage or EN pin state. Each LDO's output must be bypassed with a minimum capacitance of 4.7 µF. For the LDOs and all other channels, it is recommended to use capacitors whose value is greater than 50 % of the nominal value at the operating voltage. A capacitor voltage rating of approximately twice the operating voltage is normally sufficient.

LDO1 and LDSW1

LDO1 operates in two states. When the Channel 1 output voltage is disabled or below the switch-over threshold (5.1 V typical), the LDO1 output voltage is set to 4.8 V. In this state, LDO1 is supplied directly from VBAT, and its load current capability is limited to 70 mA. In normal operation, with Channel1 enabled, the LDO1 input switches to Channel1 and its output is regulated at 5.0 V. In this state, the LDO1 current limit increases to 300 mA (minimum). Having two modes of operation improves system efficiency by reducing the input voltage to LDO1 when Channel 1 is available. In either state, LDO1 output accuracy is within ± 2% provided that its input supply is at least 200 mV above the target output voltage.

LDO1 connects internally to Load Switch 1, LDSW1, which is enabled and disabled via the EN1 register (0x05, D4). LDSW1 allows the always-on LDO voltage to be used as an independent channel with soft-start, sequencing, output discharge, current limit, and short circuit protection. To prevent overloading LDO1, LDSW1 begins limiting current when LDO1 drops below 4.5 V. However, as both outputs come from the same source, the combination of loads should not exceed the LDO1 current limit. LDSW1 soft-start is achieved by engaging a 70 mA current limit during the start-up period, thus preventing any sudden load steps on LDO1.

Additionally, LDSW1 has a Force-ON mode, set with the LDSW1F bit in register 0x22. In this mode, LDSW1 current limit is disabled and the on resistance is minimized. In Force-ON mode, LDSW1 is not controlled by the EN pin, but only by its EN1 register bit. If the EN pin is pulled low to shut down the PMIC channels, LDSW1 will remain on (along with LDO1 and LDO2) as shown in Figure 27 below. To prevent excessive droop on LDO1 when the EN pin is low, ensure that the LDSW1 current is below the 70 mA limit of LDO1.

Because Channel 1 serves as the primary supply for LDSW1 (via LDO1) in normal operation, an OV or SC fault shutdown on Channel 1 will cause LDSW1 to automatically switch off. This is the same functionality as FSCS and FOVS described in the short circuit and over-voltage protection sections.

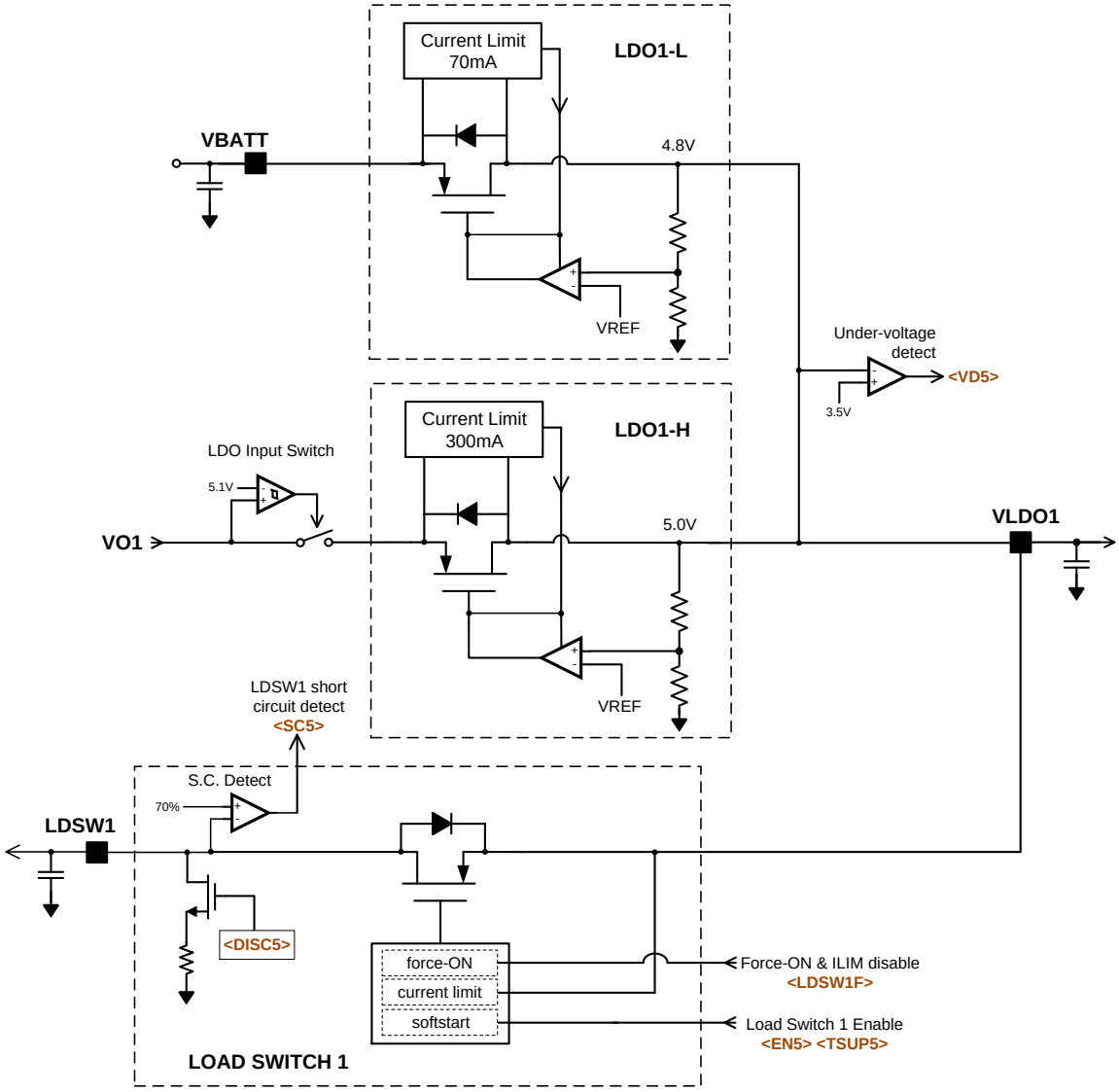


Figure 26: LDO1 and LDSW1 Architecture

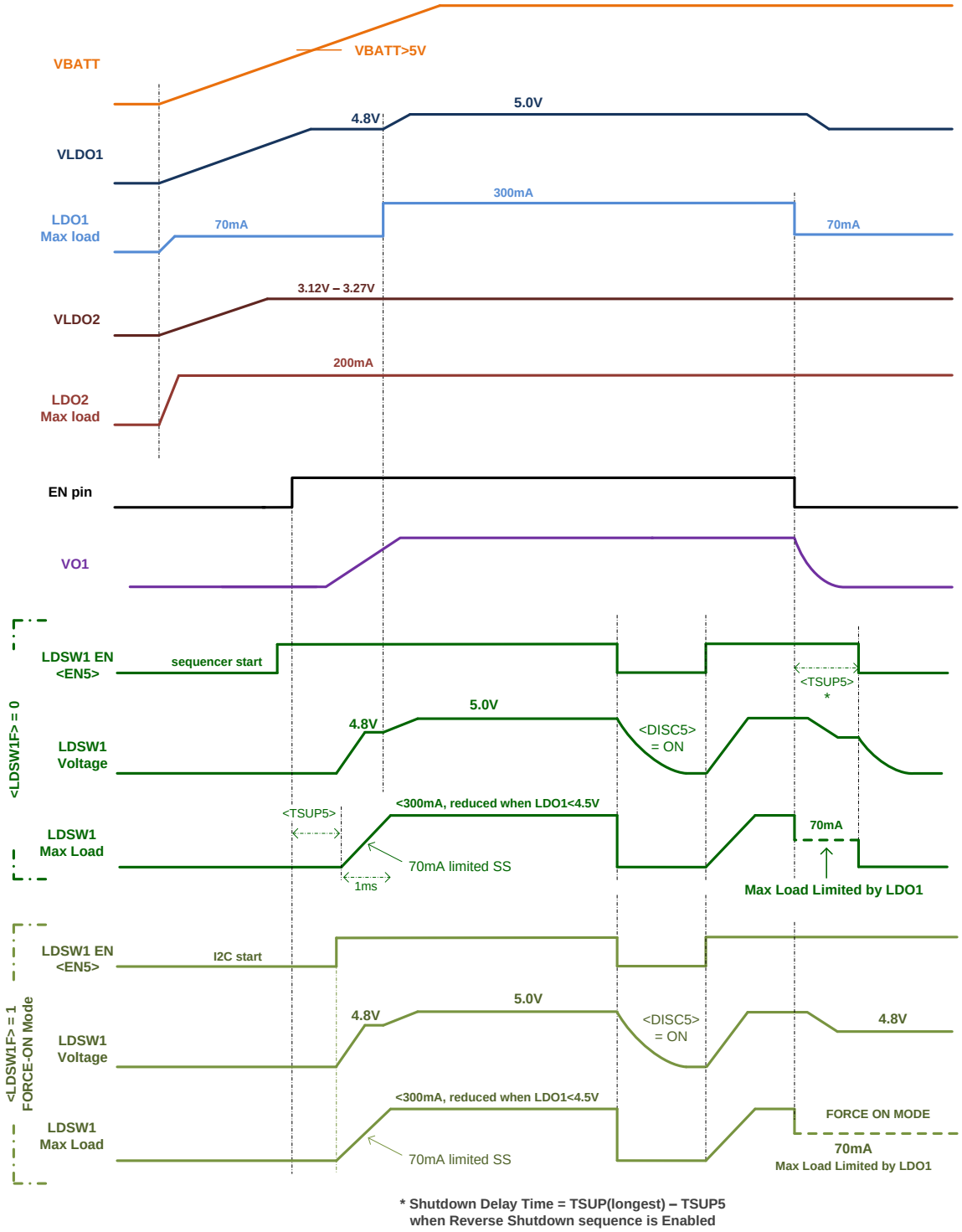


Figure 27: LDO Start-upStart-up and LDSW1 Timing

LDO2 and LDSW2

The LDO2 output voltage is programmable between 3.12 V and 3.27 V in 50 mV steps, from the CTL register (0x22, D5:4). The LDO2 current limit is fixed at 200 mA minimum, however there is no fault indicator associated with LDO2.

The LDO2 output is internally connected to Load Switch 2 (LDSW2). In a typical application when the PMIC is enabled, the LDO2 output will be bypassed by the higher efficiency switching regulator connected to the LDSW2 input. This is shown as Channel3 in Figure 28. This configuration improves system efficiency by eliminating the high losses of the LDO when in normal operation. With LDSW2

enabled through the EN1 register (0x05, D5) the voltage at VLDO2 is supplied through LDSW2. Note that the voltage at LDSW2 must be greater than the LDO2 set voltage. To ensure a smooth transition when LDSW2 is enabled, a fixed current limit is enforced for 1 ms. This limits glitches at VLDO2 and prevents reverse current from LDO2 to the supply connected to LDSW2. LDSW2 start-up delay can be programmed by sequencer but should only be enabled after the supply voltage (Channel3 typically) has reached its target.

Because Channel 3 typically serves as the primary supply for LDSW2 in normal operation, an OV or SC fault shutdown on Channel 3 will cause LDSW2 to automatically switch off. This is the same functionality as FSCS and FOVS, described in Section 9.12.

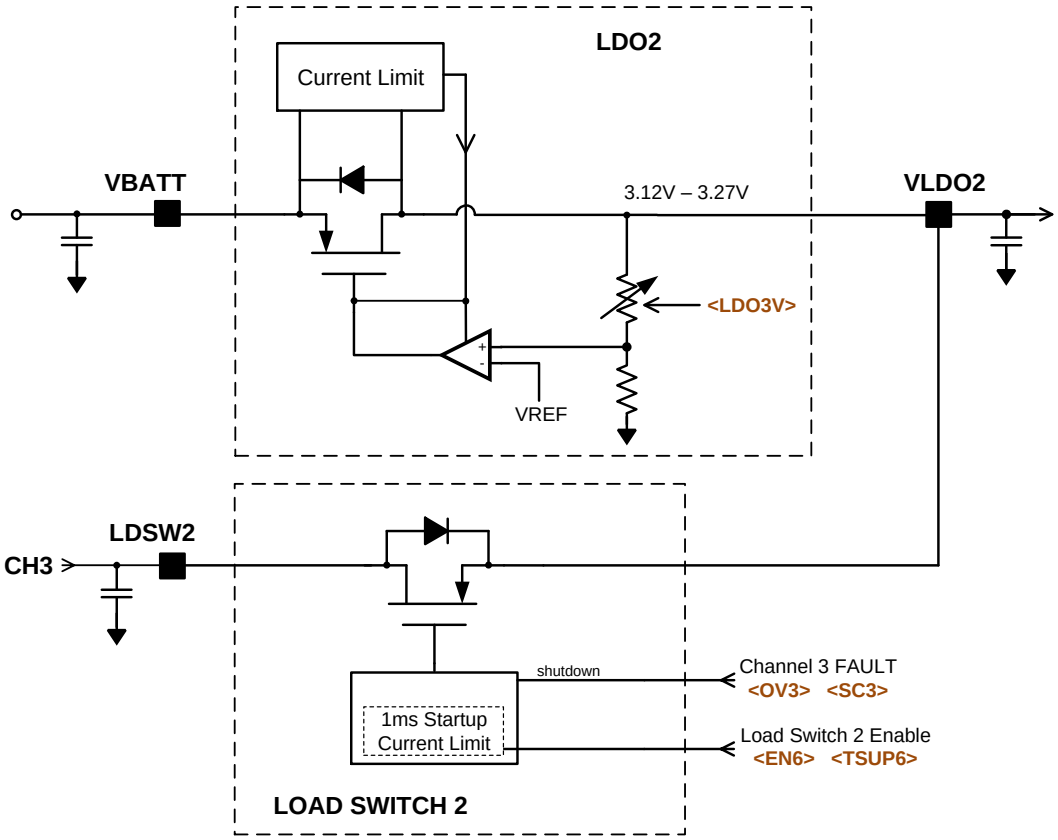


Figure 28: LDO2 and LDSW2 Architecture

9.3 ENABLE, UVLO, and Operating State Transitions

The DA6102 has multiple operating states including a low quiescent current standby mode and a wide hysteresis UVLO (Under-Voltage Lock-Out) feature that contribute to both a high system efficiency and robust performance. As the name implies, the always-on LDOs are always enabled, regardless of the state of the EN pin or battery voltage.

Referring to Figure 29, as the battery voltage increases from 0 V, the PMIC first crosses the upper UVLO threshold of approximately 3.8 V. Above this threshold the IC is initialized, allowing the OTP settings to be loaded and I^2C communication becomes active. Once the UVLO is released, the DA6102 is in standby mode with input quiescent current less than 10 µA. From the standby state, the EN pin can be driven high to start the sequencer and start up the desired channels. Once the sequencer begins starting the last channel, the PMIC is considered in Powered mode and all functions are active. Pulling the EN pin low at any time will start the powerdown sequencer and return the DA6102 to standby mode.

If the VBATT voltage drops to 2.9 V typical, the UVLO re-engages and all channels will shut down, including the CS blocks. However, the PMIC will not automatically restart if the VBATT voltage returns above 3.8 V. To restart after a UVLO event, the EN pin must be toggled. Below this lower UVLO threshold, all stored registers will be reset to their default values and the DA6102 is completely off with the exception of LDO1 and LDO2.

This large hysteresis in the UVLO circuit ensures that there is a high enough input voltage to support a smooth start-up with proper regulation, while at the same time giving additional headroom and time to keep the channels alive if the input voltage should droop during operation. Although all functions are active when the DA6102 is operating below 4 V, not all channels will be in regulation and some faults may be indicated such as under-voltage or current limit. To prevent momentary under-voltage droops at the input, follow all recommendations for input capacitors and use a minimum of 10 µF at the VBATT pin.

The DA6102 has a secondary UVLO threshold of 3.5 V at the VDR pin, referred to as VD5, see Section 9.12. VDR is supplied by the Channel 1 BuckBoost via external connection the VLDO1 pin. Therefore, if Channel 1 is not enabled, the VDR UVLO will supersede the battery UVLO.

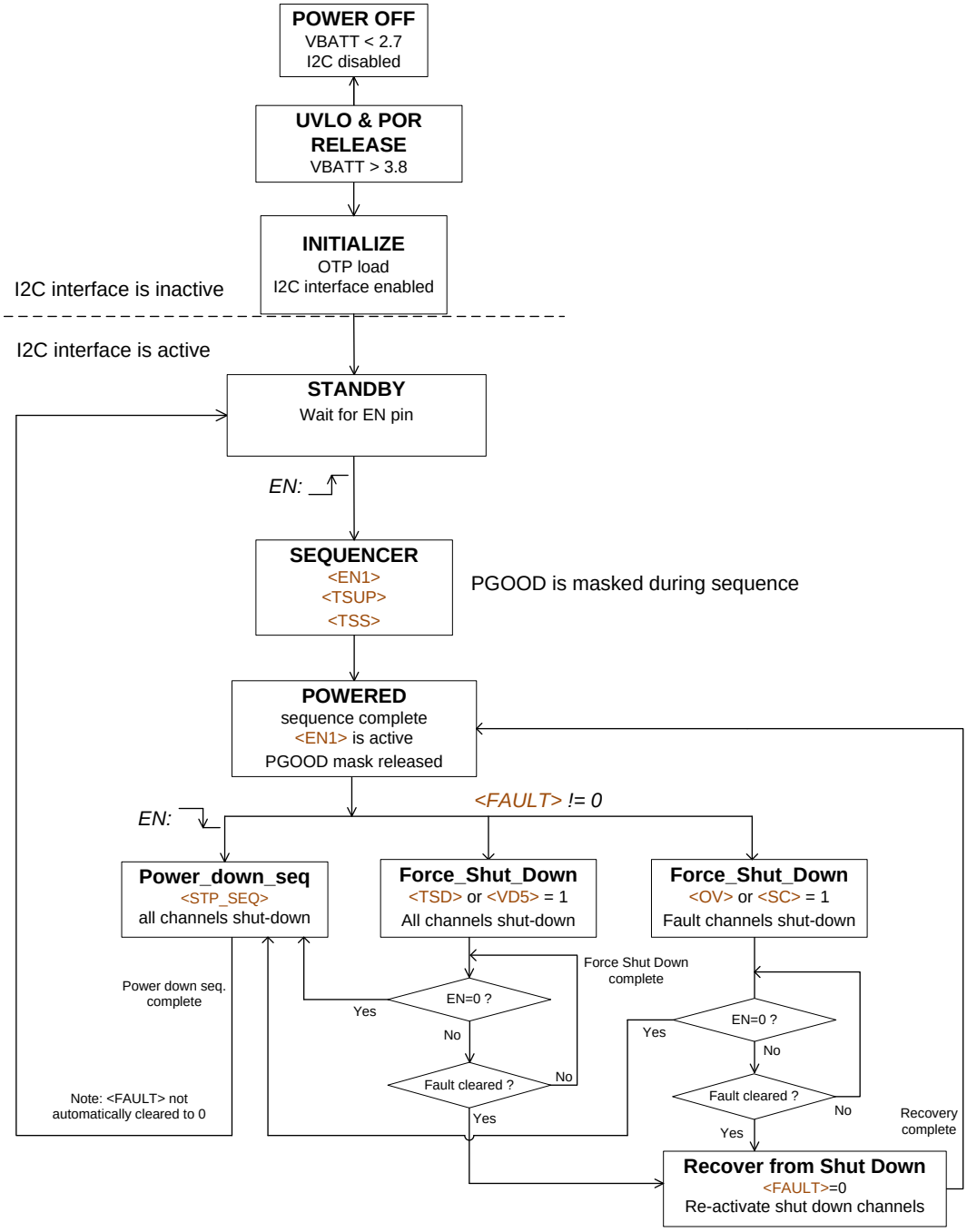


Figure 29: Operating State Transitions

9.4 Sequencer and Soft-start

The DA6102 features an integrated start-up sequencer for eight of the channel blocks: CH1, CH2, CH3, CH4, EXEN1, EXEN2, LDSW1, and LDSW2. Each of these channels can be set to start either automatically by sequencer control, or by direct register control. To turn on sequencer control, set the appropriate bit in the EN1 register (0x05) to high before driving the EN pin high. When the EN pin goes high, the start-up delay timers are initiated. Delay time for each channel can be set between 0 ms and 32 ms in the TSUP12 through TSUP78 registers. The programmed delay time sets the time interval between the EN pin rising and the beginning of the soft-start ramp.

The external LDO channels (EXEN1 and EXEN2) are digital outputs. Therefore no soft-start time applies and they will go high immediately after the start-up delay time expires. LDSW1 has a fixed start-up current limit and will begin to ramp up the output once the start-up delay time expires. LDSW1 start-up time can be calculated as shown below. The fixed current limit allows up to 10 µF to be charged within the 1 ms (typical) soft-start period.

$$T_{START-LDSW1} = \frac{C_{LDSW1} \times Vldo1}{70\,mA}$$

LDSW2 also has a fixed current limit during start-up which is designed to limit reverse current; it is not a soft-start function.

Channels 1 through 4 include programmable soft-start times. After the delay time for a channel has completed, that channel's output voltage will begin to ramp up according to the programmed soft-start time, TSS. Soft-start times are set in the TSS register (0x10) with a range of 1 ms to 10 ms.

The soft-start function prevents output voltage overshoot and excessive inrush current by slowly ramping up the output voltage in a controlled manner. Faster soft-start times will result in higher inrush current; larger output capacitance will also increase inrush current. To prevent a pre-biased output from discharging during start-up, each channel operates in DCM within the first 75% of the soft-start ramp.

The PGOOD pin will remain low until the last channel in the sequence has completed its soft-start ramp and its power good status bit (PGS, 0x01) is high.

During sequencer start-up, the EN1 register bits (0x05) can be written, but any channels to be included in the sequence must be set before the EN pin goes high. Once the sequence is completed any channel can be disabled or enabled at any time through the EN1 register.

When a channel is enabled by EN1 direct register write (not in the sequencer) the TSUP delay time register settings are not applied. The soft-start ramp set by TSS will begin as soon as the EN1 bit is set high.

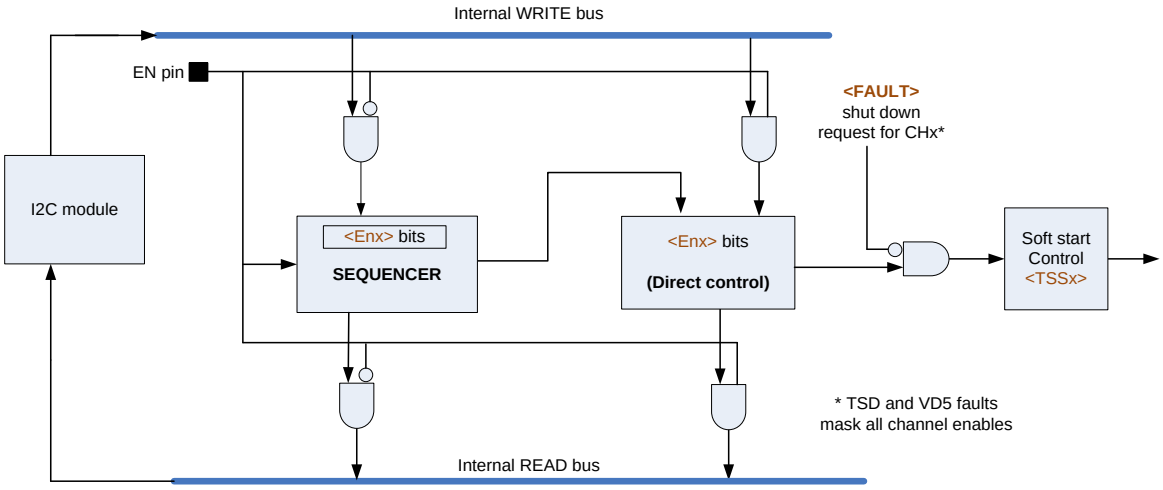


Figure 30: Sequencer, Enable, and FAULT logic

When the EN pin is pulled low, the shutdown sequencer is initiated. The shutdown sequencer can be set to shut down all channels immediately or in the reverse order from the start-up sequence. This option is available in the TSEQ register (0x11, D3). When shutting down in reverse order from start-up, all channels that were not initially set to sequenced start-up will be shut down immediately. Additionally there is no shutdown delay time applied to the first channel to shut down (last channel to start). Toggling a bit in the EN1 register after a sequenced start-up does not change a channel's status in sequenced shutdown.

Note that LDSW1 can be included in the start-up sequence, only if the LDSW1F bit (0x22) is set low. If LDSW1 is not in sequencer mode, it will be controlled only by the EN1 register and will not be shut down by the EN pin. After a FAULT shutdown, the EN pin can be toggled to restart the sequencer

and EN1 register bits can be written. However, channels that shut down will have their EN1 register bit outputs masked and will not turn on. Any FAULT condition must be first cleared by I^2C write to allow the channel to restart. A channel will restart immediately if the FAULT condition is cleared while its EN1 register bit is high.

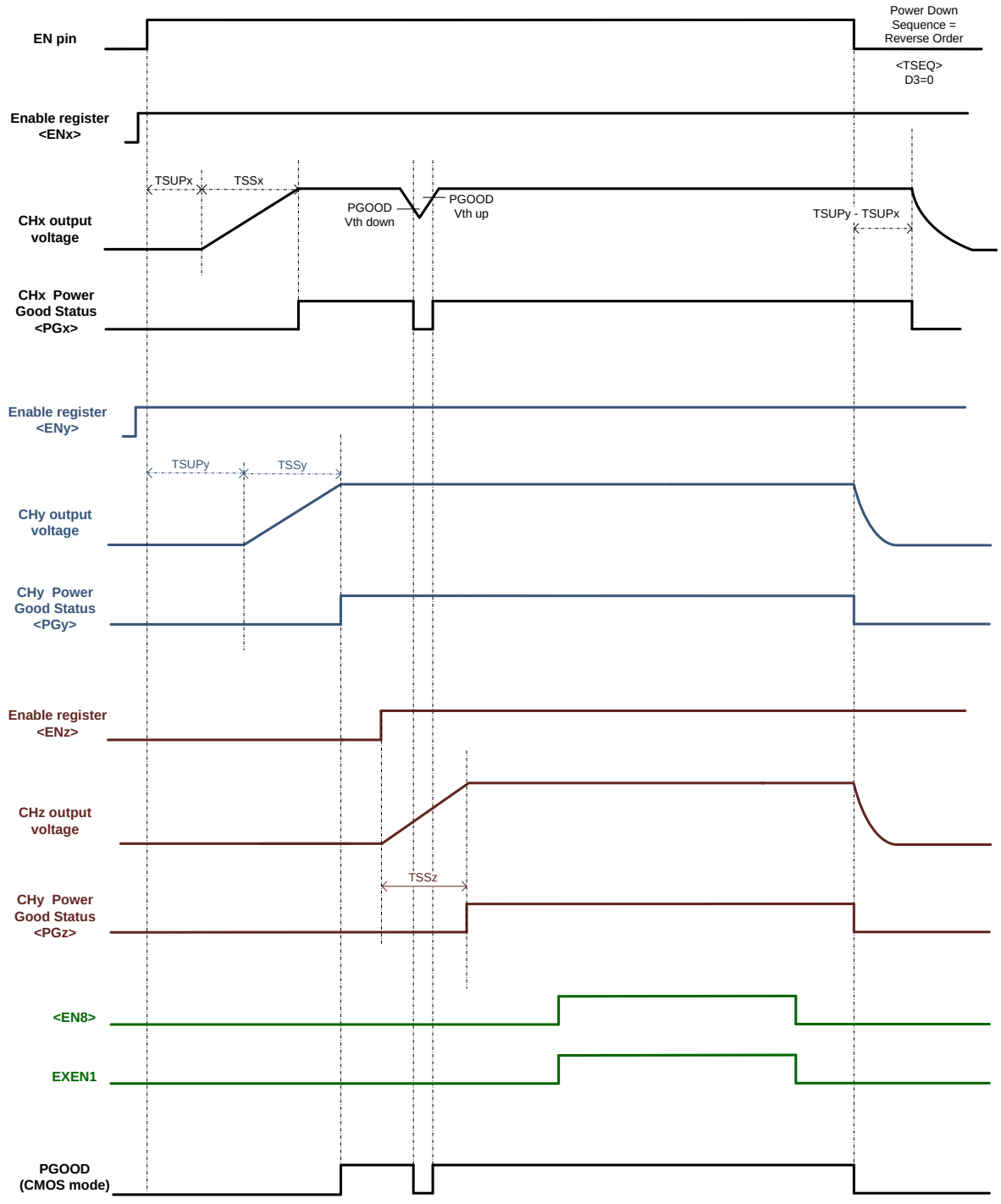


Figure 31: Sequencer Start-Up Example

9.5 Channel 1 to Channel 4, Common Features and Functionality

Basic Buck Operation

All four switching regulators are fixed frequency PWM control. Each switching regulator can support the full input voltage range up to 11.5 V and must be separately bypassed at the VIN pins. In steady state operation, a buck switching regulator works by alternately turning on the high side and low side switches with a duty cycle controlled to regulate the output voltage. When the high side turns on, LX equals VIN, the voltage across the inductor is Vin-Vout and inductor current ramps up. When the low side switch turns on, the LX voltage equals GND and the inductor ramps down. The average inductor current is equal to the load current, and will rise and fall as the load demands. The inductor ripple current is filtered by the output capacitors to provide a low ripple voltage at the output. The output voltage is sensed by the feedback pin which is compared to a reference voltage to generate the PWM duty cycle.

The duty cycle for a buck converter can be approximated as:

$$D_{BUCK} = \frac{Vout}{Vin}$$

Peak-to-peak inductor ripple current can be approximated as:

$$\Delta IL = \frac{(Vin - Vo)D}{fsw \times L}$$

And peak inductor current as:

$$IL_{PEAK} = \frac{\Delta IL}{2} + I_{LOAD}$$

Output Voltage and DVS

The output voltage for each channel is register programmable in 50 mV steps at registers DVS1 through DVS4 (0x0B to 0x0E). These registers set the reference voltage for each channel, and can be dynamically changed during operation. Each channel's voltage feedback pin (FB) should be connected at the output capacitor with the FB trace routed to avoid primary sources of noise such as inductor and switching nodes. Shielding FB traces with a ground plane is highly recommended.

When dynamically changing the voltage of any switching channel, the FB voltage will be stepped up or down towards the new target value in 50 mV steps. The time between each step is set at 50 µs or 100 µs using the TSEQ register (0x11, D2). The linearity of the output voltage response depends on several factors including inductance, output capacitance, step time, and switching frequency. Larger output capacitance values will require more current to charge (or more negative current to discharge) which may result in overshoots or undershoots at the output. To avoid false error detection, 10 ms OV and SC masking times can be enabled in the TSEQ register (0x11, D1:D0). The power good status bits (0x01) for each channel are masked during DVS transitions.

Switching Frequency

Each channel's switching frequency can be independently selected within a 1 MHz to 3 MHz range. The source clock must be selected as either internal or external. If internal, any of four frequencies can be selected, all with an accuracy within ± 2 %. An overview is shown in Figure 32 below. Channel 3 switches 180 degrees out of phase with the other channels. This reduces input ripple current, which helps to reduce input noise and stress on the input capacitors.

If the external clock option is selected via the CLKS register (0x13, D0), the external clock must be between 1.5 MHz and 3 MHz with a near 50 % duty. The external clock is applied to all channels. However, the external clock can be divided in half, providing two frequency options for each channel.

It is not recommended to divide external clock frequencies of less than 2 MHz. Frequencies higher than 3 MHz or lower than 1 MHz cannot be used.

If the external clock becomes inactive, or the external frequency is outside of the specified range, the DA6102 automatically switches to the internal clock. Similarly, when a valid external clock is detected at the EXCLK pin, the external clock will take over from the internal clock (assuming that external clock is selected in the CLKS register). The switching clock operation is designed to ensure robust operation in any condition. However, real time clock detection and switch-over requires several cycles of delay. Therefore, to avoid output voltage glitches during normal operation the clock frequency should not be changed, nor should control be switched from internal to external clock or vice versa during PMIC operation.

In general, a higher switching frequency requires smaller external components and can have a better transient response. The trade-off is that a higher switching frequency will have higher losses and therefore lower efficiency.

Table 9: External Clock and Switching Frequency Selection

Clock Select <CLKS> 0x13 [D0]	External Clock Input EXCLK	Clock Divider <CLKS> 0x13 [D4:D1]	Switching Frequency Ch1 to Ch4
1 (External)	<1.5 MHz	-	Not allowed: internal clock is used
	1.5 MHz to 2 MHz	1 (x1/2)	Not allowed
	1.5 MHz to 2 MHz	0 (x1)	1.5 MHz to 2 MHz
	2 MHz to 3 MHz	0 (x1)	2 MHz to 3 MHz
	2 MHz to3 MHz	1 (x1/2)	1 MHz to 1.5 MHz
	> 3 MHz	-	Not allowed: internal clock is used

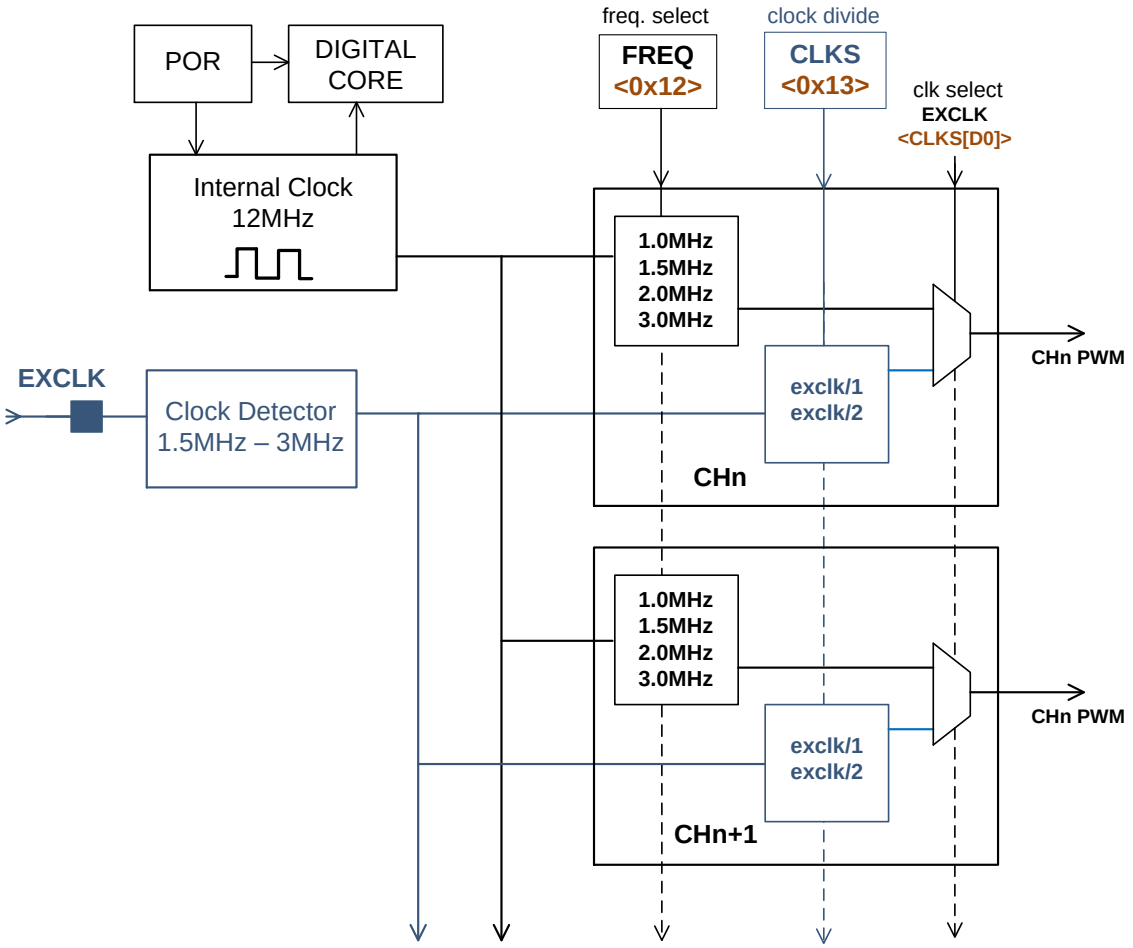


Figure 32: Frequency Selection and Distribution

BST, VDR, and Pulse Skipping

For the highest efficiency, all of the switching channels in the DA6102 use NFETs, except for the Channel 1 high side boost switch. NFETs require a drive voltage higher than the LX voltage, which is generated by the bootstrap capacitor at the BST pins. When the low side switch is on, the LX pin is at GND and the bootstrap capacitor is charged to approximately 5 V from VDR through an internal switch. When the high side turns on, the LX voltage increases to VIN and the voltage at BST follows, remaining 5 V above LX. For each switching channel in the DA6102, the BST voltage is the drive voltage for the high side NFET. A 100 nF capacitor at BST is sufficient to provide gate drive under all conditions. However, some time is required to continuously replenish the bootstrap charge. This time is imposed as the minimum high side off-time of 83 ns (on all channels). The minimum off-time defines the maximum duty cycle capability for a given frequency as shown below.

$$D_{MAX} = 1 - (fsw \times 83ns)$$

VDR supplies the gate drive voltage rail for all switching channels. The VDR pin must be externally connected to LDO1. The VDR voltage charges the BST capacitor for the high side drive and also drives the low side. Due to the fast switching currents required, VDR must be bypassed with a minimum of 10 µF ceramic capacitor placed close to the pin. When the Channel 1 BuckBoost is enabled, LDO1 and therefore VDR have a high enough input voltage for sufficient gate driving even when the battery voltage drops below 4 V. This is also the highest efficiency configuration. However, should the battery voltage drop below 4 V without Channel 1 enabled, the gate drive may not be sufficient, in which case a VD5 fault will occur.

The maximum duty cycle defines the point at which the input voltage is too low for the output voltage to be regulated. If the input voltage continues to drop, the duty cycle will remain fixed at maximum

thus causing the output voltage to drop. In this condition, up to eight off pulses can be skipped in order to maximize the duty cycle and extend the operation range of the channel. Maximum duty cycle with pulse skipping enabled is calculated as shown below.

$$D_{MAX-PSM} = 1 - \left(\frac{fsw \times 83ns}{9} \right)$$

Pulse skipping is available on channels 2, 3, and 4 via the CTL register (0x22), and on Channel 1 via BB_OPT (0x31). With or without pulse skipping, PGOOD and short circuit detection will be triggered as input voltage falls below the maximum duty.

Current Limit and Short Circuit Protection

The DA6102 incorporates cycle-by-cycle current limit on each channel. The sensed high side switch current that is used for PWM control is also used to limit the peak current. Each channel has a specified current limit threshold based on the current handling capability of that channel. When the inductor current ramps up to a peak value equal to the current limit threshold, the high side switch is immediately turned off until the next cycle. This ensures that the inductor current will not exceed the limit. Because inductor ripple current is not constant, the average load current at which the current limit is triggered will depend on frequency, inductance, and duty cycle. The current limit threshold as average load current can be calculated as shown follows.

$$I_{LOAD\_MAX} = ILIM - \frac{\Delta IL}{2}$$

The peak current limit threshold must be taken into consideration when selecting an inductor value and switching frequency. For a given inductance, ripple and peak current will increase with lower frequency. Selecting too low an inductor value may cause a channel to trigger the current limit below the required load current.

When in current limit, the switching duty cycle is reduced causing a reduction in output voltage (as the load increases, duty cycle decreases). When the output voltage drops to 85 % of nominal, the PGOOD register (PGS, 0x01) for that channel will go low. To prevent runaway inductor current, when the output is below 85% one switching cycle will be skipped after a current limit detection. If the load current continues to increase, forcing the output voltage to drop to 70 % of nominal, the short circuit status register (SCS, 0x02) for that channel will go high. The LDSW1 output also has a short circuit detection function nearly identical to that of the switching channels.

Furthermore, if the output voltage drops below 50 % of nominal, because of an output short to ground for example, the HDSRT flag (D7 in the FAULT register) will go high after four current limit cycles and the affected channel will shut down. Writing ‘1’ to the HDSRT bit will clear the fault flag and restart the channel.

Each of the DA6102 switching channels can respond to a short circuit condition in several ways: ignore, shut down, shut down after a delay, or shut down multiple channels. The SC shutdown is enabled or disabled for each channel in the SCM register (0x16, D3:D0). When set to not masked, the channel will immediately shut down. When set to “masked”, the channel will continue to operate, ignoring the short circuit condition.

A short circuit event is triggered by the output voltage dropping below 70% of nominal, which may be caused by an intermittent excessive load. To avoid shutting down a channel due to a transient event, SC shutdown can be delayed via the TSEQ register (0x11, D0). Setting the TSC bit to 0 provides a 10 ms blanking time during which a SC condition is ignored. If the short circuit continues after 10 ms, the channel will be shut down.

Any of the four switching regulator channels can also be set to shut down if a short circuit occurs on any other channel. This is set in the FSCS register (0x17, D3:D0).

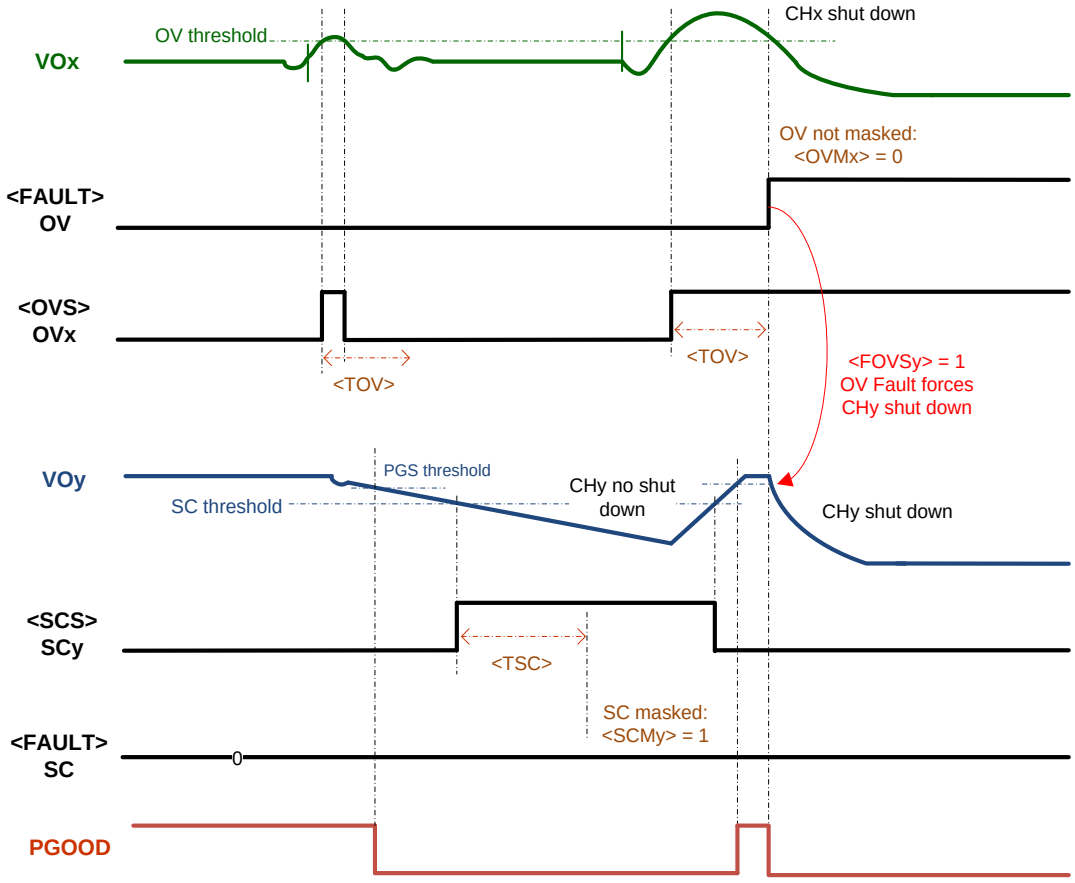


Figure 33: OV and SC Fault Protection Example

Over Voltage Protection

As an additional level of fault protection, the DA6102 switching regulators include over-voltage (OV) detection and options for automatic shutdown. If the sensed output voltage of any channel increases above 120 % of nominal (110 % for Channel1), the channel immediately stops switching and the OV status register (0x03) goes high. The DA6102 can respond to an OV event in several ways: ignore, shut down, shut down after a delay, or shut down multiple channels.

The OV shutdown is enabled or disabled for each register in the OVM register (0x15, D3:D0). When set to “not masked”, the channel will immediately shut down and when set to “masked”, the channel will continue to operate, ignoring the OV condition.

Over-voltage is most commonly caused by a dynamic change in output voltage setting or by an output voltage overshoot due to current limit recovery. To avoid shutting down a channel due to a transient event, OV shutdown can be delayed via the TSEQ register (0x11, D1). Setting the TOV bit to 0 provides a 10 ms blanking time during which an OV condition is ignored. If the over-voltage continues after 10 ms, the channel will be shut down.

Finally, any of the four switching regulator channels can be set to shut down if an OV event occurs on any other channel. This is set in the OVM register (0x15, D7:D4), and shown in Figure 33: with its FOVS bit set high, Channel y shuts down when any other channel shuts down due to OV fault, Channel x in the example.

Output Voltage Discharge

Each switching channel includes an output voltage discharge function which is enabled or disabled by the DISC register (0x18). When a channel is disabled either by shutdown sequence (EN pin), EN register, or fault shutdown, a 100 Ω typical resistance will discharge the output voltage through the FB pin. This ensures a smooth output voltage ramp-down. It also provides a known state at the outputs when restarting the sequencer.

LDSW1 also has an output voltage discharge feature, connected at the LDSW1 pin. Unlike the switching channels however, LDSW1 does not discharge by default when the EN pin is pulled low. The LDSW1 output discharge is activated only when LDSW1 is disabled by the <EN1> register.

Control Architecture and Loop Compensation

Switching channels 1, 2, and 4 use peak current mode control with internal compensation. Peak current mode control delivers excellent stability over a wide input voltage range, allowing the transient response to be easily optimized for a wide range of application conditions. In general, current mode control generates the internal PWM ramp signal by sensing the inductor current. Inductor current is sensed across the high side switch of each channel. Because this is a fast switching and noisy sensing point, some blanking time is required at turn-on to ensure that switching noise does not affect the switching stability or the current limit sensing. The blanking time is equivalent to the minimum on-time of 83 ns for all channels. Care should be taken to minimize the noise at the VIN pins by placing the input caps as close as possible to the pins. The minimum on-time restriction creates a robust control loop and is sufficiently short to maintain regulation at the maximum input voltage in most conditions. At the maximum switching frequency of 3 MHz, channels 3 and 4 may skip pulses to maintain regulation at high input voltage and low output voltage settings.

Because Channel 3 drives external FETs, current sensing could be easily affected by PCB trace parasitics, variations in FET characteristics, and external noise sources. Therefore, Channel 3 uses voltage mode control architecture, which is more robust against noise as compared to current mode control. Voltage mode control generates an internal PWM ramp signal rather than using the sensed inductor current. Although not required for control, the same 83 ns minimum on-time restriction is imposed on Channel 3.

The DA6102 is internally compensated with default settings that ensure stability with the typical component values shown in Table 11. Channels 2, 3, and 4 require that the slope compensation parameter (register 0x20) be set according to the selected inductor as shown in Table 10. This is a required setting to ensure stability over the wide range of operation. For a detailed description of how to optimize the transient response of all switching channels, refer to Appendix A.

Table 10: Recommended Slope Compensation Settings: CH1, CH2, and CH4

Nominal Inductance	Slope Setting, SLP <0x20>		
	Channel 1	Channel 2	Channel 4
1.0 µH to 1.8 µH	01	01	-
2.0 µH to 2.6 µH	00	00	01
2.7 µH to 3.3 µH	11	11	01
3.5 µH to 4.5 µH	10	10	01
4.7 µH to 5.7 µH	10	10	00
5.8 µH to 9.0 µH	10	-	11
> 9.0 µH	-	-	10

Note 1 The values shown in Table 10 are nominal inductance values and allow up to 30 % derating.

The voltage mode control of Channel 3 requires a more complex compensation scheme, based on both L and C values. The internal compensation for Channel 3 is set in the FZ23_EFET (0x21) register. First calculate the LC double pole as shown in Register Table 34, and then set the register accordingly. Alternately, Channel 3 can be compensated using the CMP3 register (0x33), see Appendix A. When calculating the double pole frequency, derated L and C values should be used to match actual operating conditions. There is also a PWM ramp setting option for Channel3 at register 0x20, SLP_VO3. The default setting is recommended for most applications.

9.6 Channel 1, BuckBoost Regulator

Channel 1 is a 4-switch BuckBoost. This channel consists of two buck switches connected between VIN1, LXD1, and GND; and two boost switches connected between VO1, LXU1, and GND. For most of the input voltage range, where the battery voltage is greater than VO1, channel 1 will operate in buck mode. In buck mode, the high side boost switch is turned on at 100% duty, which is the most efficient mode of operation.

As the input voltage approaches VO1 and the high side buck duty increases to 80%, the boost stage turns on. When in BuckBoost mode, the buck switch operates at a nearly constant duty cycle, while the boost duty varies with input voltage. The BuckBoost turn-on threshold can be estimated as shown:

$$Vin_{BOOST} = \frac{Vout}{80\%}$$

And once in BuckBoost mode (assuming 80% buck duty) the boost duty can be calculated as:

$$D_{BOOST} = 1 - \frac{Vin \times 80\%}{Vout}$$

Once the boost begins switching, Channel 1 can maintain regulation with input voltages as low as 2.9 V. In BuckBoost mode, all four switches are switching with the boost stage operating at increasing duty cycle as input voltage decreases. Channel 1 does not have a boost-only mode.

The buck to BuckBoost transition point can be adjusted if necessary via the BB_OPT register (0x31). A lower duty threshold will degrade efficiency as there will be more time spent in the 4-switch BuckBoost region. However, a lower threshold may improve the performance when transitioning between modes. The default setting of 80 % is recommended for nearly all applications. In some cases such as high switching frequency, the buck may hit maximum duty cycle before the BuckBoost transition occurs. As the input voltage drops lower than this point, Channel1 will drop out of regulation before the boost stage begins switching. To prevent this, either reduce the transition threshold, or enable the pulse skipping function which essentially increases the maximum duty cycle capability.

Channel 1 maximum load current is rated to 700 mA, which includes the current required to support the LDO1 output, LDSW1, and VDR rail. The maximum expected load from the VO1 pin is expected to be less than 500 mA. Because Channel 1 supports additional internal loads, the current limit threshold is set accordingly.

Although Channel 1 is capable of regulating from very low input voltage, load current capability may be limited as input voltage drops. The maximum peak inductor current occurs in BuckBoost mode and can be approximated as shown below.

$$IL_{PEAK\_CH1} = \frac{Iout}{1 - D_{BOOST}} + \frac{Vin \times D_{BOOST}}{2 \times fsw \times L}$$

Highest peak and average inductor current occurs at the minimum input voltage.

Channel 1 can also be configured to operate as a buck-only regulator. This function is enabled in the BB_OPT register (0x31). To configure Channel 1 as a buck-only switching regulator, disconnect L1 from the LXU1 pin and connect it directly to the output cap and FB pin. The VO1 and LXU1 pins should be connected to ground to minimize leakage current. In buck only mode, the pulse skipping function remains available and operates the same as the other switching channels.

9.7 Channels 2 and 4, Buck Regulators

Channels 2 and 4 are integrated synchronous buck switching regulators with nearly identical control and features. Channel 2 has a maximum load current capability of 2.2 A with an output voltage range of 3.0 V to 4.55 V. Due to the low on-time required at high input voltage, Channel 2 should be operated at a maximum switching frequency of 2 MHz. If the on-time reaches minimum, Channel 2 will be unregulated at higher input voltage.

Channel 4 maximum load current is 600 mA with an output voltage range of 3.2 V to 4.2 V. Unlike Channel 2, Channel 4 will maintain regulation at up to 3 MHz by engaging on-pulse skipping when the on-time reaches minimum. As described above, either of these channels will reach maximum duty cycle and drop out of regulation when the input voltage approaches the nominal output setting.

9.8 Channel 3, Buck Controller

Channel 3 is a synchronous NFET controller intended as a high current intermediate rail regulator. Using Channel 3 to step the battery voltage down to 3.3 V, followed by point of load regulators for low voltage, high current processor loads is typically more efficient than supplying low voltage rails directly from the battery. As a controller, the Channel 3 load capability can be easily scaled by selecting the appropriate external FETs. Using external FETs also provides better thermal management by separating the main source of power loss (and heat generation) of Channel 3 from the DA6102.

Pins GH3 and GL3 are the gate drive pins for the external FETs. GL3 drives the low side switch at the VDR voltage while GH3 drives the high side at the BST voltage (LXS3+VDR). In low input voltage conditions, it is recommended to have Channel 1 enabled to ensure sufficient gate drive voltage for Channel 3.

Two separate input capacitors are required for Channel 3. One must be placed close to the high side switch to provide a low inductance path for the instantaneous switch current when the switch turns on. While the value of this input cap depends on the load current required, in general capacitance greater than 10 µF for a 2 A design and 22 µF for a 4 A design is recommended. The second input capacitor should be placed near to the VIN3 pin. This capacitor serves as a high frequency bypass for high side current sensing. A value of 1 µF is typically sufficient for this bypass capacitor.

Channel 3 inductor current is sensed as the voltage drop between VIN3 and LXS3 (across the Rds_on of the external FET). This signal is used to detect current limit. As with all switching regulator channels, there is a minimum on-time of 83 ns required to avoid falsely sensing switching noise. The current limit has two threshold options which are configured in the FZ23_FET register (0x21, D4). The resulting peak current limit can be calculated as follows.

$$I_{ILIM3} = \frac{V_{ILIM3}}{Rdson}$$

Where VILIM3 is 180 mV minimum (at the high setting) and the current limit value is peak inductor current. It is important to note that Rds_on has a large variation over temperature which will cause a corresponding variation in the current limit threshold. Therefore, the current limit should be calculated using the maximum Rds_on value.

9.9 Inductors, Output Capacitors, and Input Capacitors

Inductor Selection

More than any other component, selecting an inductor requires a balancing of trade-offs between efficiency and solution size. However, there are two criteria which must be met for proper converter operation. First, the inductor for each channel is first selected based on ripple current. A typical guideline is to design for a peak to peak ripple current equal to 30 % to 50 % of nominal load current.

$$L_{MIN} = \frac{(Vin - Vo) \times Vo}{Vin \times fsw \times 0.50 \times Iload}$$

Lower inductor values will result in higher ripple content and lower efficiency, with the benefit of requiring less board area. Once the inductor value is selected, confirm that the worst-case peak inductor current is below the current limit threshold. Also consider that the Channel 3 inductor selection will affect its compensation settings and overall loop stability.

The second criterion for inductor selection is current rating. The inductor must have an rms (or average) current rating higher than the maximum load capability of the channel. More importantly, the saturation current rating must be greater than the maximum peak current. Use the equation given earlier for ILpeak to determine the maximum peak current requirement, using maximum load and maximum input voltage.

Another important selection factor is the DCR of an inductor. DCR typically accounts for a large percentage of power losses and should be considered carefully. Higher inductance values will typically have a larger DCR for a given package size.

Output Capacitor Selection

The output capacitor filters the output ripple and provides the instantaneous current during load transients. Larger capacitance values reduce output ripple and improve load response. The DA6102 is designed to work well with a very wide range of capacitance as indicated in Table 11. Within the range shown, the required capacitance is determined by the transient and PCB area requirements. At higher switching frequencies, less capacitance is required to achieve the same performance. Since the minimum value for each channel is based on loop stability requirements, it is not recommended to reduce the output capacitance below this value. As mentioned previously, the Channel 3 output capacitor in combination with the inductor must be within range of the compensation register FZ23_EFET (0x21).

Input Capacitor Selection

In a buck switching regulator, input current is pulsed via the high side FET with a high slew rate. This current is the primary source of noise and radiated EMI in a buck switching regulator. Therefore, the input capacitor is critical to providing a low impedance path for this current. Low ESR ceramic capacitors must be used, with minimum recommended values given in Table 11. The input capacitor for each channel must be placed as close as possible between the VINx and PGx pins, preferably connected without vias. It is also good practice to use multiple values of capacitor, rather than one large capacitor.

In addition to the input capacitors on each channel, at least one bypass capacitor of at least 10 µF must also be placed at VBATT.

Table 11: Recommended Inductor and Output Capacitor Values

Channel	Switching Frequency	L	Total Cout Range	Minimum Input Capacitance
1	1 MHz/1.5 MHz	3.3 µH to 6.8 µH	22 µF to 322 µF	10 µF
	2 MHz/3 MHz	1.5 µH to 3.3 µH		
2	1 MHz/1.5 MHz	2.2 µH to 4.7 µH	44 µF to 124 µF	10 µF
	2 MHz/3 MHz *	1 µH to 3.3 µH		
3	1 MHz/1.5 MHz	1.5 µH to 3.3 µH	44 µF to 244 µF	15 µF
	2 MHz/3 MHz	1 µH to 2.2 µH		
4	1 MHz/1.5 MHz	5.6 µH to 15 µH	22 µF to 322 µF	4.7 µF
	2 MHz/3 MHz	2.2 µH to 6.8 µH		

Note 1 The capacitance values shown are nominal and allow up to 50 % derating. Channel 3 inductance assumes a 2 A nominal load. 3 MHz operation is not recommended for Channel 2.

9.10 CS1, CS2, and CS3: Current Sense and Load Switches

The DA6102 includes three external load switch controllers with current sensing. As blocks these are referred to CS1, CS2, and CS3. Each has programmable current sense gain and fault thresholds. The current sense blocks are not controlled by the EN pin and cannot be programmed by sequencer. Instead, they are enabled and disabled directly via the EN2 register (0x06). The current sense channels can be enabled even when the EN pin is low.

CS1

CS1 is a load switch controller combined with highly accurate current sensing and fault detection intended for use as an input side circuit breaker. In a typical application all switching channel inputs are connected to the output of CS1 (PVDD in the typical schematic). For this reason, there is no start-up sequence available for CS1, as it should be the first channel enabled. For proper operation, CS1 must be enabled via EN2 register (0x06, D3) prior to enabling any channel or starting the sequencer. CSG1 is internally pulled up by 1 MΩ (typical) to the VBATT pin.

The CSG1 pin connects to the gate of an external PFET. When enabled, the gate is pulled approximately 5 V below the VBATT voltage to turn on the switch. CSH1 and CSL1 connect to an external current sense resistor to monitor to input current to the system. In a typical configuration, all system current will flow through this sense resistor, with the exception of LDO1 and LDO2 when EN is low. The current sense signal is amplified by a gain of 20 V/V, 40 V/V, or 100 V/V, programmable with the CS11 register (0x19, D7:6). The resulting scaled input current can be monitored directly at the CSA1 pin. Thus, using sense resistor values of 50 mΩ, 25 mΩ, or 10 mΩ will result in a 1 V/A signal at CSA1. The inputs to the current sense amplifier have a maximum differential voltage rating of 150 mV. For the best accuracy, it is recommended to use the largest sense resistor possible while keeping the voltage within this range.

$$Vsense\_\max = Iin\_\max \times R1$$

As protection against system over-current, CS1 includes both a programmable over-current threshold (ILIM1) and dedicated current limit status pin, CSD1. The over-current threshold is programmable via the CS11 register (0x19, D4:0) between 500 mV and 3.2 V. This voltage refers to the voltage at the CSA1 pin, which is limited to 3.2 V maximum. Note that the over-current protection is not a current limiting function, but results in a fault flag and shutdown.

The CSA1 voltage is calculated as shown, where GAIN is the value set by the CS11 register:

$$V_{CSA1} = Iin \times R1 \times GAIN$$

When the CSA1 voltage rises to the set over-current threshold voltage, the CS1 latch-off delay timer will start (TLAT1). The delay time is programmable in the CS12 register (0x1A) between 0 and

330.75 ms. If the over-current condition is removed within the delay time, the timer is reset. If the over-current condition continues until the end of the delay timer, the over-current status bit (OCS, 0x04) will go high and the CS1 switch will turn off. The CSD1 pin goes high simultaneously to the OC1 bit. Writing 1 to clear the OCS register or cycling the power supply is required to reset the CS1 latch-off.

CS1 shutdown can be disabled using the SDCS1 bit in the EN2 register (0x06, D0). Disabling shutdown will allow the high current condition to continue while keeping the CSD1 and OCS bits high.

Although CS1 load switch can be enabled while the EN pin is low, the current sense is not active in this state. Exercise caution when turning on the load switch with the EN pin low.

If any of the current sense channels have latched off, they will remain off until the OCS bit is cleared, regardless of the EN pin state.

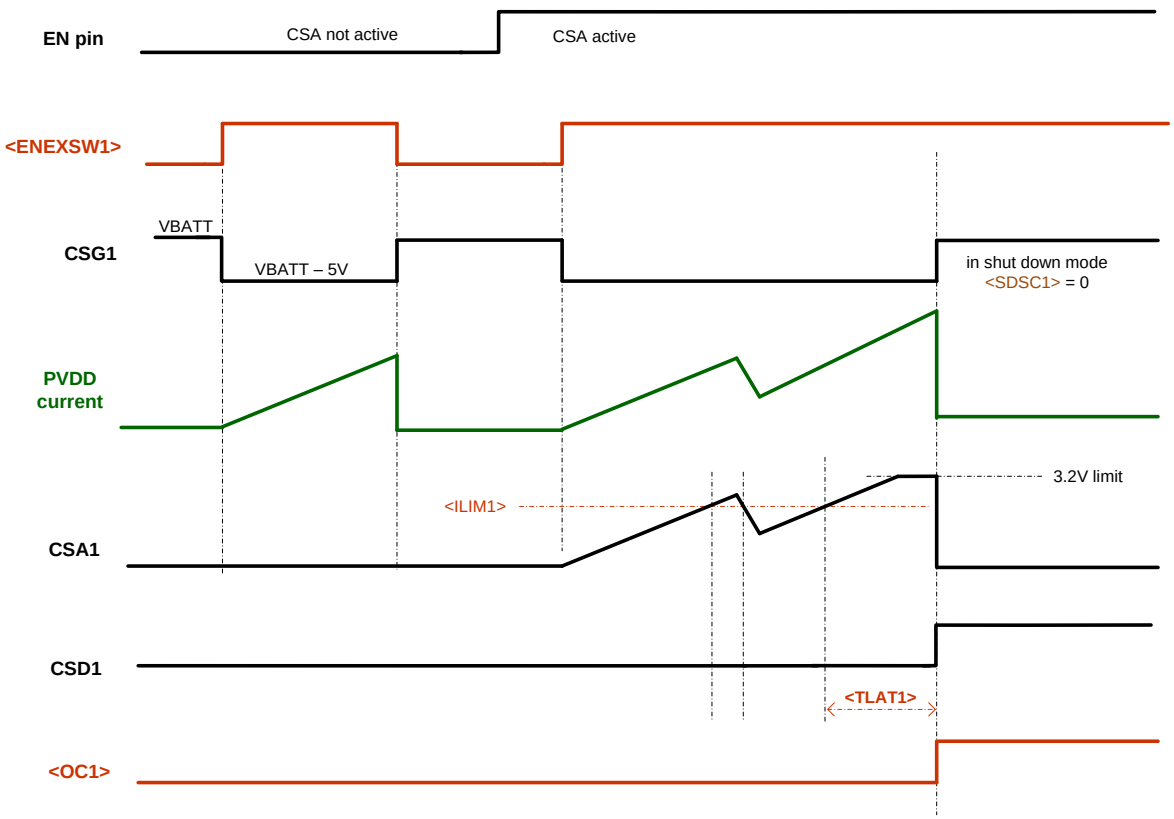


Figure 34: CS1 Functional Diagram

CS2 and CS3

CS2 and CS3 are very similar in operation to CS1, with one drive pin, CSG, and two sense pins, CSH and CSL. The current sense blocks are enabled and disabled independently from the EN pin via the EN2 register (0x06, D5:D4) and are not included in the sequencer function. As with CS1, the current sense and over-current functions are not active when the EN pin is low.

When enabled, the CSG pins will pull down the external PFET gate to turn on the external switch. The current sense gain is set with the CS21 and CS31 registers (0x1B and 0x1D) at either 20 V/V or 40 V/V. Sense resistor values of 25 mΩ to 50 mΩ are recommended to provide a 1:1 gain up to the CSD23 threshold.

CS2 and CS3 over-current and latch-off functions are identical to CS1, with programmable over-current thresholds, delay timers, over-current status bit, and latch-off disable option. However, CS2 and CS3 do not have a dedicated analog output pin for current monitoring. There is an open drain fault flag output pin, CSD23, which goes low when either of OC2 or OC3 goes high.. As with CS1, the over-current protection does not limit the current, rather it sets a fault flag and shuts down.

The CS2 pins are designed to handle input voltages as high as VBATT (as is CS1). However, the CS3 maximum voltage is 5.5 V for all three pins. Additionally, the CSL3 voltage should not be forced below CSG3. This condition will not occur in normal operation, but if CS3 is not used, connect CSH3 to ground to ensure that the circuit is off.

Both CSG2 and CSG3 are internally pulled up to their respective CSH pins, making them normally off even when battery power is removed.

9.11 External LDO Control

The DA6102 includes two circuit blocks designed to enable and monitor external regulators. This allows two additional rails to be easily included into the system's sequencing and fault detection management. The EN8 and EN7 bits in the EN1 register (0x05, D7:D6) control the EXEN1 and EXEN2 pins. These digital output pins are typically used to drive the enable pin of an external LDO or switching regulator. The external regulator can then be enabled and disabled directly by register write or by sequencer.

The EXS1 and EXS2 pins are voltage sense inputs for the externally regulated voltages. The EXS voltage is compared to a programmable reference level to indicate when the voltage is within range. The voltage thresholds are programmed at the EXLV register (0x0F), with each EXS pin having different available voltage ranges. The EXS status is reflected in the Power Good status bits in the PGS register (0x01, D4:5); when the EXS voltage is greater than the set threshold, its PGS bit is high. The EXS power good thresholds have a fixed hysteresis of 100 mV typical, regardless of the set value.

EX1 and EX2 will be disabled when a short circuit (SC or HDSRT) or over-voltage (OV) is detected on another channel.

9.12 PGOOD and FAULT Handling

Power Good Status (PGS)

Channels 1 through 4 and the external sense pins (EXS1 and EXS2) each have dedicated power good status bits in the PGS register (0x01, D5:D0). These bits are real time indicators of whether the voltage is within nominal range. For a switching channel the PGS bit shows high when the voltage is greater than the 90% of the target value and low when the voltage drops below 85% of nominal. The PGS bits for EXS1 and EXS2 have programmed thresholds. Each of these bits can be masked in the PGM register (0x14); when masked the PGS bit is held high. Unless masked, the PGS status bits are reflected in the PGOOD pin and PWGD bit (0x01, D7).

Power Good Pin (PGOOD)

The PGOOD pin can be configured as either an open drain or logic output, with a high state indicating that the DA6102 is in the Powered state (shown in Figure 29) with all enabled channels within range (PGS high). The PGOOD pin is active when the EN pin is high, the start-up sequence has ended, and the FAULT register (0x00) equals 0x00. PGOOD is masked during start-up for the duration of start-up delays (TSUPx: 0x07-0x0A) and soft-start times. Therefore, for channels not enabled using the sequencer, the TSUP delay time should be set to 0 to avoid unnecessary PGOOD blanking time. Any non-zero bit in the FAULT register will cause the PGOOD pin to go low. Simultaneously, a non-zero bit in the FAULT register will cause a shutdown of one or more channels. As such, the PGOOD pin can be understood as an indicator that all enabled channels are operating normally. To set the PGOOD pin to open drain mode, set the PGCME bit in the CTL register (0x22, D3) to 0. In open drain mode, a high state is indicated by high impedance at the PGOOD pin, allowing the node to be pulled up to an external logic rail via external resistor. Any pull-up voltage of 5 V of less can be used. In a low state the PGOOD pin is pulled to ground. When the EN pin is low, PGOOD is low in CMOS mode and high impedance in open drain mode.

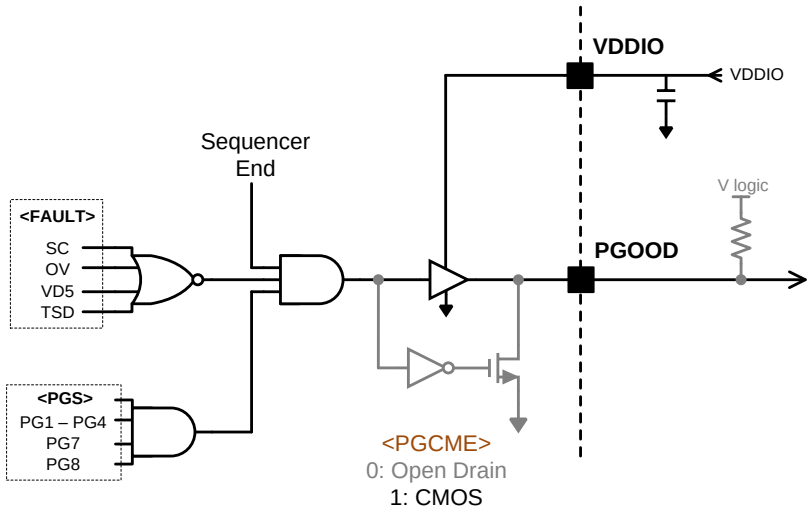


Figure 35: PGOOD Function

FAULT

The DA6102 FAULT register (0x00) indicates five types of faults: over-voltage, short circuit, hard short, TSD, and LDO1 under-voltage (VD5). Any of these fault indicators will cause an immediate shutdown of one or more channels. The OCS register (0x04) indicates over-current on the current sense channels and behaves exactly as the FAULT register, shutting down its respective current sense channel. A high FAULT or OCS bit can only be cleared writing 1 to that bit, or by cycling power. If HDSRT, OV, OCS, or SC fault bits are cleared while the EN pin is high, the affected channel will restart immediately.

OV, SC, and HDSRT faults will shut down one or more channels, while allowing the others to remain in regulation.

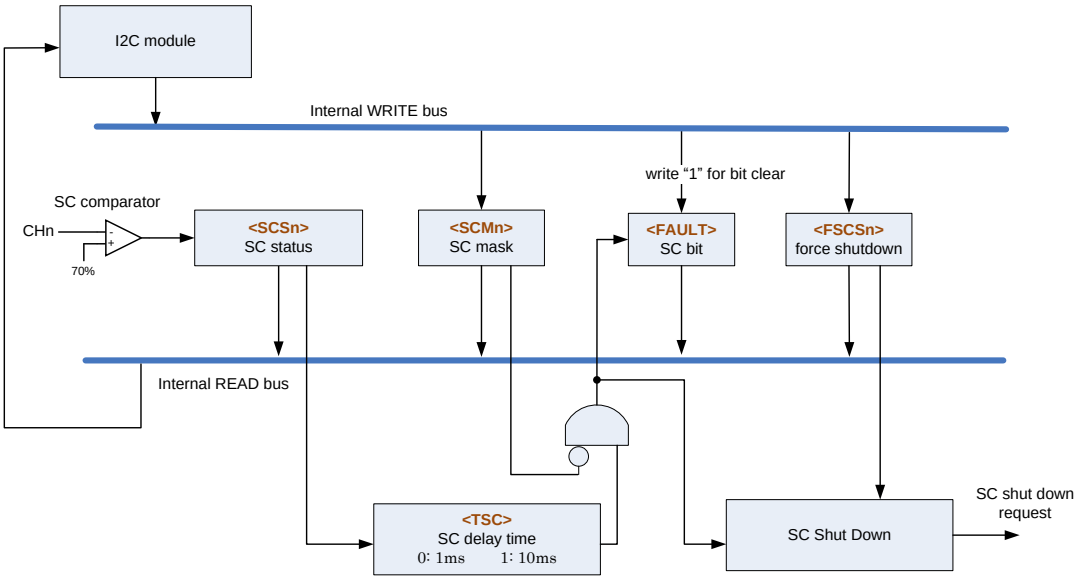


Figure 36: Short Circuit FAULT Logic

Figure 36 shows the logic for an SC fault. For OV faults, the functionality is identical. A summary of each channel and the type of fault protection available is shown in Table 12.

TSD and Global FAULTS

Thermal Shutdown (TSD) and VDR under-voltage (VD5) are considered global faults and will shut down all channels immediately. To clear these faults, the error must be removed (temperature reduced or VDR recovers) followed by clearing the FAULT bit.

The TSD function protects the PMIC from over-heating in extreme conditions or failure modes. Although the DA6102 is a highly efficient converter, a combination of heavy load and high ambient temperature can cause the device temperature to rise above the recommended maximum of 125°C. Ensure that the internal power dissipation (PD) in worst case operating conditions does not allow the junction temperature to rise above 125 °C. Junction temperature (T_J) is a function of PD, IC and PCB thermal resistance (θ_{JA}), and ambient temperature (T_A).

$$T_J = T_A + PD \times \theta_{JA}$$

T_J can be difficult to accurately calculate, primarily due to unknown PCB thermal characteristics. Note that the θ_{JA} specifications given in Table 8 are intended as benchmark values for typical PCB designs; the thermal performance of a real-world PCB may be better or worse.

Therefore, a better approach to determine junction temperature is to measure the temperature directly at the case top (T_C). The junction-to-case thermal resistance (θ_{JC}) of the WLCSP package is very low, approximately 0.1°C/W. Therefore, the measured case temperature will be within 1 degree of the junction temperature.

$$T_C = T_A + PD \times (\theta_{JA} - \theta_{JC})$$

and combining equations:

$$T_J = T_C + PD \times \theta_{JC} \cong T_C$$

Case temperature should be measured in the worst case operating conditions, including ambient temperature, to safeguard that device temperature is within the recommended range.

The TSD threshold is 150 °C typical with a hysteresis of 15 °C. When the junction temperature rises to the TSD threshold, all channels will shut down immediately with the exception of LDO1 and LDO2. In TSD, I²C communication is not interrupted and the TSD fault status can be read from the FAULT register. The DA6102 will not automatically restart after a TSD event. Even when the temperature is reduced, the TSD fault bit is not automatically cleared; it must be cleared by I²C write.

VD5 Fault

The VD5 fault function is an under-voltage protection for the drive voltage at the VDR pin. The DA6102 switching channels may not function properly if the drive voltage is excessively low. Faulty conditions such as Channel 1 current limit, combined with a low battery voltage may pull this voltage below the minimum required voltage. In order to prevent improper device operation, all channels will shut down if VDR drops below 3.5 V (typical). Similar to the TSD function, the PMIC will not restart automatically when the VDR voltage recovers to nominal; a VD5 fault condition must be cleared by I²C write. The VD5 fault protection is only active when the EN pin is high.

Table 12: Protection Features per Channel

<REG>	PROTECTION FEATURE options	CH1	CH2	CH3	CH4	EX1	EX2
	Current limit						
<PGS>	Power good status						
<PGM>	mask						
<SCS>	Short circuit status						
<FAULT> SC	Short circuit fault						
<SCM>	mask						
<TSC>	delay						
<FSCS>	shutdown by other CH					*	*
<FAULT> HDSRT	Hard Short fault						
<OVS>	Over voltage status						
<FAULT> OV	Over voltage fault						
<OVM>	mask						
<TOV>	delay						
<FOVS>	shutdown by other CH					*	*
<OCS>	Over current status						
	Over current latch off						
<SDCS>	mask						
<TLAT>	delay						
<FAULT> VD5	VDR under-voltage	GLOBAL					
<FAULT> TSD	Thermal Shut Down	GLOBAL					

<REG>	PROTECTION FEATURE options	LDSW1	LDSW2	CS1	CS2	CS3	LDO1	LDO2
	Current limit	**						
PGS>	Power good status							
<PGM>	mask							
<SCS>	Short circuit status							
<FAULT> SC	Short circuit fault							
<SCM>	mask							
<TSC>	delay							
<FSCS>	shutdown by other CH	CH1 only	CH3 only					
<OVS>	Over voltage status							
<FAULT>OV	Over voltage fault							
<OVM>	mask							
<TOV>	delay							
<FOVS>	shutdown by other CH	CH1 only	CH3 only					
<OCS>	Over current status							
	Over current latch off							
<SDCS>	mask							
<TLAT>	delay							
<FAULT> VD5	VDR under-voltage	GLOBAL					keep alive	
<FAULT> TSD	Thermal Shut Down	GLOBAL					keep alive	

* EX1/2 shutdown is not programmable

Blue indicates a shutdown condition

** LDSW1 current limit can be disabled

9.13 VDDIO and VCORE

The VDDIO and VCORE voltages are the digital supply rails for the DA6102. Each pin should be bypassed with a capacitor placed close to the pin, and grounded to the quiet GND pin. The VCORE voltage (1.5 V typical) is the supply and reference voltage for the internal digital circuits, as well as the EXCLK input. VCORE should be bypassed with a 4.7 µF or larger capacitor.

VDDIO is an external supply rail input, which can be supplied with any voltage between 1.5 V and 5.0 V as required to interface with external logic. I²C communication (SDA, SCL), the PGOOD pin in CMOS mode, and the EXEN and CSD pins are all referenced to the VDDIO level. A bypass capacitor of 1 µF or larger is recommended for VDDIO.

9.14 I²C Communication

The DA6102 includes an I²C-compatible 2-wire serial interface to access the internal registers. Through the I²C interface, the host processor can control each channel and current sense block and read back system status. The DA6102 will only operate as a slave device. For detailed information about each register, see Section 10.2.

The host processor provides the serial clock at the SCL pin. The DA6102 supports I²C clock frequencies up to 400 kHz. Register data is shifted into or out of the DA6102 at the SDA pin as requested by the host processor. All registers are initially configured from the OTP values, which are loaded during the initial power-up of the DA6102. All registers subsequently programmed by the I²C interface are cleared and reset to their default OTP values by Power-On Reset (POR).

Register addresses 0x01, 0x02, and 0x03 are read only; no acknowledge will be given to a write command at these addresses. Additionally, register 0x04 is a self-clearing register. Writing a 1 to any bit in address 0x04 will clear that bit to 0.

The I²C data pin, SDA, is open drain, allowing multiple devices to share a communication line. Both SCL and SDA must be externally pulled up to VDDIO with resistors in the range of 2 kΩ to 20 kΩ.

All data is transmitted across the 2-wire bus in 8-bit groups, with each bit transferred at the SCL rising edge. Each pulse of SCL clocks the SDA bit into the receivers shift register.

All transmissions begin with a START condition issued from the master while the bus is in an IDLE state (the bus is free). The START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state. Alternately, a STOP condition is indicated by a low to high transition on the SDA line while the SCL line is in the high state, see Figure 37.

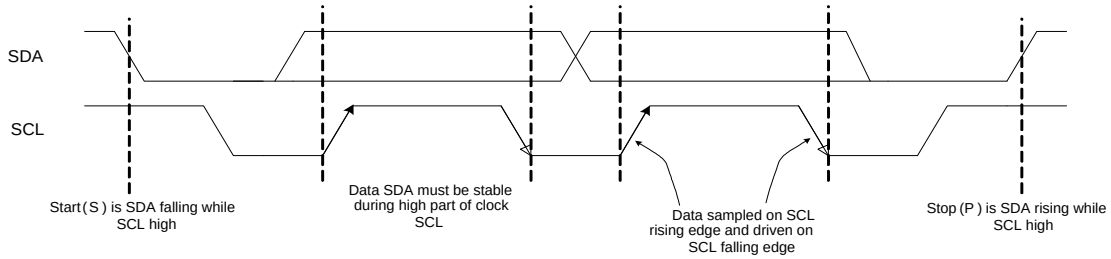


Figure 37: I²C Start (S) and Stop (P)

The I²C interface uses a 2-byte serial protocol containing one byte for address and one byte for data. Data and address are transferred with MSB transmitted first for both read and write operations.

The DA6102 monitors the serial bus for a valid SLAVE address whenever the interface is enabled. When it receives its own slave address, the DA6102 immediately gives and acknowledge signal to the host by pulling the SDA line low during the following clock cycle. A NotAcknowledge signal is given by a logic 1, not pulling down the SDA line.

A single byte WRITE is shown in Figure 38. Here the slave address is followed by a WRITE bit (low), the register address, and the WRITE data. Finally, the transaction is terminated with a STOP.

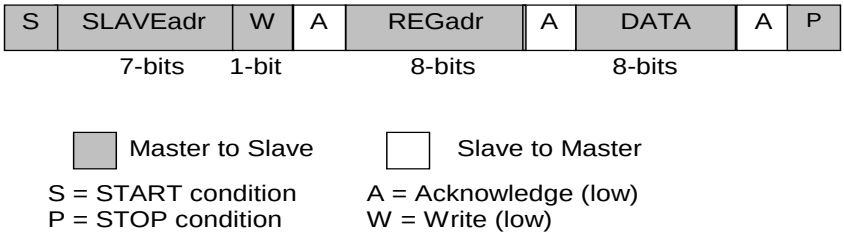


Figure 38: Single Write Command

The DA6102 also supports multiple byte writes, as shown in Figure 39. By not sending the STOP command, data is written to consecutive addresses.

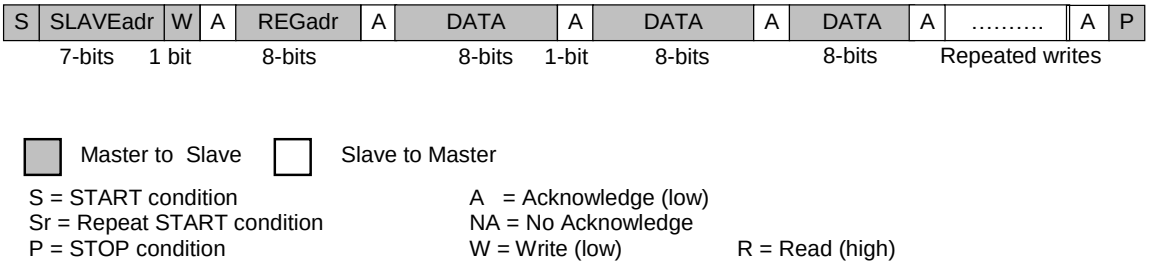


Figure 39: Consecutive Write Command

The data READ protocol is somewhat different in that a READ does not have a register address immediately preceding it. The data returned from a basic READ command begins from address 00. To READ from a specific address, the register address is given by using a write command followed by a Repeated START. Both methods of commanding a single byte READ are shown in Figure 40. Either a Repeated START or a START is followed by the slave address and a READ bit. After the READ data is returned to the host, the host then responds with a NotAcknowledge and a STOP. Note that if a WRITE command is aborted by a STOP followed by a START, rather than a repeated START, the subsequent READ address will reset to 00.

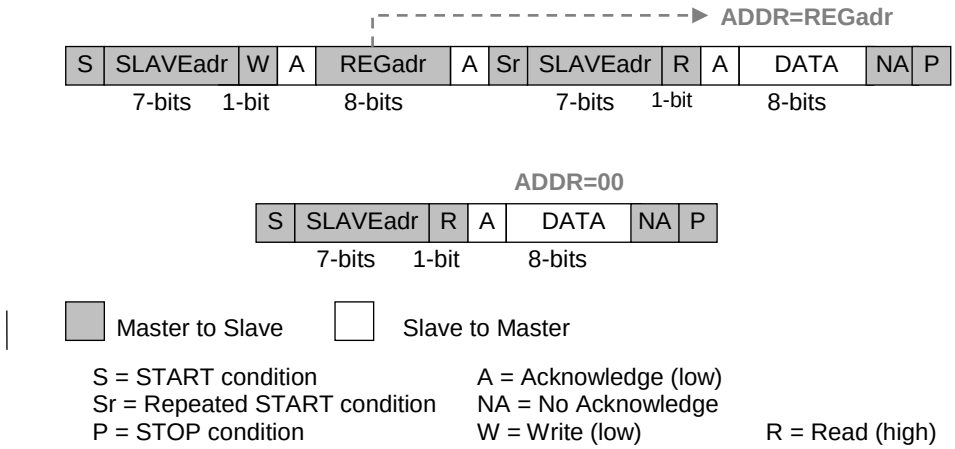


Figure 40: Single Read Command (Two Methods)

The DA6102 also supports a multiple byte READ protocol. If the host responds to the returned data with an ACKnowledge (ACK) rather than NotACKnowledge (NACK) and STOP, data will be read from sequential addresses, as shown in Figure 41. A simple multiple READ command always starts from address 00, and sequential addresses will be READ until a NACK and STOP command is given. If a READ address is given with a WRITE and repeated START, consecutive addresses are read from the WRITE address.

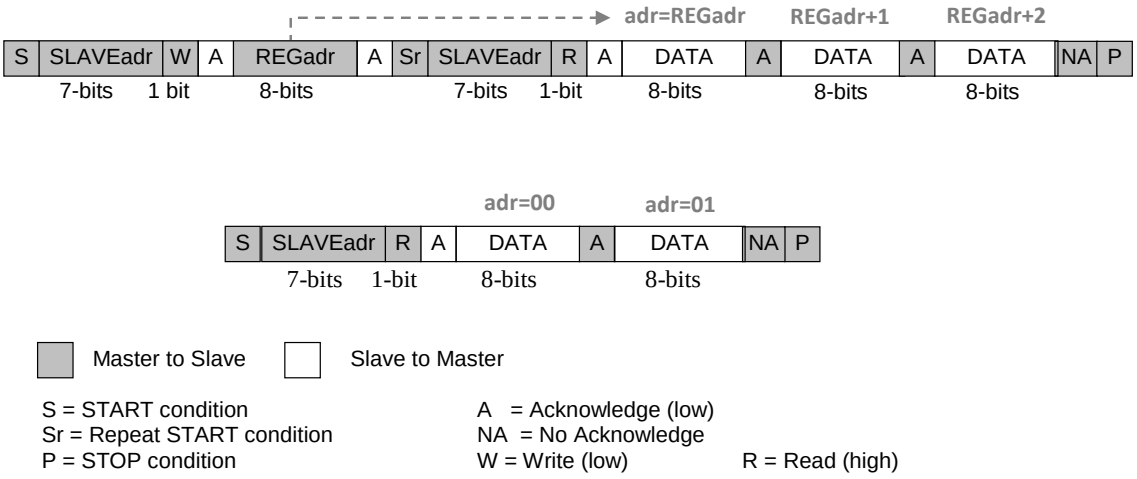


Figure 41: Sequential Address Multiple Read Command

9.15 PCB Layout Guidelines

Following a few basic PCB design practices will ensure proper operation and optimal thermal performance from the DA6102.

The first priority is to reduce and isolate high frequency switching noise so that it does not disturb sensitive nodes, including adjacent channels. For buck switching regulators, the primary sources of noise are at the input capacitor ground and supply side. The input capacitor should be connected as close as possible to the PG and VIN pins of each channel. This reduces the parasitic inductance responsible for much of the voltage spikes in switching. The current carrying traces (VIN, PG, VOUT) should route directly to the pads of all capacitors, not through vias or separate traces. This applies to both input and output capacitors and is good practice in general. A simplified routing example is shown in Figure 42.

This applies somewhat differently to Channel 3, where input caps should be place close to the external FETs rather than the DA6102 pins. Additionally, the PG3 pin should have a low impedance connection to the ground plane directly and does not need to be connected to the external FET ground directly.

The second largest noise source is the LX node. Although the current here is not switching, the fast voltage swings can introduce noise through capacitive coupling. To reduce this, use the smallest area possible for the LX node, while keeping in mind the current handling requirements.

The VDR capacitor supplies the instantaneous current required to drive the power FETs for each switching channel. To prevent excessive voltage drop at the VDR pin, the capacitor must be placed close to the IC with a wide trace and good connection to the PG plane.

All sensitive nodes, such as FB, CSH, and CSL, should be routed away from the input capacitors and inductors. Additionally it is recommended to route them on the bottom side of the PCB where they are shielded from switching noise.

The I^2C signal traces, SDA and SCL, must be shielded and routed away from switching noise as much as possible. Specifically, take care that the I^2C lines are noise isolated from Channel 1 as these pins are adjacent on the IC.

To create a good shield, one mid-layer should be flooded with copper and connected as a common ground at the output capacitors and GND pin of the IC. Use this common ground as a connection for all noise sensitive and low current signals. It is important that the common ground is not connected to power ground, except at Vout, so that no switching currents will flow in this plane.

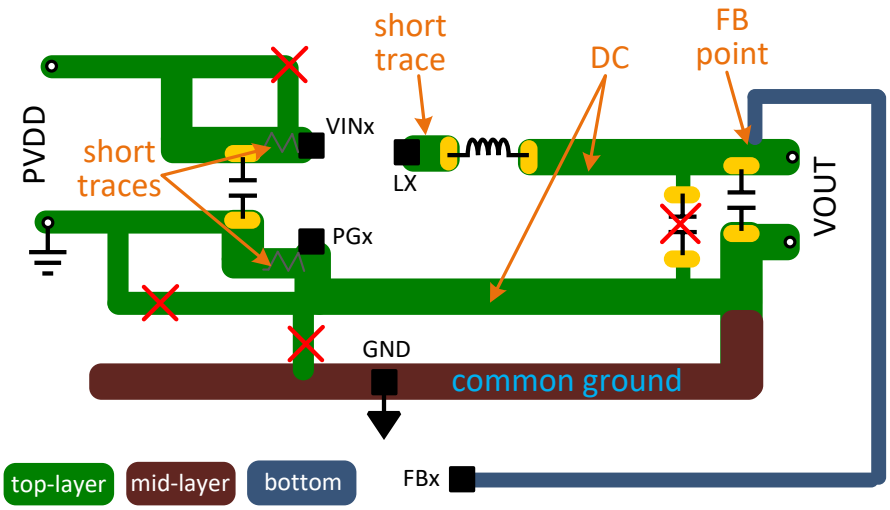


Figure 42: PCB Layout Guidelines

Finally, the PCB is an important element in the thermal performance of the IC. Wherever possible, flood all PCB layers with copper to maximize heat spreading. Route the VIN, LX, and PG connections, which have the highest power dissipation, on the top layer. This minimizes both electrical and thermal impedance. Be sure that all high current traces, both DC and switching, have sufficient trace width. The minimum recommended width is 0.75 mm/A for 1oz copper thickness, and wider is better.

10 Register Definitions

The I²C Slave Address can be set by OTP with values from 0x01 to 0x7F.

The OTP-80 Slave Address is 0x2F

10.1 Register Map

Table 13: Register Map

All un-shaded registers are programmable by OTP. The OTP-80 values apply to the -80 version only.

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Reset
											OTP-80
0x00	FAULT	RW	HDSRT	RCHK			TSD	VD5	OV	SC	0x00
0x01	PGS	R	PWGD		PG8	PG7	PG4	PG3	PG2	PG1	0x80
0x02	SCS	R				SC5	SC4	SC3	SC2	SC1	0x00
0x03	OVS	R					OV4	OV3	OV2	OV1	0x00
0x04	OCS	RW						OC3	OC2	OC1	0x00
0x05	EN1	RW	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	0xE5
0x06	EN2	RW			ENEXSW3	ENEXSW2	ENEXSW1	SDCS3	SDCS2	SDCS1	0x00
0x07	TSUP12	RW			TSUP2[2:0]			TSUP1[2:0]			0x00
0x08	TSUP34	RW			TSUP4[2:0]			TSUP3[2:0]			0x00
0x09	TSUP56	RW			TSUP6[2:0]			TSUP5[2:0]			0x10
0x0A	TSUP78	RW			TSUP8[2:0]			TSUP7[2:0]			0x01
0x0B	DVS1	RW					DVS1[3:0]				0x04
0x0C	DVS2	RW				DVS2[4:0]					0x06
0x0D	DVS3	RW					DVS3[3:0]				0x06
0x0E	DVS4	RW				DVS4[4:0]					0x10
0x0F	EXLV	RW	EXLV2[3:0]				EXLV1[3:0]				0x00
0x10	TSS	RW	TSS4[1:0]		TSS3[1:0]		TSS2[1:0]		TSS1[1:0]		0x00
0x11	TSEQ	RW					STP_SEQ	TDVS	TOV	TSC	0x00
0x12	FREQ	RW	FREQ4[1:0]		FREQ3[1:0]		FREQ2[1:0]		FREQ1[1:0]		0x8A
0x13	CLKS	RW				CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	EXCLK	0x09
0x14	PGM	RW			PGM8	PGM7	PGM4	PGM3	PGM2	PGM1	0x3A
0x15	OVM	RW	FOVS4	FOVS3	FOVS2	FOVS1	OVM4	OVM3	OVM2	OVM1	0x00
0x16	SCM	RW				SCM5	SCM4	SCM3	SCM2	SCM1	0x00

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Reset
											OTP-80
0x17	FSCS	RW					FSCS4	FSCS3	FSCS2	FSCS1	0x0F
0x18	DISC	RW				DISC5	NDISC4	NDISC3	NDISC2	NDISC1	0x00
0x19	CS11	RW	GAIN1[1:0]			ILIM1[4:0]					0x0C
0x1A	CS12	RW			TLAT1[5:0]						0x04
0x1B	CS21	RW		GAIN2		ILIM2[4:0]					0x1D
0x1C	CS22	RW			TLAT2[5:0]						0x05
0x1D	CS31	RW		GAIN3		ILIM3[4:0]					0x50
0x1E	CS32	RW			TLAT3[5:0]						0x05
0x1F	-	RW									0x00
0x20	SLP	RW	SLP_VO4[1:0]		SLP_VO3[1:0]		SLP_VO2[1:0]		SLP_VO1[1:0]		0x04
0x21	FZ23_EFET	RW		CMP_VO3[1:0]		EXTFET					0x40
0x22	CTL	RW		LDSW1F	LDO3V[1:0]		PGCME	PSM4	PSM3	PSM2	0x07
0x23	SRST	RW	SRST[7:0]								0x00
0x30	HDSRT	R	NHST4	PHST4	NHST3	PHST3	NHST2	PHST2	NHST1	PHST1	0x00
0x31	BB_OPT	RW					BST_VTH [1:0]		PSM1	BKONLY	0x02
0x32	CMP12	RW	EA_CC2 [1:0]		EA_HFGAIN2 [1:0]		EA_CC1 [1:0]		EA_HFGAIN1 [1:0]		0x00
0x33	CMP3	RW					EA_CC3 [1:0]		EA_HFGAIN3 [1:0]		0x00
0x34	CMP4	RW	EA_CC4 [1:0]		EA_HFGAIN4 [1:0]						0x00

10.2 Register Details

Register Table 1: Fault Flag (FAULT <0x00>)

Bit	Mode	Symbol	Description	Reset
D7	R/W	HDSRT	1: Hard short error	0
D6	R/W	RCHK	1: Reset check Error	0
D3	R/W	TSD	1: Thermal Shutdown	0
D2	R/W	VD5	1: VDR under-voltage	0
D1	R/W	OV	1: Over-voltage status (OVS register)	0
D0	R/W	SC	1: Short circuit status (SCS register)	0

Note 1 0 indicates no fault condition.

Register Table 2: Power Good Status (PGS <0x01>)

Bit	Mode	Symbol	Description	Reset
D7	R	PWGD	PGOOD pin state 0: logic low or low impedance, not good 1: logic high or high impedance, power good	1
D5	R	PG8	External LDO2 Power Good status, 1 = good	0
D4	R	PG7	External LDO1 Power Good status, 1 = good	0
D3	R	PG4	CH4 Power Good status, 1 = good	0
D2	R	PG3	CH3 Power Good status, 1 = good	0
D1	R	PG2	CH2 Power Good status, 1 = good	0
D0	R	PG1	CH1 Power Good status, 1 = good	0

Note 1 PGx bits [D5:D0] are masked during the soft-start ramp. PWGD bit [D7] is high when EN pin is low

Register Table 3: Short Circuit Status (SCS <0x02>)

Bit	Mode	Symbol	Description	Reset
D4	R	SC5	Short circuit status of LDSW1, 1 = short circuit	0
D3	R	SC4	Short circuit status of CH4, 1 = short circuit	0
D2	R	SC3	Short circuit status of CH3, 1 = short circuit	0
D1	R	SC2	Short circuit status of CH2, 1 = short circuit	0
D0	R	SC1	Short circuit status of CH1, 1 = short circuit	0

Note 1 SCx bits [D4:D0] are always active.

Register Table 4: Over-Voltage Status (OVS <0x03>)

Bit	Mode	Symbol	Description	Reset
D3	R	OV4	Over-Voltage Status of CH4, 1 = Over-Voltage	0
D2	R	OV3	Over-Voltage Status of CH3, 1 = Over-Voltage	0
D1	R	OV2	Over-Voltage Status of CH2, 1 = Over-Voltage	0
D0	R	OV1	Over-Voltage Status of CH1, 1 = Over-Voltage	0

Note 1 OVx bits [D3:D0] are always active.

Register Table 5: Load Switch Over-Current Status (OCS <0x04>)

Bit	Mode	Symbol	Description	Reset
D2	R/W	OC3	Over-Current status of CS3, 1 = Over-Current	0
D1	R/W	OC2	Over-Current status of CS2, 1 = Over-Current	0
D0	R/W	OC1	Over-Current status of CS1, 1 = Over-Current	0

Note 1 Reset by writing <1>

Note 2 OCx bits go high after the TLATx time ends

Note 3 OCx bits are masked when SDCSx = 1

Register Table 6: Enable 1 (EN1 <0x05>)

Bit	Mode	Symbol	Description	OTP-80
D7	R/W	EN8	Enable External LDO2 0: Shutdown 1: Enable	1
D6	R/W	EN7	Enable External LDO1 0: Shutdown 1: Enable	1
D5	R/W	EN6	Enable LDSW2 input 0: Shutdown 1: Enable	1
D4	R/W	EN5	Enable LDSW1 0: Shutdown 1: Enable	0
D3	R/W	EN4	Enable CH4 0: Shutdown 1: Enable	0
D2	R/W	EN3	Enable CH3 0: Shutdown 1: Enable	1
D1	R/W	EN2	Enable CH2 0: Shutdown 1: Enable	0
D0	R/W	EN1	Enable CH1 0: Shutdown 1: Enable	1

Note 1 Channels set to <1> will start-up in sequencer mode. After the start-up sequence is complete, ENx bits can be used to enable or disable individual channels.

Register Table 7: Enable 2 (EN2 <0x06>)

Bit	Mode	Symbol	Description	OTP-80
D5	R/W	ENEXSW3	Enable CSG3 0: Shutdown 1: Enable	0
D4	R/W	ENEXSW2	Enable CSG2 0: Shutdown 1: Enable	0
D3	R/W	ENEXSW1	Enable CSG1 0: Shutdown 1: Enable	0
D2	R/W	SDCS3	CS3 Fault override 0: Shutdown mode 1: Stay on (ignore faults)	0
D1	R/W	SDCS2	CS2 Fault override 0: Shutdown mode 1: Stay on (ignore faults)	0
D0	R/W	SDCS1	CS1 Fault override 0: Shutdown mode 1: Stay on (ignore faults)	0

Note 1 SDCSx bits also disable the OC status bits (OCS, 0x04)

Register Table 8: Start-up Delay Time Control 1/2 (TSUP12 <0x07>)

Bit	Mode	Symbol	Description	OTP-80
D[5:3]	R/W	TSUP2 [2:0]	CH2 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000
D[2:0]	R/W	TSUP1 [2:0]	CH1 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000

Note 1 It is recommended to set TSUPx to 000 if the channel is not enabled by sequencer

Register Table 9: Start-up Delay Time Control 3/4 (TSUP34 <0x08>)

Bit	Mode	Symbol	Description	OTP-80
D[5:3]	R/W	TSUP4 [2:0]	CH4 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000
D[2:0]	R/W	TSUP3 [2:0]	CH3 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000

Note 1 It is recommended to set TSUPx to 000 if the channel is not enabled by sequencer

Register Table 10: Start-up Delay Time Control 5/6 (TSUP56 <0x09>)

Bit	Mode	Symbol	Description	OTP-80
D[5:3]	R/W	TSUP6 [2:0]	LDSW2 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	010
D[2:0]	R/W	TSUP5 [2:0]	LDSW1 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000

Note 1 It is recommended to set TSUPx to 000 if the channel is not enabled by sequencer

Register Table 11: Start-up Delay Time Control 7/8 (TSUP78 <0x0A>)

Bit	Mode	Symbol	Description	OTP-80
D[5:3]	R/W	TSUP8 [2:0]	External LDO2 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	000
D[2:0]	R/W	TSUP7 [2:0]	External LDO1 start-up delay time: 000: 0 ms 001: 2.1 ms 010: 3.15 ms 011: 5.25 ms 100: 6.3 ms 101: 8.4 ms 110: 16.8 ms 111: 33.6 ms	001

Note 1 It is recommended to set TSUPx to 000 if the channel is not enabled by sequencer

Register Table 12: Dynamic Voltage Scaling Channel1 (DVS1 <0x0B>)

Bit	Mode	Symbol	Description	OTP-80
D[3:0]	R/W	DVS1 [3:0]	CH1 Output Voltage Setting (V): 0000 5.10 0001 5.15 0010 5.20 0011 5.25 0100 5.30 0101 5.35 0110 5.40 0111 5.45 1000 5.50 1001 5.55 1010 5.60 1011 5.65 1100 5.70 1101 5.75 1110 5.80 1111 Reserved	0100 (5.3 V)

Register Table 13: Dynamic Voltage Scaling Channel2 (DVS2 <0x0C>)

Bit	Mode	Symbol	Description	OTP-80
D[4:0]	R/W	DVS2 [4:0]	CH2 Output Voltage Setting (V): 00000 3.00 00001 3.05 00010 3.10 00011 3.15 00100 3.20 00101 3.25 00110 3.30 00111 3.35 01000 3.40 01001 3.45 01010 3.50 <01011 – 10100> 50mV steps 10101 4.05 10110 4.10 10111 4.15 11000 4.20 11001 4.25 11010 4.30 11011 4.35 11100 4.40 11101 4.45 11110 4.50 11111 4.55	00110 (3.30 V)

Register Table 14: Dynamic Voltage Scaling Channel3 (DVS3 <0x0D>)

Bit	Mode	Symbol	Description	OTP-80
D[3:0]	R/W	DVS3 [3:0]	CH3 Output Voltage Setting (V): 0000 3.00 0001 3.05 0010 3.10 0011 3.15 0100 3.20 0101 3.25 0110 3.30 0111 3.35 1000 3.40 1001 3.45 1010 3.50 1011 3.55 1100 3.60 1101 3.65 1110 3.70 1111 3.75	0110 (3.30 V)

Register Table 15: Dynamic Voltage Scaling Channel4 (DVS4 <0x0E>)

Bit	Mode	Symbol	Description	OTP-80
D[4:0]	R/W	DVS4 [4:0]	CH4 Output Voltage Setting (V): 00000 3.20 00001 3.25 00010 3.30 00011 3.35 00100 3.40 00101 3.45 00110 3.50 00111 3.55 01000 3.60 01001 3.65 01010 3.70 01011 3.75 01100 3.80 01101 3.85 01110 3.90 01111 3.95 10000 4.00 10001 4.05 10010 4.10 10011 4.15 10100 4.20 <10101 – 11111> Reserved	10000 (4.0 V)

Register Table 16: External LDO Power Good Voltage (EXLV <0x0F>)

Bit	Mode	Symbol	Description	OTP-80
D[7:4]	R/W	EXLV2 [3:0]	External LDO2 PGOOD voltage (V): 0000 2.1 0001 2.2 0010 2.3 0011 2.4 0100 2.5 0101 2.6 0110 2.7 0111 2.8 1000 2.9 1001 3.0 1010 3.1 1011 3.2 1100 3.3 1101 3.4 1110 3.5 1111 3.6	0000

Bit	Mode	Symbol	Description	OTP-80
D[3:0]	R/W	EXLV1 [3:0]	External LDO1 PGOOD voltage (V): 0000 0.8 0001 0.9 0010 1.0 0011 1.1 0100 1.2 0101 1.3 0110 1.4 0111 1.5 1000 1.6 1001 1.7 1010 1.8 1011 1.9 1100 2.0 1101 2.1 1110 2.2 1111 2.3	0000

Note 1 EXLV1 and EXLV2 set the rising threshold for power good status (<PGS> D4:D5).

Register Table 17: Soft-start (TSS <0x10>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	TSS4 [1:0]	CH4 Soft-start time: 00 1 ms 01 2 ms 10 4 ms 11 10 ms	00
D[5:4]	R/W	TSS3 [1:0]	CH3 Soft-start time: 00 1 ms 01 2 ms 10 4 ms 11 10 ms	00
D[3:2]	R/W	TSS2 [1:0]	CH2 Soft-start time: 00 1 ms 01 2 ms 10 4 ms 11 10 ms	00
D[1:0]	R/W	TSS1 [1:0]	CH1 Soft-start time: 00 1 ms 01 2 ms 10 4 ms 11 10 ms	00

Register Table 18: Timing and Sequence (TSEQ <0x11>)

Bit	Mode	Symbol	Description	OTP-80
D3	R/W	STP_SEQ	Shutdown sequence : 0: Shutdown with reverse start-up sequence 1: Shutdown all channels simultaneously	0
D2	R/W	TDVS	DVS step time (us/step): 0: 52.5 1: 105	0
D1	R/W	TOV	Over-Voltage shutdown delay time: 0: 10.5 ms 1: 0 ms	0
D0	R/W	TSC	Short circuit shutdown delay time: 0: 10.5 ms 1: 1 ms	0

Note 1 TOV and TSC prevent shutdown due to momentary voltage transients such as during DVS. TOV and TSC do not affect the OVS and SCS status bits.

Register Table 19: Switching Frequency (FREQ <0x12>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	FREQ4[1:0]	CH4 Switching frequency: 00: 1.0 MHz 01: 1.5 MHz 10: 2.0 MHz 11: 3.0 MHz	10 (2 MHz)
D[5:4]	R/W	FREQ3[1:0]	CH3 Switching frequency: 00: 1.0 MHz 01: 1.5 MHz 10: 2.0 MHz 11: 3.0 MHz	00 (1 MHz)
D[3:2]	R/W	FREQ2[1:0]	CH2 Switching frequency: 00: 1.0 MHz 01: 1.5 MHz 10: 2.0 MHz 11: 3.0 MHz	10 (2 MHz)
D[1:0]	R/W	FREQ1[1:0]	CH1 Switching frequency: 00: 1.0 MHz 01: 1.5 MHz 10: 2.0 MHz 11: 3.0 MHz	10 (2 MHz)

Register Table 20: Clock Select (CLKS <0x13>)

Bit	Mode	Symbol	Description	OTP-80
D4	R/W	CLKDIV4	CH4 Clock divider: 0: 1 1: 0.5	0
D3	R/W	CLKDIV3	CH3 Clock divider: 0: 1 1: 0.5	1
D2	R/W	CLKDIV2	CH2 Clock divider: 0: 1 1: 0.5	0
D1	R/W	CLKDIV1	CH1 Clock divider: 0: 1 1: 0.5	0
D0	R/W	EXCLK	External clock select: 0: Internal clock 1: External clock	1

Note 1 Internal clock is enabled if the external clock is out of range, regardless of EXCLK register state.

Register Table 21: Power Good Mask (PGM <0x14>)

Bit	Mode	Symbol	Description	OTP-80
D5	R/W	PGM8	External LDO2 PGOOD mask 0: not masked 1: masked	1
D4	R/W	PGM7	External LDO1 PGOOD mask 0: not masked 1: masked	1
D3	R/W	PGM4	CH4 PGOOD mask 0: not masked 1: masked	1
D2	R/W	PGM3	CH3 PGOOD mask 0: not masked 1: masked	0
D1	R/W	PGM2	CH2 PGOOD mask 0: not masked 1: masked	1
D0	R/W	PGM1	CH1 PGOOD mask 0: not masked 1: masked	0

Note 1 PGM register bits mask the PGx (0x01) status registers, forcing PGx to always high state.

Register Table 22: Over-Voltage Mask (OVM <0x15>)

Bit	Mode	Symbol	Description	OTP-80
D7	R/W	FOVS4	Shutdown CH4 if OV detected on another channel 0: no shutdown 1: Shutdown	0
D6	R/W	FOVS3	Shutdown CH3 if OV detected on another channel 0: no shutdown 1: Shutdown	0
D5	R/W	FOVS2	Shutdown CH2 if OV detected on another channel 0: no shutdown 1: Shutdown	0
D4	R/W	FOVS1	Shutdown CH1 if OV detected on another channel 0: no shutdown 1: Shutdown	0
D3	R/W	OVM4	CH4 OV shutdown 0: not masked 1: masked	0
D2	R/W	OVM3	CH3 OV shutdown 0: not masked 1: masked	0
D1	R/W	OVM2	CH2 OV shutdown 0: not masked 1: masked	0
D0	R/W	OVM1	CH1 OV shutdown 0: not masked 1: masked	0

Note 1 OVMx register settings mask the OV FAULT register bit and OV Shutdown. They do not affect the OVS status registers (0x03).

Register Table 23: Short Circuit Mask (SCM <0x16>)

Bit	Mode	Symbol	Description	OTP-80
D4	R/W	SCM5	LDSW1 SC shutdown 0: not masked 1: masked	0
D3	R/W	SCM4	CH4 SC shutdown 0: not masked 1: masked	0
D2	R/W	SCM3	CH3 SC shutdown 0: not masked 1: masked	0

Bit	Mode	Symbol	Description	OTP-80
D1	R/W	SCM2	CH2 SC shutdown 0: not masked 1: masked	0
D0	R/W	SCM1	CH1 SC shutdown 0: not masked 1: masked	0

Note 1 SCM register settings mask the SC FAULT register bit and SC shutdown. They do not affect SC detection or SCS status registers.

Register Table 24: Force Short Circuit Stop (FSCS <0x17>)

Bit	Mode	Symbol	Description	OTP-80
D3	R/W	FSCS4	Shutdown CH4 if SC detected on another channel 0: no shutdown 1: Shutdown	1
D2	R/W	FSCS3	Shutdown CH3 if SC detected on another channel 0: no shutdown 1: Shutdown	1
D1	R/W	FSCS2	Shutdown CH2 if SC detected on another channel 0: no shutdown 1: Shutdown	1
D0	R/W	FSCS1	Shutdown CH1 if SC detected on another channel 0: no shutdown 1: Shutdown	1

Register Table 25: Output Discharge (DISC <0x18>)

Bit	Mode	Symbol	Description	OTP-80
D4	R/W	DISC5	LDSW1 output discharge at shutdown 0: no discharge 1: discharge enabled	0
D3	R/W	NDISC4	CH4 output discharge at shutdown 0: discharge enabled 1: no discharge	0
D2	R/W	NDISC3	CH3 output discharge at shutdown 0: discharge enabled 1: no discharge	0
D1	R/W	NDISC2	CH2 output discharge at shutdown 0: discharge enabled 1: no discharge	0
D0	R/W	NDISC1	CH1 output discharge at shutdown 0: discharge enabled 1: no discharge	0

Note 1 LDSW1 is not discharged when the EN pin is low, regardless of DISC5 setting.

Register Table 26: Current Sense Control 1 (CS11 <0x19>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	GAIN1[1:0]	CS1 current sense gain: 00: 20 01: 40 10: 100 11: 100	00
D[4:0]	R/W	ILIM1[4:0]	CS1 current limit threshold (V): 00000 - 00100 0.5 00101 0.6 00110 0.7 00111 0.8 01000 0.9 01001 1.0 01010 1.1 01011 1.2 01100 1.3 01101 1.4 01110 1.5 01111 1.6 10000 1.7 10001 1.8 10010 1.9 10011 2.0 10100 2.1 10101 2.2 10110 2.3 10111 2.4 11000 2.5 11001 2.6 11010 2.7 11011 2.8 11100 2.9 11101 3.0 11110 3.1 11111 3.2	01100 (1.3 V)

Register Table 27: Current Sense Time 1 (CS12 <0x1A>)

Bit	Mode	Symbol	Description	OTP-80
D[5:0]	R/W	TLAT1[5:0]	CS1 current limit delay time (ms): 000000 0 000001 5.25 000010 10.5 000011 15.75 000100 21 000101 26.25 000110 31.5 000111 36.75 001000 42 001001 - 111010 5.25 ms per step 111011 309.75 111100 315 111101 320.25 111110 325.5 111111 330.75	000100 (21 ms)

Register Table 28: Current Sense Control 2 (CS21 <0x1B>)

Bit	Mode	Symbol	Description	OTP-80
D6	R/W	GAIN2	CS2 current sense gain: 0: 20 1: 40	0
D[4:0]	R/W	ILIM2[4:0]	CS2 current limit threshold (V): 00000 - 00100 0.5 00101 0.6 00110 0.7 00111 0.8 01000 0.9 01001 1.0 01010 1.1 01011 1.2 01100 1.3 01101 1.4 01110 1.5 01111 1.6 10000 1.7 10001 1.8 10010 1.9 10011 2.0 10100 2.1 10101 2.2 10110 2.3 10111 2.4 11000 2.5 11001 2.6 11010 2.7 11011 2.8 11100 2.9 11101 3.0 11110 3.1 11111 3.2	11101 (3.0 V)

Register Table 29: Current Sense Time 2 (CS22 <0x1C>)

Bit	Mode	Symbol	Description	OTP-80
D[5:0]	R/W	TLAT2[5:0]	CS2 current limit delay time (ms): 000000 0 000001 1.05 000010 2.1 000011 3.15 000100 4.2 000101 5.25 000110 6.3 000111 7.35 001000 8.4 001001 - 111010 1.05 ms per step 111011 61.95 111100 63 111101 64.05 111110 65.1 111111 66.15	000101 (5.25 ms)

Register Table 30: Current Sense Control 3 (CS31 <0x1D>)

Bit	Mode	Symbol	Description	OTP-80
D6	R/W	GAIN3	CS3 current sense gain: 0: 20 1: 40	1
D[4:0]	R/W	ILIM3[4:0]	CS3 current limit threshold (V): 00000 - 00100 0.5 00101 0.6 00110 0.7 00111 0.8 01000 0.9 01001 1.0 01010 1.1 01011 1.2 01100 1.3 01101 1.4 01110 1.5 01111 1.6 10000 1.7 10001 1.8 10010 1.9 10011 2.0 10100 2.1 10101 2.2 10110 2.3 10111 2.4 11000 2.5 11001 2.6 11010 2.7 11011 2.8 11100 2.9 11101 3.0 11110 3.1 11111 3.2	10000 (1.7 V)

Register Table 31: Current Sense Time 3 (CS32 <0x1E>)

Bit	Mode	Symbol	Description	OTP-80
D[5:0]	R/W	TLAT3[5:0]	CS3 current limit delay time (ms): 000000 0 000001 1.05 000010 2.1 000011 3.15 000100 4.2 000101 5.25 000110 6.3 000111 7.35 001000 8.4 001001 - 111010 1.05 ms per step 111011 61.95 111100 63 111101 64.05 111110 65.1 111111 66.15	000101 (5.25 ms)

Register Table 32: Not Used <0x1F>

Bit	Mode	Symbol	Description	OTP-80
D[7:0]	R/W		Not Used	00

Register Table 33: Slope Adjust Control (SLP <0x20>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	SLP_VO4 [1:0]	CH4 slope compensation 00: 4.7 µH range 01: 2.2 µH range 10: 10 µH range 11: 6.8 µH range	00
D[5:4]	R/W	SLP_VO3 [1:0]	CH3 PWM ramp 00: VIN3/14 01: VIN3/7 10: VIN3/28 11: VIN3/17.5	00
D[3:2]	R/W	SLP_VO2 [1:0]	CH2 slope compensation 00: 2.2 µH range 01: 1.0 µH range 10: 4.7 µH range 11: 3.3 µH range	01

Bit	Mode	Symbol	Description	OTP-80
D[1:0]	R/W	SLP_VO1 [1:0]	CH1 slope compensation 00: 2.2 µH range 01: 1.0 µH range 10: 4.7 µH range 11: 3.3 µH range	00

Register Table 34: Channel3 Zero Frequency (FZ23_EFET <0x21>)

Bit	Mode	Symbol	Description	OTP-80
D[6:5]	R/W	CMP_VO3 [1:0]	CH3 output filter compensation: 00: 3 kHz < LC pole < 8 kHz 01: 7 kHz < LC pole < 12 kHz 10: 11 kHz < LC pole < 18 kHz 11: 17 kHz < LC pole < 30 kHz	10
D4	R/W	EXTFET	CH3 external FET current limit: 0: Typical 200 mV ILIM threshold 1: Typical 100 mV ILIM threshold	0

Note 1 LC pole frequency = $\frac{1}{2\pi\sqrt{L \times Co}}$

Register Table 35: Control (CTL <0x22>)

Bit	Mode	Symbol	Description	OTP-80
D6	R/W	LDSW1F	LDSW1 force ON 0: Current limit enabled 1: Force ON, current limit disabled	0
D[5:4]	R/W	LDO3V [1:0]	LDO2 output voltage: 00: 3.12 V 01: 3.17 V 10: 3.22 V 11: 3.27 V	00 (3.12 V)
D3	R/W	PGCME	Power Good pin output type: 0: Open drain 1: CMOS	0
D2	R/W	PSM4	CH4 Pulse skipping mode enable 0: Not enabled (fixed max duty operation) 1: Enabled (Extended max duty operation)	1
D1	R/W	PSM3	CH3 Pulse skipping mode enable 0: Not enabled (fixed max duty operation) 1: Enabled (Extended max duty operation)	1
D0	R/W	PSM2	CH2 Pulse skipping mode enable 0: Not enabled (fixed max duty operation) 1: Enabled (Extended max duty operation)	1

Note 1 With LDSW1F set high, LDSW1 is controlled only by the EN1 register, and can be enabled with the EN pin low.

Register Table 36: Soft Reset (SRST <0x23>)

Bit	Mode	Symbol	Description	Reset
D[7:0]	R/W	SRST [7:0]	Soft Reset Initiate Soft Reset by writing 0x55.	00000000

Soft Reset resets all registers and shuts down the IC regardless of the EN pin state.

Register Table 37: Hard Short Flag (HDSRT <0x30>)

Bit	Mode	Symbol	Description	Reset
D7	R	NHST4	1: Channel 4 negative current hard short error	0
D6	R	PHST4	1: Channel 4 positive current hard short error	0
D5	R	NHST3	1: Channel 3 negative current hard short error	0
D4	R	PHST3	1: Channel 3 positive current hard short error	0
D3	R	NHST2	1: Channel 2 negative current hard short error	0
D2	R	PHST2	1: Channel 2 positive current hard short error	0
D1	R	NHST1	1: Channel 1 negative current hard short error	0
D0	R	PHST1	1: Channel 1 positive current hard short error	0

Register Table 38: BuckBoost Options (BB_OPT <0x31>)

Bit	Mode	Symbol	Description	OTP-80
D[3:2]	R/W	BST_VTH [1:0]	CH1 BuckBoost transition threshold 00: 80% 01: 85% 10: 70% 11: 75%	00
D1	R/W	PSM1	1: Enable Channel 1 pulse skipping mode	1
D0	R/W	BKONLY	1: Enable buck only mode	0

Register Table 39: Channel 1 and 2 Compensation Settings (CMP12 <0x32>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	EA_CC2 [1:0]	Channel 2 compensation LF pole 00: 0.35 Hz 01: x2 10: x4 11: x8	00
D[5:4]	R/W	EA_HFGAIN2 [1:0]	Channel 2 compensation HF gain 00: 20 dB 01: 26 dB 10: 32 dB 11: 38 dB	00

Bit	Mode	Symbol	Description	OTP-80
D[3:2]	R/W	EA_CC1 [1:0]	Channel 1 compensation LF pole 00: 0.35 Hz 01: x2 10: x4 11: x8	00
D[1:0]	R/W	EA_HFGAIN1 [1:0]	Channel 1 compensation HF gain 00: 20 dB 01: 26 dB 10: 32 dB 11: 38 dB	00

Register Table 40: Channel 3 Compensation Settings (CMP3 <0x33>)

Bit	Mode	Symbol	Description	OTP-80
D[3:2]	R/W	EA_CC3 [1:0]	Channel 3 compensation LF pole 00: 0.35 Hz 01: x2 10: x4 11: x8	00
D[1:0]	R/W	EA_HFGAIN3 [1:0]	Channel 3 compensation HF gain 00: 5 dB 01: 8.5 dB 10: 11 dB 11: 13 dB	00

Register Table 41: Channel 4 Compensation Settings (CMP4 <0x34>)

Bit	Mode	Symbol	Description	OTP-80
D[7:6]	R/W	EA_CC4 [1:0]	CH4 compensation LF pole 00: 0.35 Hz 01: x2 10: x4 11: x8	00
D[5:4]	R/W	EA_HFGAIN4 [1:0]	CH4 compensation HF gain 00: 20 dB 01: 26 dB 10: 32 dB 11: 38 dB	00

Appendix A Optimizing Transient Performance

Although the DA6102 is designed to be stable over the full range of operation with a wide range of external components, each channel's transient response can be fine-tuned for specific application conditions. This is most useful when the output capacitance or inductance is near the edge of the recommended range, which may reduce loop bandwidth or lead to instability. Higher bandwidth is associated with faster transient response, but also with lower stability. When adjusting the compensation register settings or using component values outside the typical range, the stability should always be confirmed either through direct loop gain measurement or load step response.

Current Mode Channels

For channels 1, 2, and 4 there are two available compensation adjustments: EA_CC and EA_HFGAIN. These are found in the CMP12 and CMP4 registers (0x32 and 0x34). The simplified graphic in Figure 43 shows how these registers affect the loop gain, with the comp and mod curves summing to the loop gain.

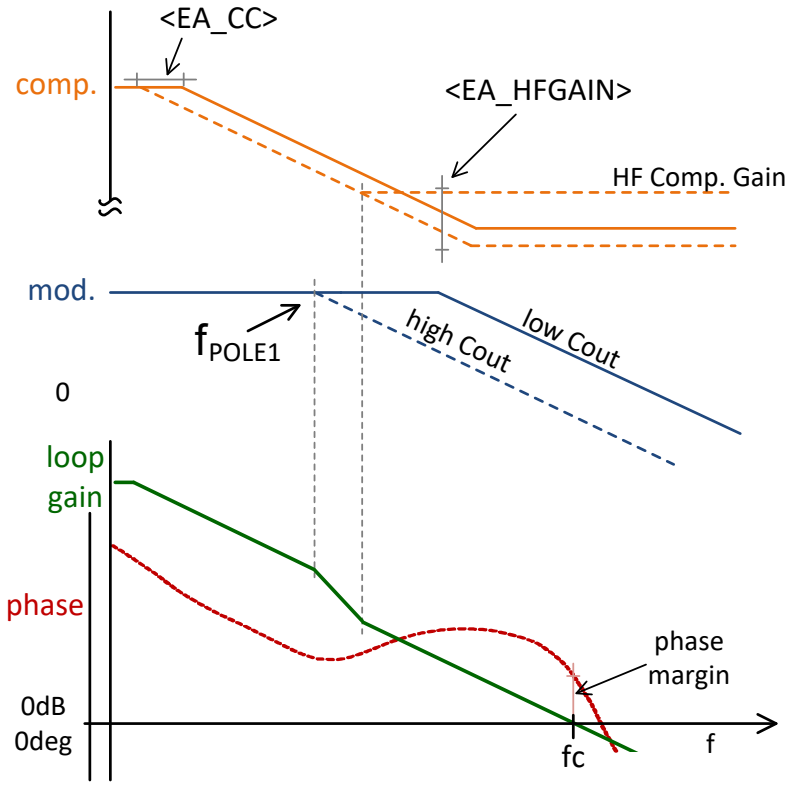


Figure 43: Current Mode Loop Gain

The first step in manually setting the compensation parameters is to determine the primary pole frequency of the output stage. This can be approximated as:

$$f_{POLE1} = \frac{1}{2 \times \pi \times Co \times Ro}$$

where Ro is the load resistance or Vout/Iout; use the nominal load value here.

Referring to Table 14, find the Compensation Zero frequency which is the closest match to the output stage pole frequency and set the EA_CC and EA_HFGAIN bits accordingly. In most cases there are several settings which result in the same zero frequency. Use the setting with the lowest gain initially as this will be the most stable (and lowest bandwidth). The settings can then be modified to increase the gain until the desired response is achieved. At higher gain settings some instability is likely; therefore any change in settings must be tested in the worst case conditions to ensure stability.

Table 14 : Channel 1, 2, and 4 Optional Compensation Settings

EA_CC	EA_HFGAIN	Comp. Zero (Hz)	HF Comp. Gain (dB)
00	00	698	20
01	00	1395	20
10	00	2790	20
11	00	5581	20
00	01	349	26
01	01	698	26
10	01	1395	26
11	01	2790	26
00	10	174	32
01	10	349	32
10	10	698	32
11	10	1395	32
00	11	87	38
01	11	174	38
10	11	349	38
11	11	698	38

Voltage Mode, Channel 3

Compensating Channel 3 follows a similar process to the current mode channels, with the addition of the previously described register setting, CMP_VO3 (0x21). The Channel 3 optional compensation registers are found at CMP3 (0x33). The goal for Channel 3 compensation is to set two compensation zeroes around or just below the LC pole frequency. To accomplish this, first calculate the LC pole frequency highlighted in the mod curve of Figure 44. Next, in Table 15 find the closest Zero1 frequency equal or less than the LC pole frequency and set the EA_CC3 and EA_HFGAIN3 bits accordingly. In most cases there are several settings which result in the same Zero1 frequency. Use the setting with the lowest gain initially as this will be the most stable (and lowest bandwidth). Next set the Zero2 frequency with CMP_VO3 in Table 15 that most closely matches or is just below the LC pole frequency.

The SLP_VO3 register at 0x20 controls the PWM ramp for Channel3, which determines the modulator gain. In the rare case where the loop cannot be stabilized as described above, the overall gain can be reduced by setting SLP_VO3 to 01.

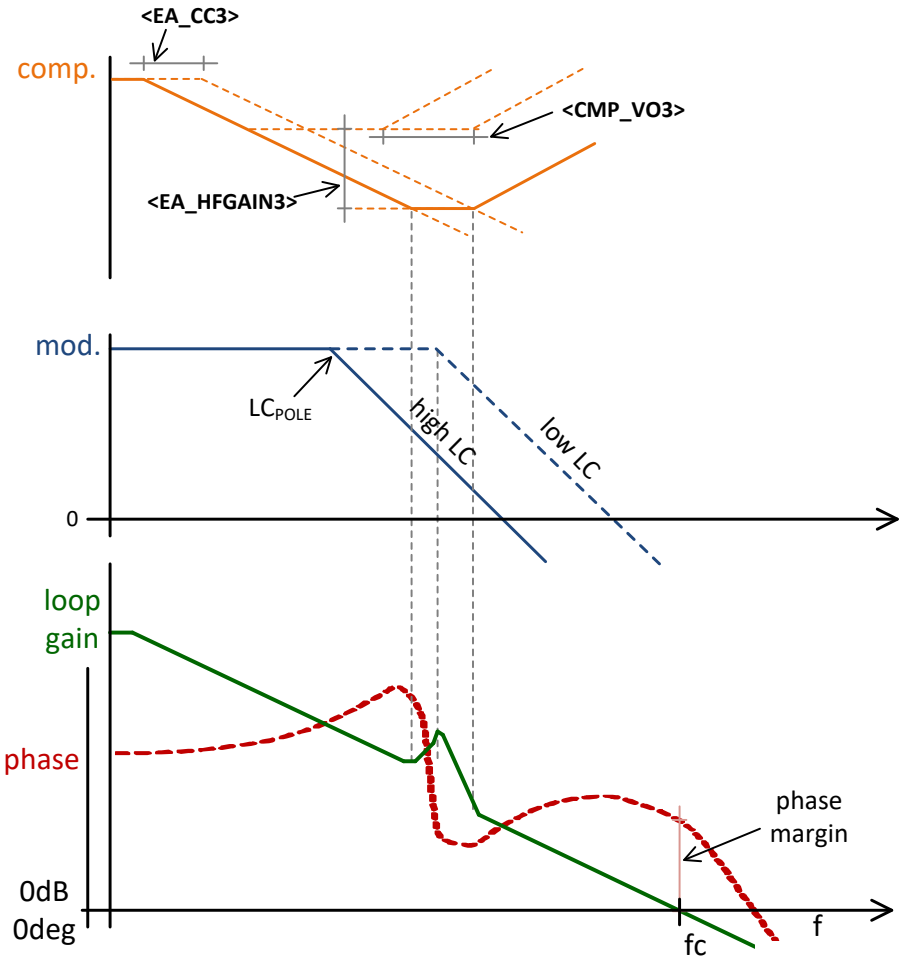


Figure 44: Voltage Mode Loop Gain (Channel3)

Table 15: Channel 3 Optional Compensation Settings

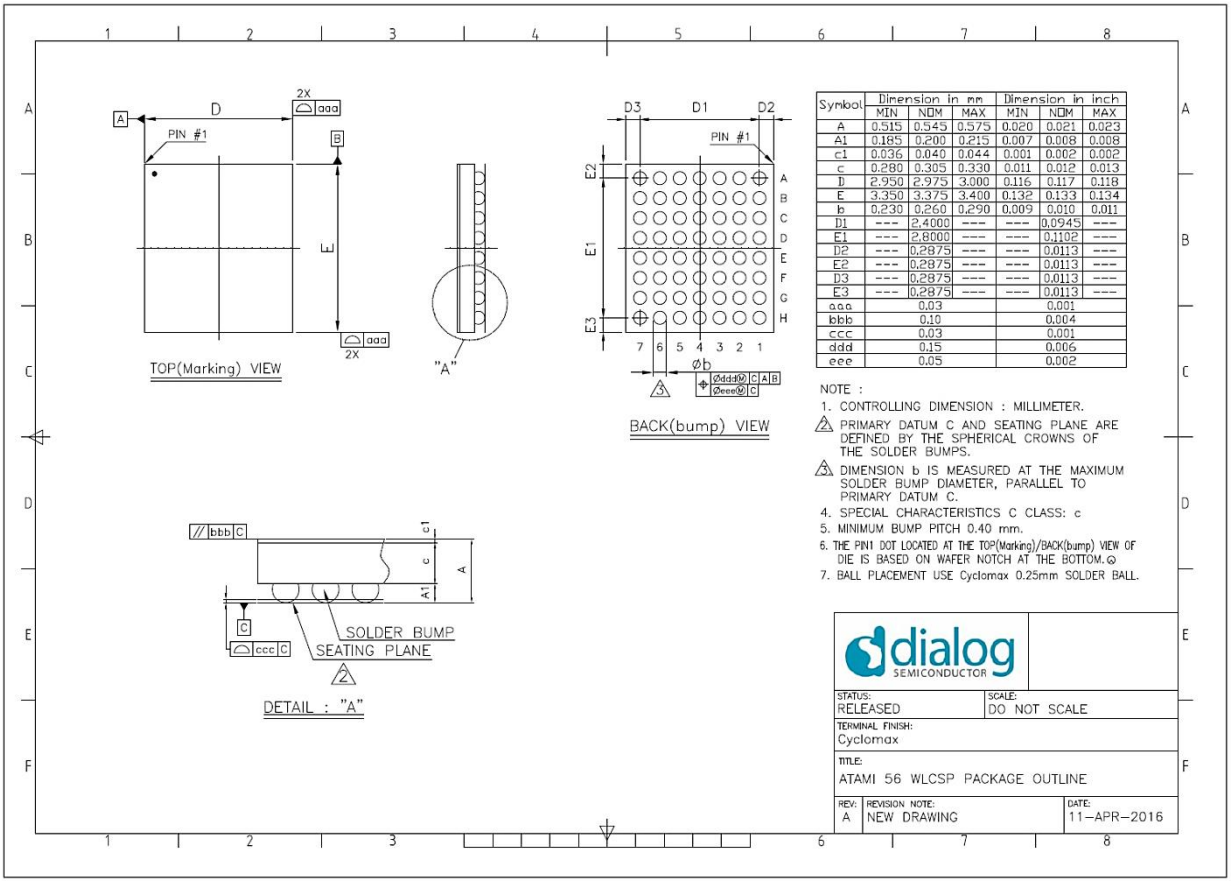
<EA_CC3>	<EA_HFGAIN3>	Zero 1 (kHz)	Mid-Band Gain (dB)
00	00	3.9	5
01	00	7.8	5
10	00	15.7	5
11	00	31.4	5
00	01	2.6	8.5
01	01	5.2	8.5
10	01	10.5	8.5
11	01	21.0	8.5
00	10	2.0	11
01	10	3.9	11
10	10	7.9	11
11	10	15.7	11
00	11	1.6	13

<EA_CC3>	<EA_HFGAIN3>	Zero 1 (kHz)	Mid-Band Gain (dB)
01	11	3.1	13
10	11	6.2	13
11	11	12.5	13

CMP_VO3	Zero 2 (kHz)
00	3.5
01	8
10	16
11	32

11 Package Information

11.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.515	0.545	0.575	0.020	0.021	0.023
A1	0.185	0.200	0.215	0.007	0.008	0.008
c1	0.036	0.040	0.044	0.001	0.002	0.002
c	0.280	0.305	0.330	0.011	0.012	0.013
D	2.950	2.975	3.000	0.116	0.117	0.118
E	3.350	3.375	3.400	0.132	0.133	0.134
b	0.230	0.260	0.290	0.009	0.010	0.011
D1	---	2.4000	---	---	0.0945	---
E1	---	2.8000	---	---	0.1102	---
D2	---	0.2875	---	---	0.0113	---
E2	---	0.2875	---	---	0.0113	---
D3	---	0.2875	---	---	0.0113	---
E3	---	0.2875	---	---	0.0113	---
aaa	0.03			0.001		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.15			0.006		
eee	0.05			0.002		

Figure 45: Package Outline Drawing

11.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity (RH) before the solder reflow process. The MSL classification is defined in Table 16.

The WLCSP package is qualified for MSL 1.

Table 16: MSL Classification

MSL level	Floor Lifetime
MSL 1	Unlimited at 30 °C / 85 % RH

11.3 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 17: Ordering Information

Part number	Package	Size (mm)	Shipment form	Pack Quantity
DA6102-xxVL2 (Note 1)	WLCSP-56	2.975 x 3.375	Tape and Reel	7500

Note 1 OTP variants are indicated by xx in the part number above.

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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