ACS541MS

Radiation Hardened Octal Buffer/Line Driver Three-State

FN4085
Rev.0.00
January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96710 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
- SEU LET Threshold>100 MEV-cm^2/mg
- Dose Rate Upset>10^{11} RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability>10^{12} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range-55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay17ns (Max), 12ns (Typ)

Description

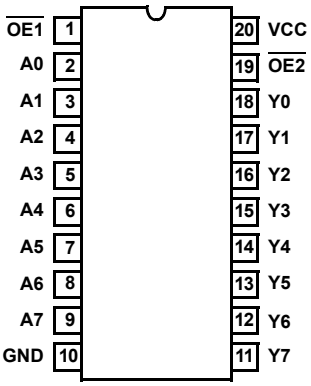
The Intersil ACS541MS is a Radiation Hardened Octal Buffer/Line Driver, with three-state outputs. The output enable pins $\overline{OE1}$, $\overline{OE2}$ control the Three-State outputs. If either enable is high the output will be in a high impedance state. For data output both enables must be low.

The ACS541MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

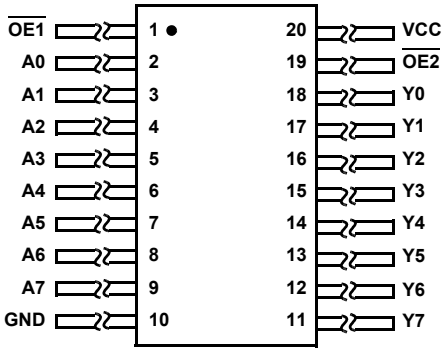
The ACS541MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line package (D suffix).

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR,
CDIP2-T20, LEAD FINISH C
TOP VIEW



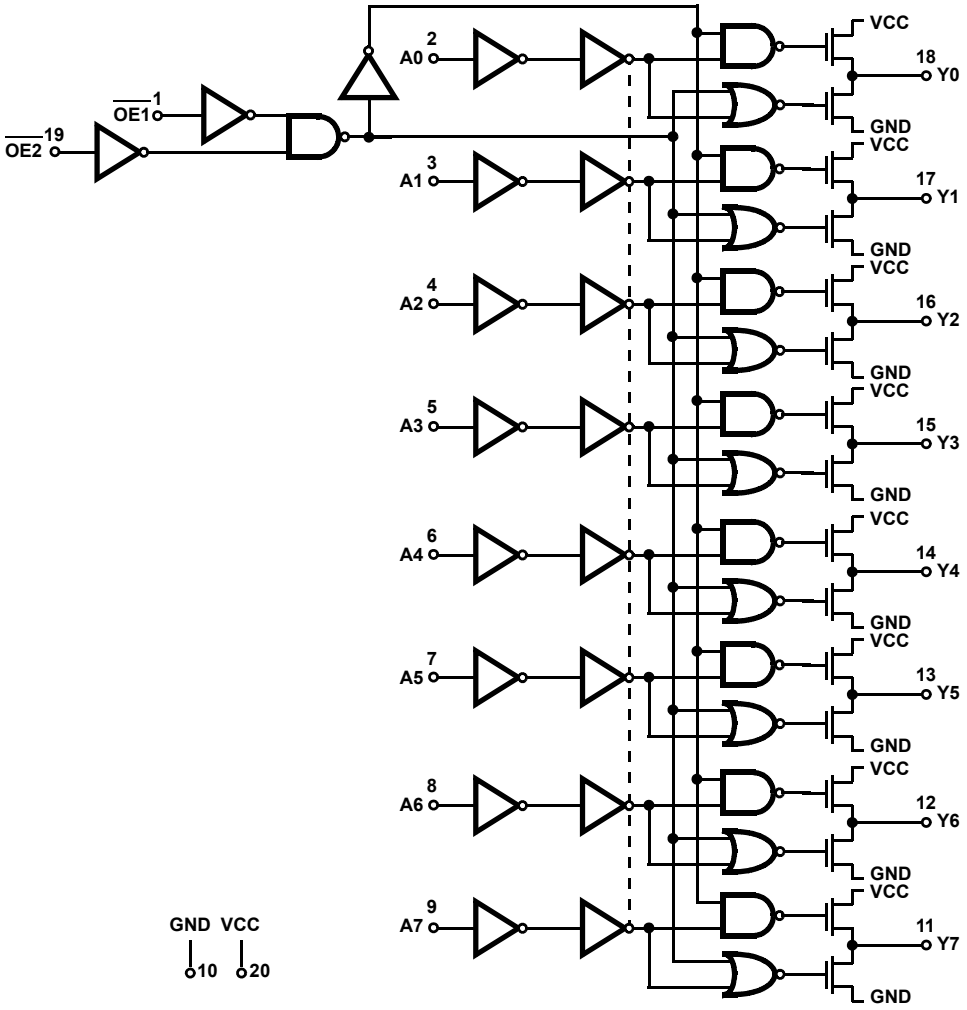
20 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR,
CDFP4-F20, LEAD FINISH C
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9671001VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9671001VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACS541D/Sample	25°C	Sample	20 Lead SBDIP
ACS541K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACS541HMSR	25°C	Die	Die

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	An	Yn
L	L	H	H
L	L	L	L
H	X	X	Z
X	H	X	Z

NOTE: L = Low Logic Level, H = High Logic Level, Z = High Impedance

Die Characteristics

DIE DIMENSIONS:

102 mils x 102 mils
2,600mm x 2,600mm

METALLIZATION:

Type: AlSi
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5$ A/cm^2

BOND PAD SIZE:

> 4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout

ACS541MS