

## DDR Phase Lock Loop Clock Driver (60MHz - 210MHz)

### Recommended Application:

DDR Clock Driver

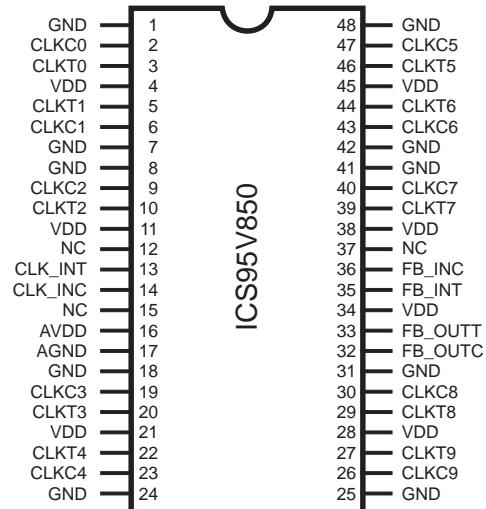
### Product Description/Features:

- Low skew, low jitter PLL clock driver
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- With bypass mode mux
- Operating frequency 60 to 210 MHz
- AC Coupled (Universal) CLK inputs:
  - 400 mV switching amplitude
  - (LVTTL, LVPELL, LVDS, LVC MOS) standards translation to SSTL2

### Switching Characteristics:

- CYCLE - CYCLE jitter: <60ps
- OUTPUT - OUTPUT skew: <60ps
- Period jitter:  $\pm 30$ ps
- DUTY CYCLE: 49.5% - 50.5%

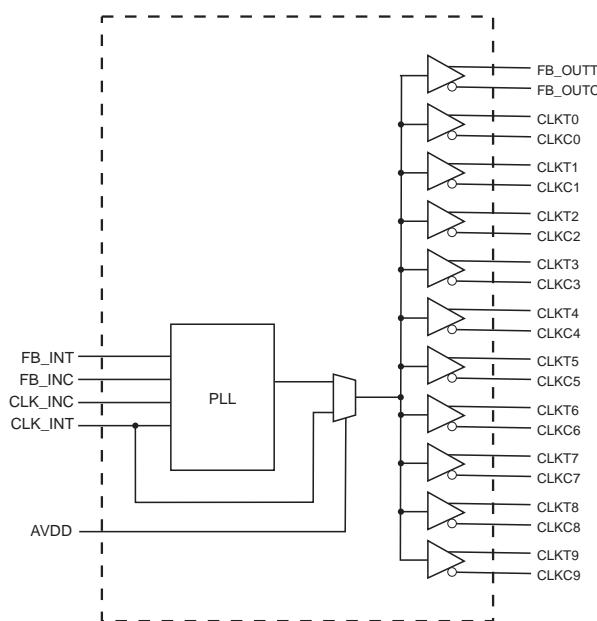
### Pin Configuration



48-Pin TSSOP

6.10mm Body, 0.5mm Pitch

### Block Diagram



### Functionality

AVDD	INPUTS			OUTPUTS			PLL State
	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V (nom)	L	H	L	H	L	H	On
2.5V (nom)	H	L	H	L	H	L	On

## Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLK[9:0]	OUT	"Complementary" clocks of differential pair outputs
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLK[9:0]	OUT	"True" Clock of differential pair outputs
4, 11, 21, 28, 34, 38, 45,	VDD	PWR	Power supply, 2.5V
13	CLK_INT	IN	"True" reference clock input
14	CLK_INC	IN	"Complementary" reference clock input
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground
32	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC
33	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT
35	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error
36	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error
12, 15, 37	NC		No Connects

## Absolute Maximum Ratings

Supply Voltage: (VDD & AVDD) .....	-0.5V to 3.6V
Input clamp current: $I_{IK}$ ( $V_I < 0$ or $V_I > VDD$ ) .....	+/- 50mA
Output clamp current: $I_{OK}$ ( $V_O < 0$ or $V_O > VDD$ ) ..	+/- 50mA
Continuous output current: $I_O$ ( $V_O = 0$ to $VDD$ ) ..	+/- 50mA
Package thermal impedance, theta JA: DGG package	+89°C/Ω
Storage Temperature .....	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0$  - 85°C; Supply Voltage  $A_{VDD}$ ,  $V_{DD} = 2.5$  V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	$I_{IH}$	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	$I_{IL}$	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	$C_L = 0\text{pf}$ @ 200MHz			148	mA
	$I_{DDPD}$	$C_L = 0\text{pf}$			100	µA
High Impedance Output Current	$I_{OZ}$	$V_{DD} = 2.7$ V, $V_{out} = V_{DD}$ or GND			$\pm 10$	mA
Input Clamp Voltage	$V_{IK}$	$V_{DD} = 2.3$ V $I_{in} = -18$ mA			-1.2	V
High-level output voltage	$V_{OH}$	$I_{OH} = -1$ mA	$V_{DD} - 0.1$			V
		$I_{OH} = -12$ mA	1.7V			V
Low-level output voltage	$V_{OL}$	$I_{OL} = 1$ mA			0.1	V
		$I_{OH} = 12$ mA			0.6	V
Input Capacitance <sup>1</sup>	$C_{IN}$	$V_I = GND$ or $V_{DD}$	2.5		3.5	pF

<sup>1</sup>Guaranteed by design at 233MHz, not 100% tested in production.

### Recommended Operating Condition (see note1)

$T_A = 0 - 85^\circ\text{C}$ ; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}, A_{VDD}$		2.3	2.5	2.7	V
Low level input voltage	$V_{IL}$	CLK_INT, CLK_INC, FB_INC		0.4	$V_{DD}/2 - 0.18$	V
		CLK_INT, CLK_INC (Universal Input)	-0.3		$V_{DD} - 0.4$	V
High level input voltage	$V_{IH}$	CLK_INT, CLK_INC, FB_INC	$V_{DD}/2 + 0.18$	2.1		V
		CLK_INT, CLK_INC (Universal Input)	0.4		$V_{DD} + 0.3$	V
DC input signal voltage (note 2)	$V_{IN}$		-0.3		$V_{DD} + 0.3$	V
Differential input signal voltage (note 3)	$V_{ID}$	DC - CLK_INT, FB_INT	0.36		$V_{DD} + 0.6$	V
		AC - CLK_INT, FB_INT (Universal Input)	0.4		$V_{DD} + 0.6$	V
Output differential cross-voltage (note 4)	$V_{OX}$		$V_{DD}/2 - 0.15$		$V_{DD}/2 + 0.15$	V
Input differential cross-voltage (note 4)	$V_{IX}$	(Universal Input)	$0.45(V_{IH} - V_{IL})$		$0.55(V_{IH} - V_{IL})$	V
High level output current	$I_{OH}$				-6.4	mA
Low level output current	$I_{OL}$				5.5	mA
Operating free-air temperature	$T_A$		0		85	$^\circ\text{C}$

#### Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of  $V_{DD}$  and is the voltage at which the differential signal must be crossing.

### Timing Requirements

$T_A = 0 - 85^\circ\text{C}$ ; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating clock frequency	$\text{freq}_{op}$		66		210	MHz
Input clock duty cycle	$d_{tin}$		40		60	%
CLK stabilization	$T_{STAB}$				15	$\mu\text{s}$

### Switching Characteristics (see note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	$t_{PLH}^1$	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	$t_{PLL}^1$	CLK_IN to any output		5.5		ns
Period jitter	$T_{jit\ (per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	$t_{(jit\_hper)}$	100MHz to 200MHz	-75		30	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2.5	V/ns
Cycle to Cycle Jitter <sup>1</sup>	$T_{cyc}-T_{cyc}$	100MHz to 200MHz			60	ps
Phase error	$t_{(phase\ error)}^4$		-50	0	50	ps
Output to Output Skew	$T_{skew}$				60	ps

#### Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle =  $t_{wH}/t_c$ , where the cycle ( $t_c$ ) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

Parameter Measurement Information

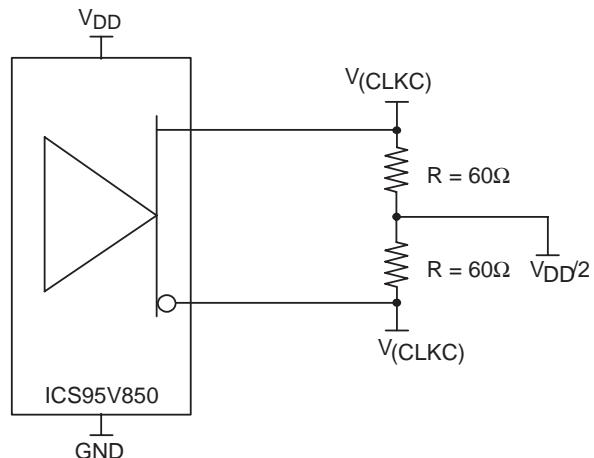
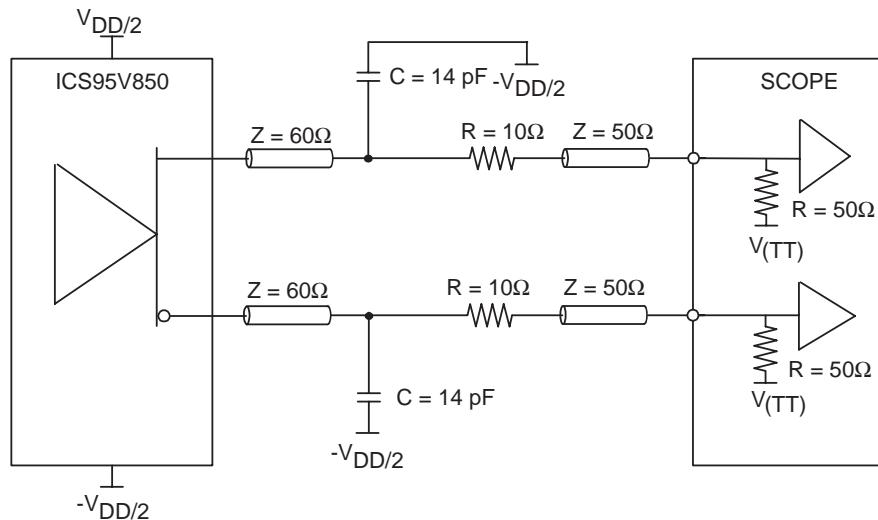
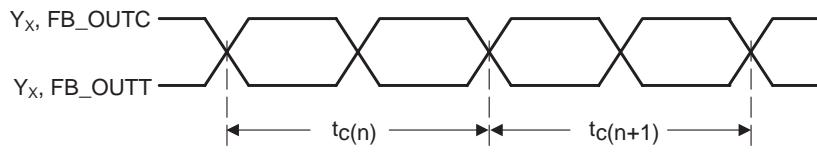


Figure 1. IBIS Model Output Load



NOTE:  $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit



$$t_{\text{jit(cc)}} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

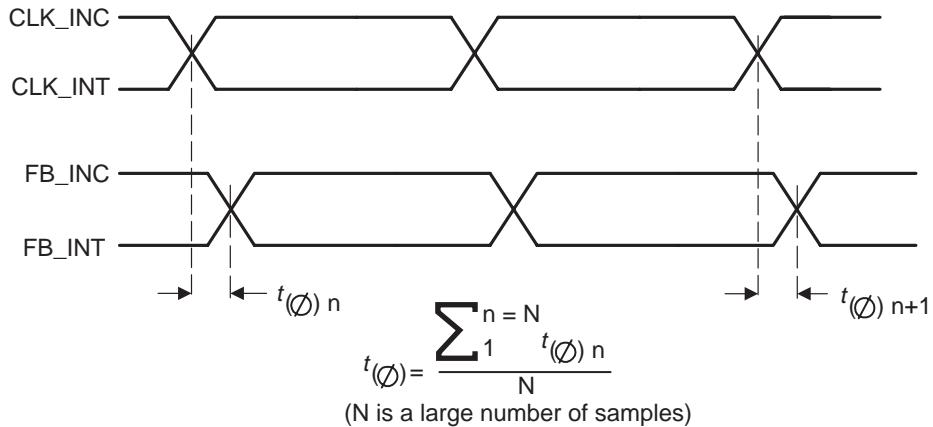


Figure 4. Static Phase Offset

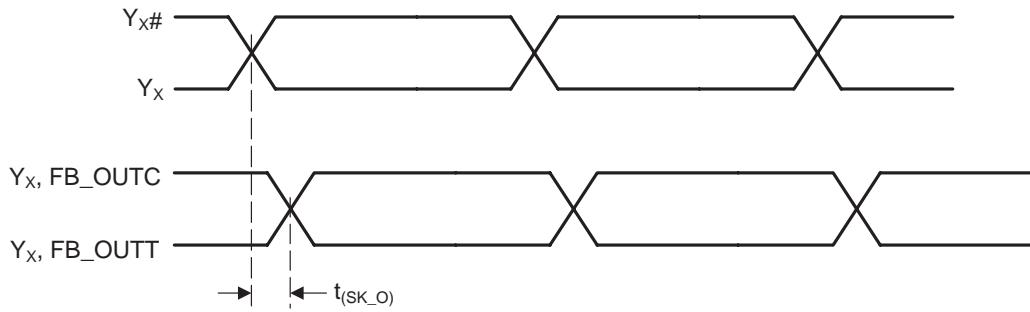


Figure 5. Output Skew

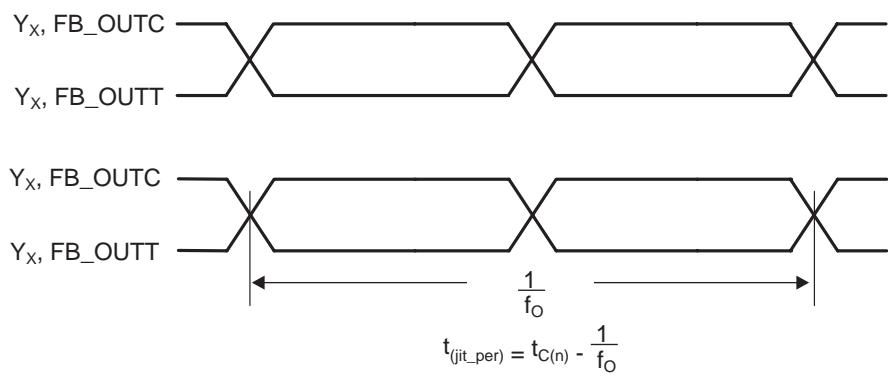
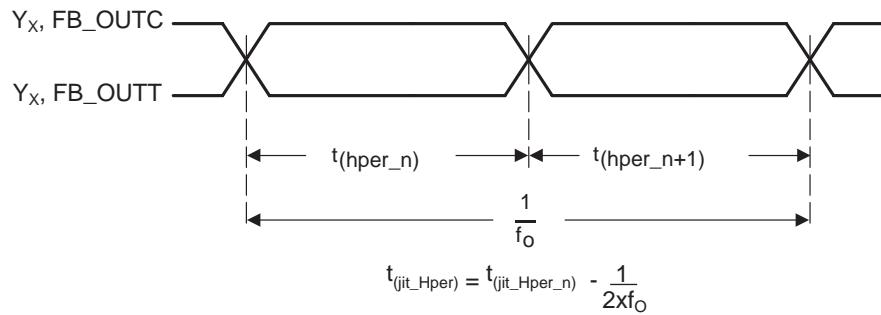
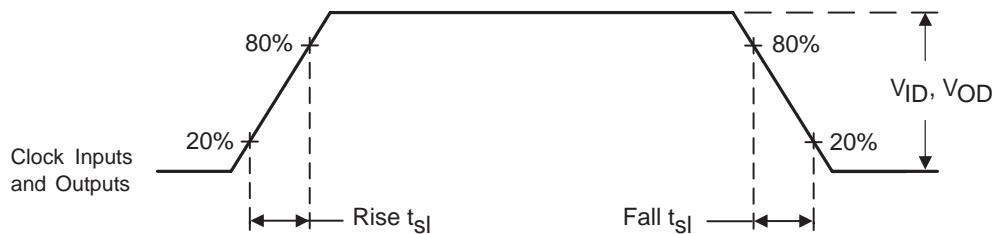


Figure 6. Period Jitter

**Parameter Measurement Information**



**Figure 7. Half-Period Jitter**



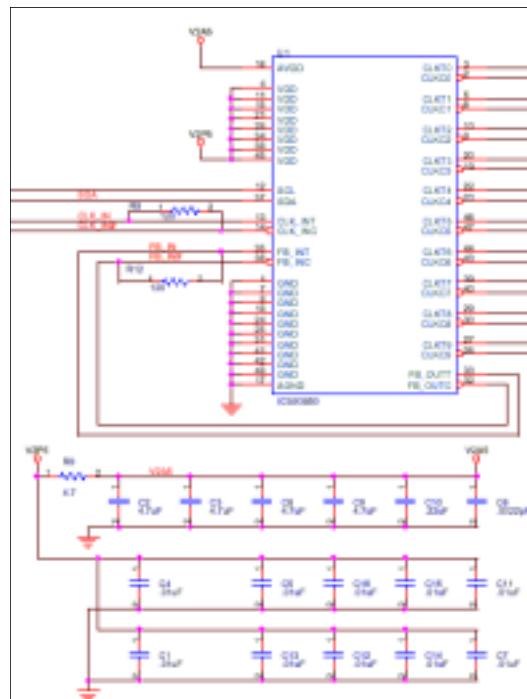
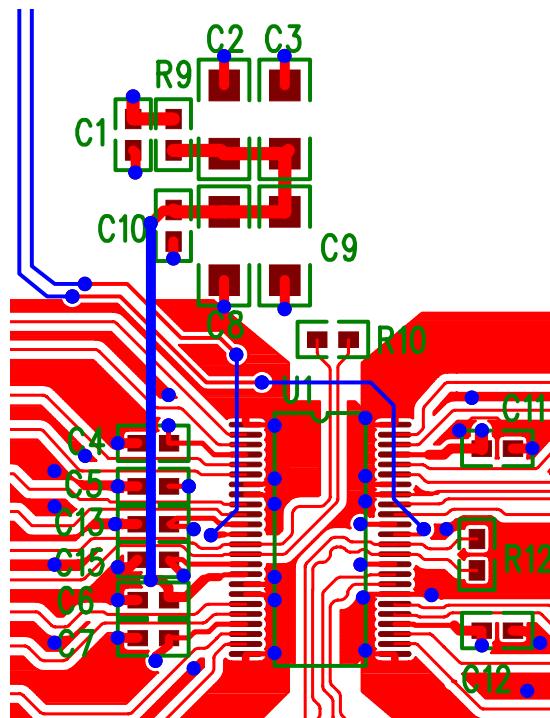
**Figure 8. Input and Output Slew Rates**

## Recommended Layout for the ICS95V850

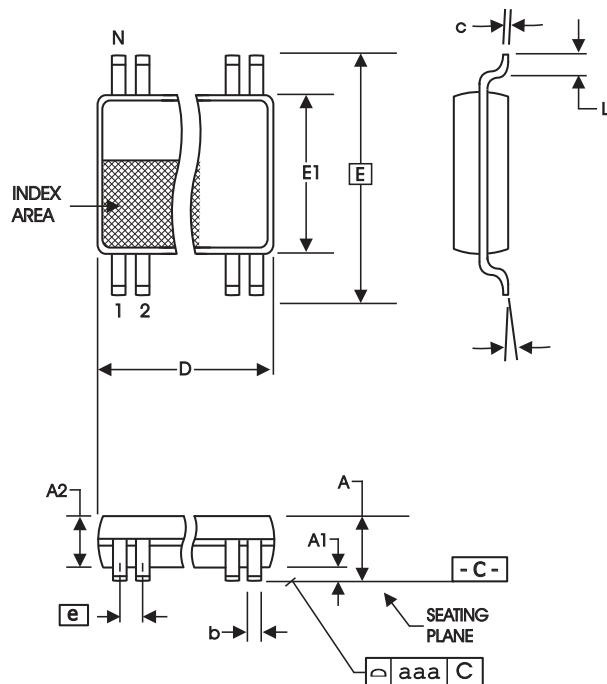
### **General Layout Precautions:**

Use copper flooded ground on the top signal layer under the clock buffer. The area under U1 on the right is an example. Flood over the ground vias.

- 1) Use power vias for power and ground. Vias 20 mil or larger in diameter have lower high frequency impedance. Vias for signals may be minimum drill size.
- 2) Make all power and ground traces are as wide as the via pad for lower inductance.
- 3) VAA for pin 16 has a low pass RC filter to decouple the digital and analog supplies. The 4.7uF capacitors may be replaced with a single low ESR device with the same total capacitance. VAA is routed on a outside signal layer. Do not cut a power or ground plane and route in it.
- 4) Notice that ground vias are never shared.
- 5) When ever possible, VCC (net V2P5 in the schematic) pins have a decoupling capacitor. Power is always routed from the plane connection via to the capacitor pad to the VCC pin on the clock buffer. Moats or plane cuts are not used to isolate power.
- 6) Differential mode clock output traces are routed:
  - a. With a ground trace between the pairs. Trace is grounded on both ends.
  - b. Without a ground trace, clock pairs are routed with a separation of at least 5 times the thickness of the dielectric. If the dielectric thickness is 4.5 mil, the trace separation is at least 18 mils.
- 7) Terminate differential CLK\_IN and FB\_IN traces after routing to buffer pads.



Component Values:				
Ref	Desg.	Value	Description	Package
C1, C4, C5, C7, C11, C12		.01uF	CERAMIC MLC	0603
C2, C3, C8, C9		4.7uF	CERAMIC MLC	1206
C10		.22uF	CERAMIC MLC	0603
C6		2200pF	CERAMIC MLC	0603
R9, R12		120 $\Omega$		0603
R9		4.7 $\Omega$		0603
U1			ICS95V850	TSSOP48



6.10 mm. Body, 0.50 mm. pitch TSSOP  
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	.004

#### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

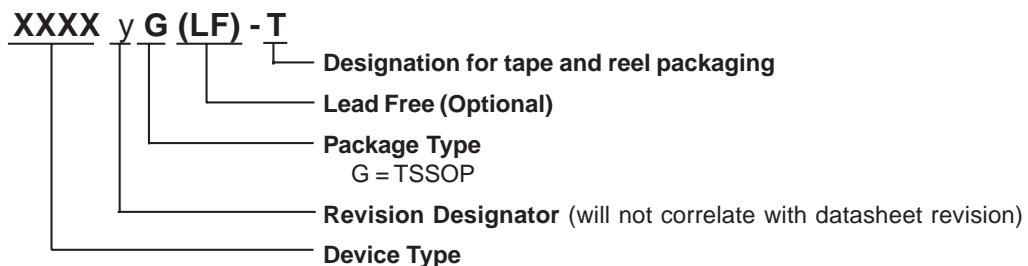
Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

### 95V850yLFGT

Example:



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