

Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

VIA PT890/894 style chipset

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 10 - PCI, 33MHz
- 2 - REF, 14.318MHz
- 3 - 3V66, 66.66MHz
- 1 - 48MHz
- 1 - 24/48MHz selectable output
- 3 - PCI Express™ 0.7V current mode differential pairs
- 1 CPU/PCI Express 0.7 current mode selectable differential pair

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 500ps
- PCI Express outputs cycle-cycle jitter < 125ps

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	PCIEX	3v66	PCI
FS4	FS3	FSL2	FSL1	FSL0	MHz	MHz	MHz	MHz
0	0	0	0	0	266.66	100.00	66.67	33.33
0	0	0	0	1	133.33	100.00	66.67	33.33
0	0	0	1	0	200.00	100.00	66.67	33.33
0	0	0	1	1	N/A	N/A	N/A	N/A
0	0	1	0	0	N/A	N/A	N/A	N/A
0	0	1	0	1	100.00	100.00	66.67	33.33
0	0	1	1	0	400.00	100.00	66.67	33.33
0	0	1	1	1	200.00	100.00	66.67	33.33
0	1	0	0	0	266.66	133.33	66.67	33.33
0	1	0	0	1	133.33	133.33	66.67	33.33
0	1	0	1	0	200.00	133.33	66.67	33.33
0	1	0	1	1	N/A	N/A	N/A	N/A
0	1	1	0	0	N/A	N/A	N/A	N/A
0	1	1	0	1	100.00	133.33	66.67	33.33
0	1	1	1	0	400.00	133.33	66.67	33.33
0	1	1	1	1	200.00	133.33	66.67	33.33
1	0	0	0	0	269.33	101.00	67.33	33.67
1	0	0	0	1	134.66	101.00	67.33	33.67
1	0	0	1	0	202.00	101.00	67.33	33.67
1	0	0	1	1	N/A	N/A	N/A	N/A
1	0	1	0	0	274.66	103.00	68.66	34.33
1	0	1	0	1	137.33	103.00	68.66	34.33
1	0	1	1	0	206.00	103.00	68.67	34.33
1	0	1	1	1	N/A	N/A	N/A	N/A
1	1	0	0	0	279.99	105.00	70.00	35.00
1	1	0	0	1	140.00	105.00	70.00	35.00
1	1	0	1	0	210.00	105.00	70.00	35.00
1	1	0	1	1	N/A	N/A	N/A	N/A
1	1	1	0	0	287.99	108.00	72.00	36.00
1	1	1	0	1	144.00	108.00	72.00	36.00
1	1	1	1	0	216.00	108.00	72.00	36.00
1	1	1	1	1	N/A	N/A	N/A	N/A

Pin Configuration

VDDA	1	56	GND
GND	2	55	IREF
VDDREF	3	54	CPUCLKT0
**FS _L 0/REF0	4	53	CPUCLKC0
FS _L 1/REF1	5	52	GNDCPU
X1	6	51	CPUCLKT1
X2	7	50	CPUCLKC1
GNDREF	8	49	VDDCPU
VttPWR_GD/PD#	9	48	SDATA
**FS _L 2/PCICLK0	10	47	CPUCLKT2/PCIEXT0
**FS3/~PCICLK1	11	46	CPUCLKC2/PCIEXC0
PCICLK2	12	45	VDDPCIEX
PCICLK3	13	44	PCIEXT1
GNDPCI	14	43	PCIEXC1
VDDPCI	15	42	PCIEXT2
PCICLK4	16	41	PCIEXC2
PCICLK5	17	40	GNDPCIEX
PCICLK6	18	39	VDDPCIEX
VDDPCI	19	38	PCIEXT3
GNDPCI	20	37	PCIEXC3
PCICLK7	21	36	GNDPCIEX
PCICLK8	22	35	SCLK
PCICLK9	23	34	GND3V66
*Turbo#	24	33	3V66_0
Reset#	25	32	3V66_1/FS4**
VDD48	26	31	3V66_2/Mode0**
48MHz	27	30	VDD3V66
*Sel24_48#/24_48MHz	28	29	GND48

56-Pin SSOP

*These inputs have 120K internal pull-up resistors to VDD.

**These inputs have 120K internal pull-down resistors to GND.

~This output is default 2X drive strength.

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDA	PWR	3.3V power for the PLL core.
2	GND	PWR	Ground pin.
3	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
4	**FSL0/REF0	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 14.318 MHz reference clock.
5	FSL1/REF1	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 14.318 MHz reference clock.
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GNDREF	PWR	Ground pin for the REF outputs.
9	VttPWR_GD/PD#	IN	This 3.3V LVTTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
10	**FSL2/PCICLK0	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 3.3V PCI clock output.
11	**FS3/PCICLK1	I/O	Frequency select latch input pin / 3.3V PCI clock output.
12	PCICLK2	OUT	PCI clock output.
13	PCICLK3	OUT	PCI clock output.
14	GNDPCI	PWR	Ground pin for the PCI outputs
15	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
16	PCICLK4	OUT	PCI clock output.
17	PCICLK5	OUT	PCI clock output.
18	PCICLK6	OUT	PCI clock output.
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	GNDPCI	PWR	Ground pin for the PCI outputs
21	PCICLK7	OUT	PCI clock output.
22	PCICLK8	OUT	PCI clock output.
23	PCICLK9	OUT	PCI clock output.
24	*Turbo#	IN	Real time input pin to change frequency to a pre-programmed under or over clock entries located in the Rom table.
25	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
26	VDD48	PWR	Power pin for the 48MHz output.3.3V
27	48MHz	OUT	48MHz clock output.
28	*Sel24_48#/24_48MHz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24MHz, 0 = 48MHz.

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
29	GND48	PWR	Ground pin for the 48MHz outputs
30	VDD3V66	PWR	Power pin for the 3.3V 66MHz clocks.
31	3V66_2/Mode0**	I/O	3.3V 66.66MHz clock output / Function select latch input pin for CPUCLK/PCIEX selectable pin. 0 = PCIEXT/C ; 1 = CPUCLKT/C.
32	3V66_1/FS4**	I/O	3.3V 66.66MHz clock output. / Frequency select latch input pin
33	3V66_0	OUT	3.3V 66.66MHz clock output
34	GND3V66	PWR	Ground pin for the 3.3V 66MHz clocks
35	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
36	GNDPCIEX	PWR	Ground pin for the PCI-EX outputs
37	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
38	PCIEXT3	OUT	True clock of differential PCI_Express pair.
39	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
40	GNDPCIEX	PWR	Ground pin for the PCI-EX outputs
41	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
42	PCIEXT2	OUT	True clock of differential PCI_Express pair.
43	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
44	PCIEXT1	OUT	True clock of differential PCI_Express pair.
45	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
46	CPUCLKC2/PCIEXC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias./ Complement clock of differential PCIEX pair
47	CPUCLKT2/PCIEXT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair
48	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
49	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
50	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
51	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	GNDCPU	PWR	Ground pin for the CPU outputs
53	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
54	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
55	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
56	GND	PWR	Ground pin.

General Description

ICS953008 is a 56-pin clock chip for P4 type processors with PCI Express.

Block Diagram

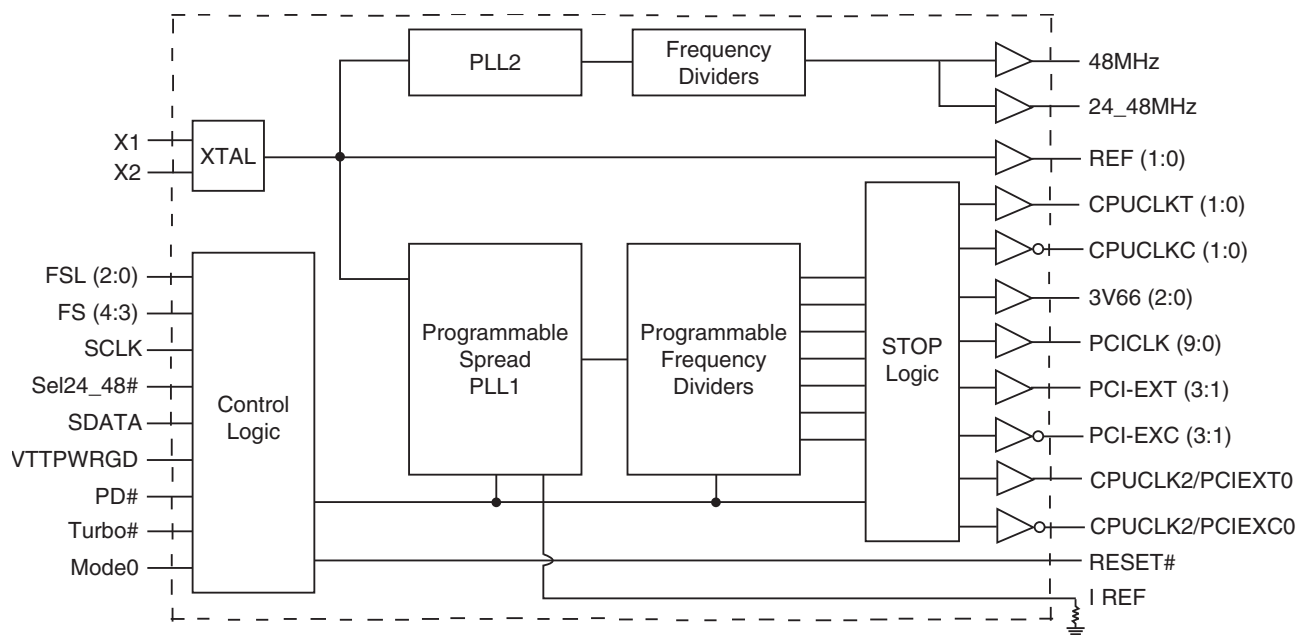


Table1: Frequency Selection Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	PCIEX	3V66	PCI	Spread
FS4	FS3	FSL2	FSL1	FSL0	MHz	MHz	MHz	MHz	%
0	0	0	0	0	266.66	100.00	66.67	33.33	0 to -0.5% Down
0	0	0	0	1	133.33	100.00	66.67	33.33	0 to -0.5% Down
0	0	0	1	0	200.00	100.00	66.67	33.33	0 to -0.5% Down
0	0	0	1	1	N/A	N/A	N/A	N/A	N/A
0	0	1	0	0	N/A	N/A	N/A	N/A	N/A
0	0	1	0	1	100.00	100.00	66.67	33.33	0 to -0.5% Down
0	0	1	1	0	400.00	100.00	66.67	33.33	0 to -0.5% Down
0	0	1	1	1	200.00	100.00	66.67	33.33	0 to -0.5% Down
0	1	0	0	0	266.66	133.33	66.67	33.33	+/-0.3% Center
0	1	0	0	1	133.33	133.33	66.67	33.33	+/-0.3% Center
0	1	0	1	0	200.00	133.33	66.67	33.33	+/-0.3% Center
0	1	0	1	1	N/A	N/A	N/A	N/A	N/A
0	1	1	0	0	N/A	N/A	N/A	N/A	N/A
0	1	1	0	1	100.00	133.33	66.67	33.33	+/-0.3% Center
0	1	1	1	0	400.00	133.33	66.67	33.33	+/-0.3% Center
0	1	1	1	1	200.00	133.33	66.67	33.33	+/-0.3% Center
1	0	0	0	0	269.33	101.00	67.33	33.67	+/-0.3% Center
1	0	0	0	1	134.66	101.00	67.33	33.67	+/-0.3% Center
1	0	0	1	0	202.00	101.00	67.33	33.67	+/-0.3% Center
1	0	0	1	1	N/A	N/A	N/A	N/A	N/A
1	0	1	0	0	274.66	103.00	68.66	34.33	+/-0.3% Center
1	0	1	0	1	137.33	103.00	68.66	34.33	+/-0.3% Center
1	0	1	1	0	206.00	103.00	68.67	34.33	+/-0.3% Center
1	0	1	1	1	N/A	N/A	N/A	N/A	N/A
1	1	0	0	0	279.99	105.00	70.00	35.00	+/-0.3% Center
1	1	0	0	1	140.00	105.00	70.00	35.00	+/-0.3% Center
1	1	0	1	0	210.00	105.00	70.00	35.00	+/-0.3% Center
1	1	0	1	1	N/A	N/A	N/A	N/A	N/A
1	1	1	0	0	287.99	108.00	72.00	36.00	+/-0.3% Center
1	1	1	0	1	144.00	108.00	72.00	36.00	+/-0.3% Center
1	1	1	1	0	216.00	108.00	72.00	36.00	+/-0.3% Center
1	1	1	1	1	N/A	N/A	N/A	N/A	N/A

General SMBus serial interface information for the ICS953008

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		
		ACK
○		○
○		○
○		○
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 _(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3 _(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
ACK		Beginning Byte N
		○
○		○
○		○
○		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	SS_EN1	PLL1 Spread Enable	RW	OFF	ON	0
Bit 5	-	SS_EN2	PLL2 Spread Enable	RW	OFF	ON	1
Bit 4	-	FS4	Freq Select Bit 4	RW	See Table1:PLL1 Frequency Selection Table		Latch
Bit 3	-	FS3	Freq Select Bit 3	RW			Latch
Bit 2	-	FSL2	Freq Select Bit 2	RW			Latch
Bit 1	-	FSL1	Freq Select Bit 1	RW			Latch
Bit 0	-	FSL0	Freq Select Bit 0	RW			Latch

I²C Table: General Device Behaviour Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	IREF Bit0	IREF Multiplier Programming Bits	RW	6 x Iref	7 x Iref	0
Bit 6	-	SEL24_48MHz	Output Select	RW	48MHz	24MHz	Latch
Bit 5	-	Mode 0	Output Select	RW	PCIEXCLKT/C0	CPUCLKT/C2	Latch
Bit 4	-	PCIEX PLL Cntrl	PCIEX PLL Source	RW	Sync	Async	0
Bit 3	-	3V66/PCI PLL Cntrl	3V66/PCI PLL Source	RW	Sync	Async (PLL2)	0
Bit 2	-	ASYN01	3V66/PCI Async Freq Prog bits	RW	00 = PLL2	10 = 75.4/37.7	0
Bit 1	-	ASYN00		RW	01 = 66.0/33.0	11 = 88.0/44.0	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REF0	Output Control	RW	Disable	Enable	1
Bit 6	-	REF1	Output Control	RW	Disable	Enable	1
Bit 5	-	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 4	-	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 3	-	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 2	-	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 1	-	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 0	-	PCICLK5	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	48MHz	Output Control	RW	Disable	Enable	1
Bit 6	-	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	3V66_2	Output Control	RW	Disable	Enable	1
Bit 4	-	3V66_1	Output Control	RW	Disable	Enable	1
Bit 3	-	3V66_0	Output Control	RW	Disable	Enable	1
Bit 2	-	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 1	-	PCICLK7	Output Control	RW	Disable	Enable	1
Bit 0	-	PCICLK8	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIEXCLKT/C3	Output Control	RW	Disable	Enable	1
Bit 6	-	PCIEXCLKT/C2	Output Control	RW	Disable	Enable	1
Bit 5	-	PCIEXCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 4	-	CPUCLK2/PCIEX0	Output Control	RW	Disable	Enable	1
Bit 3	-	CPUCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 2	-	CPUCLKT/C0	Output Control	RW	Disable	Enable	1
Bit 1	-	PCICLK9	Output Control	RW	Disable	Enable	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Programmable Skew Control Register

Byte 5		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		PCISkw3	CPU-PCI 7 Steps Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 6	-		PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 5	-		PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-		PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-		3V66Skw3	CPU-3V66 7 Steps Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 2	-		3V66Skw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	0
Bit 1	-		3V66Skw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 0	-		3V66Skw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0

I²C Table: Reserved Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved		RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved		RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved		RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved		RW	-	-	1

I²C Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REVID3	Revision ID	R	-	-	0
Bit 6	-	REVID2	Revision ID	R	-	-	0
Bit 5	-	REVID1	Revision ID	R	-	-	0
Bit 4	-	REVID0	Revision ID	R	-	-	0
Bit 3	-	VID3	Vendor ID	R	-	-	0
Bit 2	-	VID2	Vendor ID	R	-	-	0
Bit 1	-	VID1	Vendor ID	R	001 = ICS	-	0
Bit 0	-	VID0	Vendor ID	R	-	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: WD Time Control Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDEN	Watchdog Alarm Enable (Hard alarm only)	RW	Disable	Enable	0
Bit 6	-	WDSSEN	Watchdog Soft Alarm Enable (Hard and Soft alarm)	RW	Disable	Enable	0
Bit 5	-	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	x
Bit 4	-	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	x
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: M/N Programming & WD Safe Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	PLL1 M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	WD Safe Freq Source	WD Safe Freq Source	RW	B10b(4:0)	Latch Inputs	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: PLL1 Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: PLL1 Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $14.318 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PLL2		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PLL2		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: Programmable Output Divider Register

Byte 19		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-		CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-		CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-		CPUDiv0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X
Bit 3	-		PCIEXDiv3	PCIEX Divider Ratio Programming Bits for Sync mode	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-		PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-		PCIEXDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-		PCIEXDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Programmable Output Divider Register

Byte 20		Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-		3V66/PCIDiv3	3V66/PCI Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-		3V66/PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-		3V66/PCIDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-		3V66/PCIDiv0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X
Bit 3	-		PCIEXDiv3	PCIEX Divider Ratio Programming Bits for Async PLL2 mode	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-		PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-		PCIEXDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-		PCIEXDiv0		RW	0011:/15	0111:/30	1011:/60	1111:/120	X

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

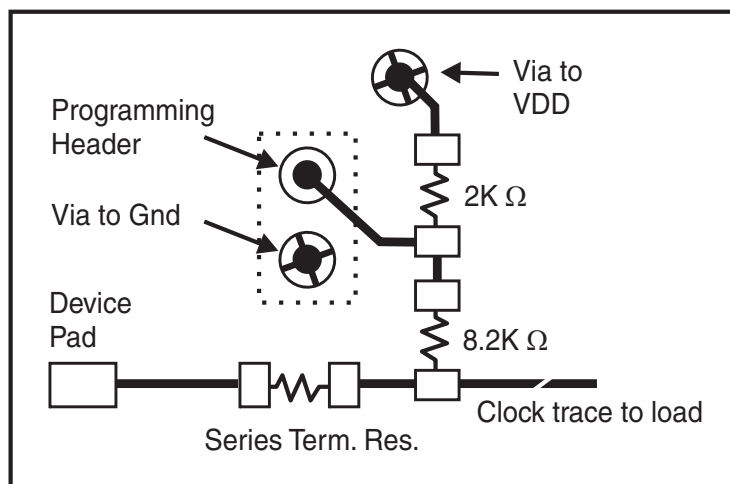


Fig. 1

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			$V_{DD} + 0.5V$	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		$V_{DD} + 0.5V$	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		$V_{DD} + 0.3$	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	$V_{SS} - 0.3$		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	$V_{IN} = 0V$; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	$V_{IN} = 0V$; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		$V_{DD} + 0.3$	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	$V_{SS} - 0.3$		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, $C_L =$ Full load;			350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	$V_{DD} = 3.3V$		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at $V_{OL} = 0.4V$	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

² Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T _{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t _r	V _{OL} = 0.175V, V _{OH} = 0.525V	175		700	ps	1
Fall Time	t _f	V _{OH} = 0.525V V _{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t _r	V _{OL} = 0.175V, V _{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t _f	V _{OH} = 0.525V V _{OL} = 0.175V			125	ps	1
Duty Cycle	d _{t3}	Measurement from differential waveform	45		55	%	1
Skew	t _{sk3}	CPU(1:0), V _T = 50%			100	ps	1
Skew	t _{sk4}	CPU(1:0) to CPU2_ITP, V _T = 50%			150	ps	1
Jitter, Cycle to cycle	t _{jcy-cyc}	Measurement from differential waveform (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	t _{jcy-cyc}	Measurement from differential waveform, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 2pF, R_S = 33.2Ω, R_P = 49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O = 50Ω.

Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Z _o	V _O = V _x	3000			Ω	1
Voltage High	V _{High}	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	V _{Low}		-150		150	mV	1,3
Max Voltage	V _{ovs}	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	V _{uds}		-300			mV	1
Crossing Voltage (abs)	V _{x(abs)}		250		550	mV	1
Crossing Voltage (var)	d-V _x	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see T _{period} min-max values	-300		300	ppm	1,2
Average period	T _{period}	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T _{absmin}	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t _r	V _{OL} = 0.175V, V _{OH} = 0.525V	175		700	ps	1
Fall Time	t _f	V _{OH} = 0.525V V _{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t _r	V _{OL} = 0.175V, V _{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t _f	V _{OH} = 0.525V V _{OL} = 0.175V			125	ps	1
Duty Cycle	d _{t3}	Measurement from differential waveform	45		55	%	1
Skew	t _{sk3}	V _T = 50%			250	ps	1
Jitter, Cycle to cycle	t _{jyc-cyc}	Measurement from differential waveform			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

³I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	V _O = V _{DD} *(0.5)	12		55	Ω	1
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-33			mA	1
		V _{OH} @ MAX = 3.135 V			-33	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	30			mA	1
		V _{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	t _{slew/rf}	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t _r	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t _f	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	t _{jyc-cyc}	V _T = 1.5 V			500	ps	1

*T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, C_L = 20 pF with R_S = 7Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see T _{period} min-max values	-100		100	ppm	1
Clock period	T _{period}	48.00MHz output nominal	20.8313		20.8354	ns	
Output Impedance	R _{DSP}	V _O = V _{DD} *(0.5)	12		55	Ω	1
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-33			mA	1
		V _{OH} @ MAX = 3.135 V			-33	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	30			mA	1
		V _{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	t _{slewr/f}	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t _{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t _r	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t _f	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t _{r_USB}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	1		2	ns	1
Fall Time	t _{f_USB}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	t _{jyc-cyc}	V _T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - AGPCLK/3V66

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	V _O = V _{DD} *(0.5)	12		55	Ω	1
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-33			mA	1
		V _{OH} @ MAX = 3.135 V			-33	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	30			mA	1
		V _{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t _r	V _{OL} = 0.4 V, V _{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t _f	V _{OH} = 2.4 V, V _{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Group Skew	t _{skew}	V _T = 1.5 V			150	ps	1
Jitter, Cycle to cycle	t _{jyc-cyc}	V _T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 10-30 pF (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

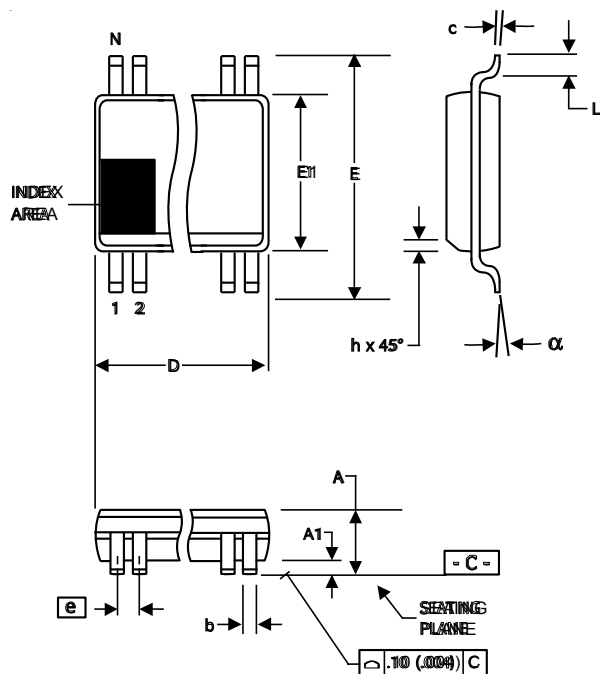
Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.4	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V, V _{OH} @ MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V, @ MAX = 0.4 V	29		27	mA	1
Edge Rate	t _{slew/rf}	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t _{r1}	V _{OL} = 0.4 V, V _{OH} = 2.4 V	1		2	ns	1
Fall Time	t _{f1}	V _{OH} = 2.4 V, V _{OL} = 0.4 V	1		2	ns	1
Skew	t _{sk1}	V _T = 1.5 V			500	ps	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45		55	%	1
Jitter	t _{jyc-cyc}	V _T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

953008yFLFT

Example:

XXXX y F L F T

Designation for tape and reel packaging

RoHS Compliant

Package Type

F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.