Low Cost DDR Phase Lock Loop Clock Driver

Recommended Application:
DDR Clock Driver

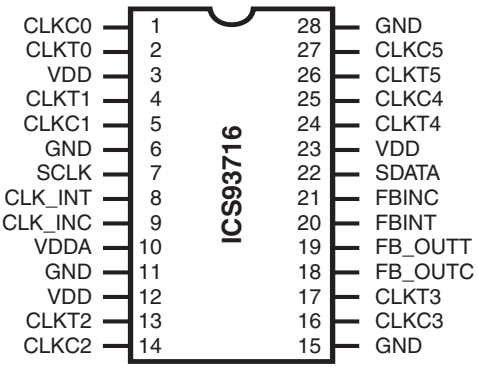
Product Description/Features:

- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- **Bypass mode on B revision only**

Switching Characteristics:

- PEAK - PEAK jitter (66MHz): <75ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 550ps - 950ps

Pin Configuration

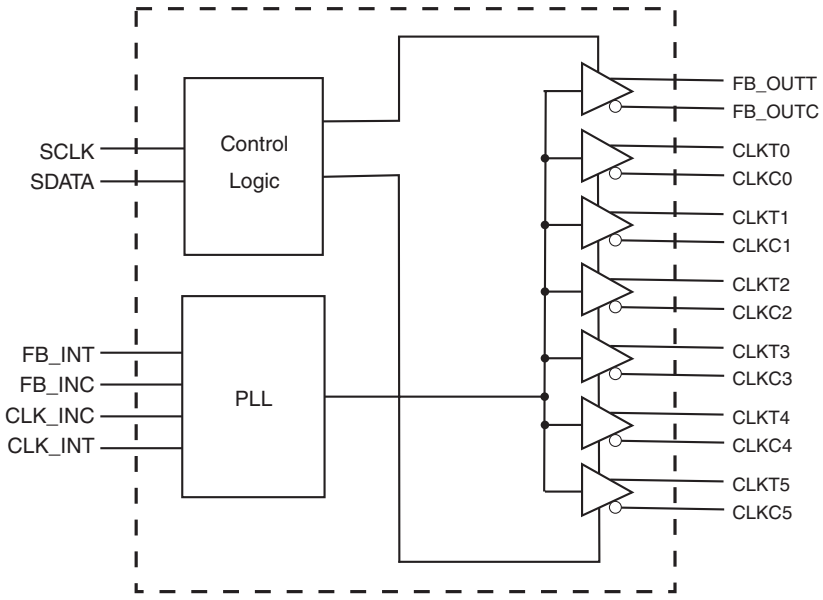


28-Pin SSOP and TSSOP

Functionality

INPUTS			OUTPUTS				PLL State
AVDD	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
2.5V (nom)	L	H	L	H	L	H	on
2.5V (nom)	H	L	H	L	H	L	on
2.5V (nom)	<20MHz		Z	Z	Z	Z	off
GND	L	H	L	H	L	H	Bypassed/off
GND	H	L	H	L	H	L	Bypassed/off

Block Diagram



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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
6, 11, 15, 28	GND	PWR	Ground
27, 25, 16, 14, 5, 1	CLKC(5:0)	OUT	"Complementary" clocks of differential pair outputs.
26, 24, 17, 13, 4, 2	CLKT(5:0)	OUT	"True" Clock of differential pair outputs.
3, 12, 23	VDD	PWR	Power supply 2.5V
7	SCLK	IN	Clock input of I^2C input, 5V tolerant input
8	CLK_INT	IN	"True" reference clock input
9	CLK_INC	IN	"Complementary" reference clock input
10	VDDA	PWR	Analog power supply, 2.5V
18	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
19	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
20	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
21	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
22	SDATA	IN	Data input for I^2C serial input, 5V tolerant input

Byte 0: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	2, 1	1	CLKT0, CLKC0
Bit 6	4, 5	1	CLKT1, CLKC1
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	13, 14	1	CLKT2, CLKC2
Bit 2	26, 27	1	CLKT5, CLKC5
Bit 1	-	1	Reserved
Bit 0	24, 25	1	CLKT4, CLKC4

Byte 1: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	17, 16	1	CLKT3, CLKC3
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Byte 2: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Byte 3: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Byte 4: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Byte 5: Reserved
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND - 0.5V to V_{DD} + 0.5V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V, R_L = 120Ω, C_L=15pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	V_I = V_{DD} or GND	5			µA
Input Low Current	I_{IL}	V_I = V_{DD} or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	R_L = 120Ω, C_L = 0pf @ 170MHz		250	350	mA
	I_{DDPD}	C_L = 0pf		65	90	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -1 mA	V_{DD} - 0.1			V
		I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	I_{OL}=1 mA			0.1	V
		I_{OL}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		3		pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}		3		pF

[1]Guaranteed by design at 233MHz, not 100% tested in production.

DC Electrical Characteristics (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INC, FB_INT		0.4	V_{DD}/2 - 0.18	V
		SCLK, SDATA	-0.3		0.7	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INC, FB_INT	V_{DD}/2 + 0.18	2.1		V
		SCLK, SDATA	1.7		5	V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.36		V_{DD} + 0.6	V
		AC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.7		V_{DD} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.2	V_{DD}/2	V_{DD}/2 + 0.2	V
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, V_{OUT}=V_{DD} or GND		0.1	±5	µA
Operating free-air temperature	T_A		0		85	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC excursion of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal crosses.

Timing Requirements

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V, R_L = 120Ω, C_L=15pF (unless otherwise

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency[3]	$freq_{op}$		33	233	MHz
Application Frequency Range[3]	$freq_{App}$		60	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			100	µs

Switching Characteristics

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V, R_L = 120 , C_L=15pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PHL}[1]	CLK_IN to any output		5.5		ns
Duty Cycle	DC		49		51	%
Input clock slew rate	$t_{sl(I)}$		1		4	v/ns
Cycle to Cycle Jitter[1]	t_{cyc}-t_{cyc}	100MHz < f < 170MHz		50	65	ps
Cycle to Cycle Jitter[1]	t_{cyc}-t_{cyc}	f=66MHz		72	75	ps
Phase error	$t_{(phase\ error)}$[4]		-150	0	150	ps
Output to Output Skew	t_{skew}			75	100	ps
Rise Time, Fall Time	t_r, t_f	See figure 8	550		950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{WH}/t_c, were the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

Parameter Measurement Information

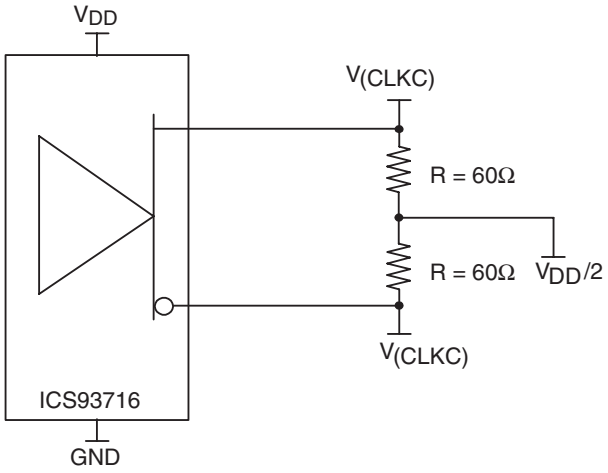
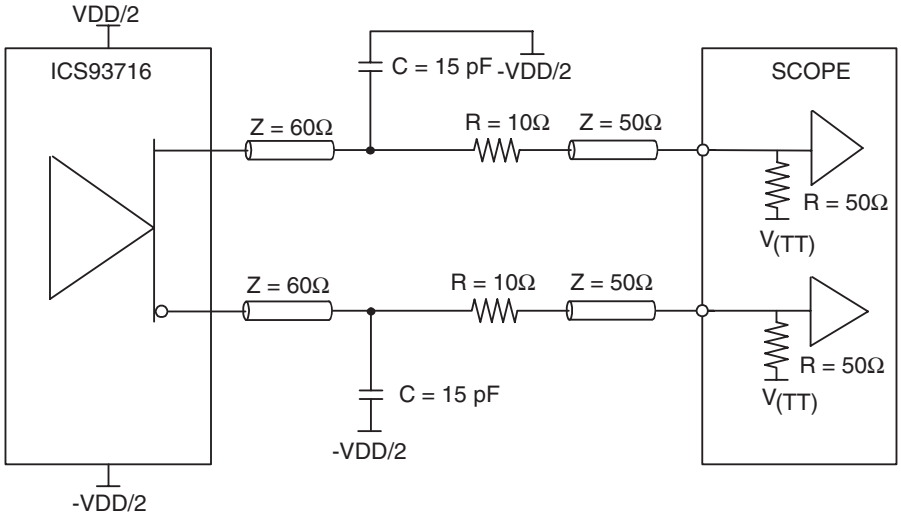
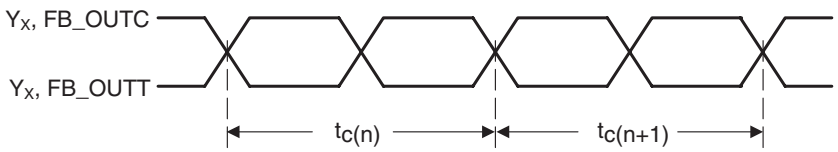


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

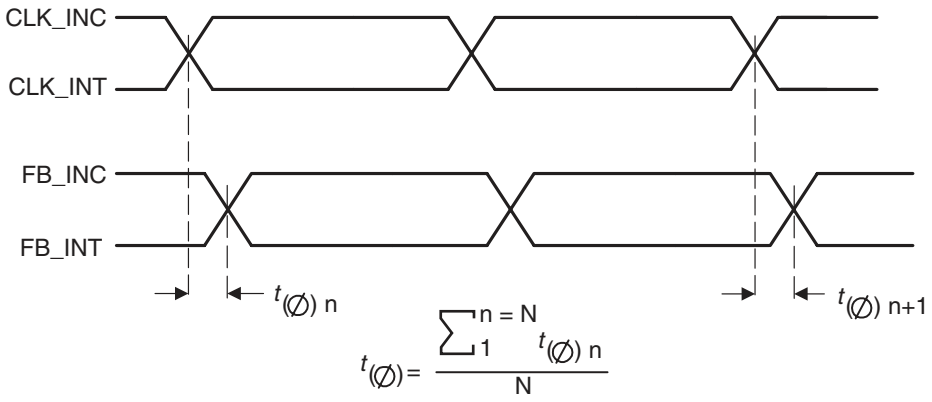


Figure 4. Static Phase Offset

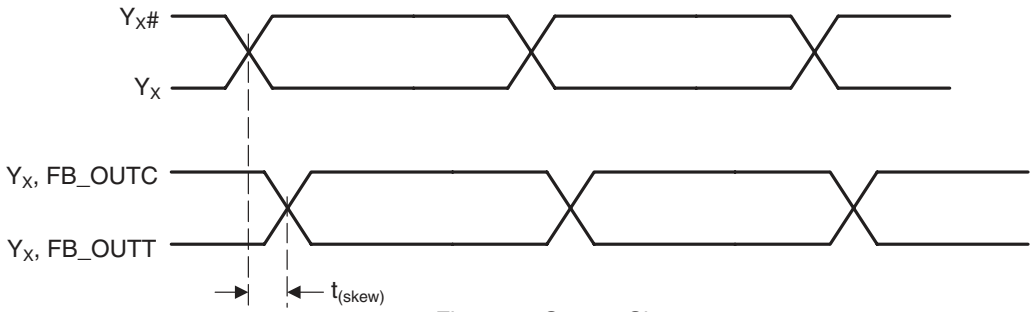


Figure 5. Output Skew

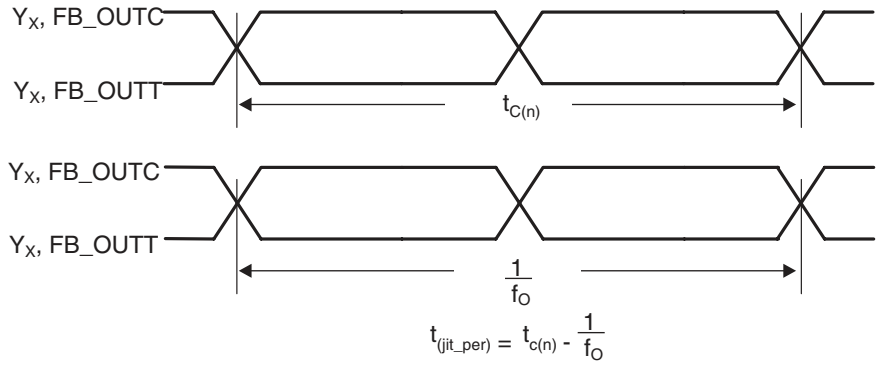


Figure 6. Period Jitter

Parameter Measurement Information

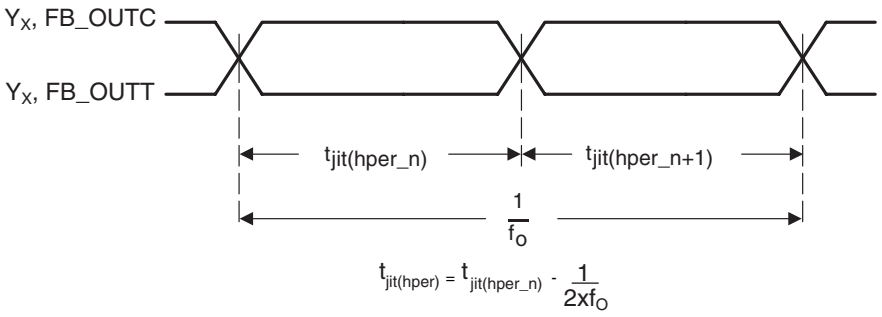


Figure 7. Half-Period Jitter

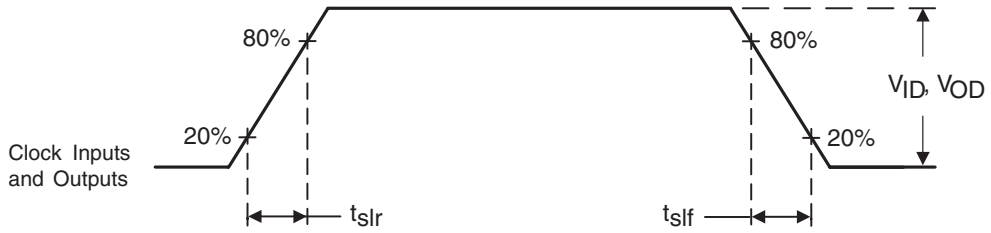


Figure 8. Input and Output Slew Rates

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

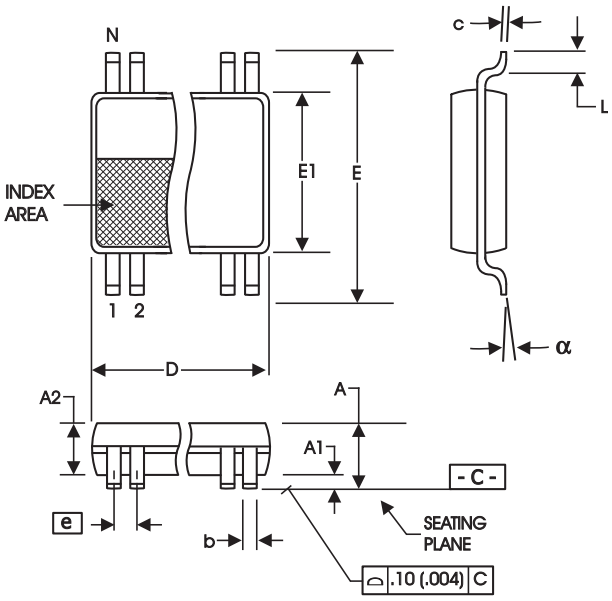
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

Ordering Information

93716yFLF-T

Example:

XXXXX y F LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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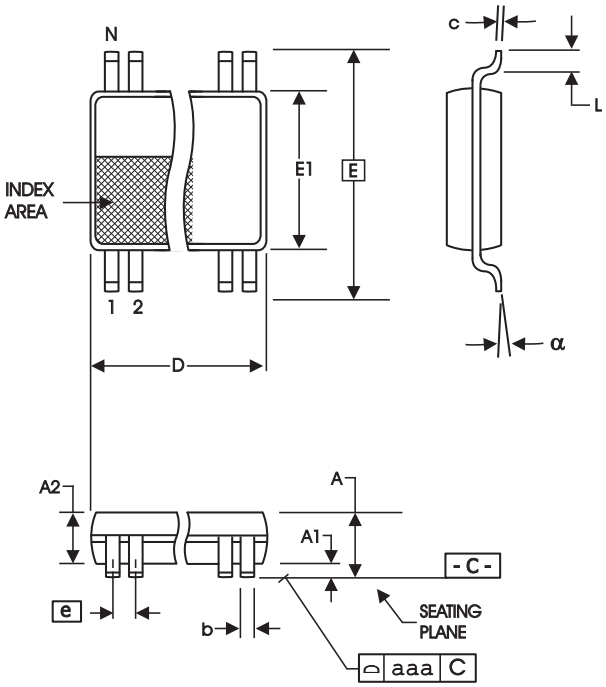

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.65 mm. pitch TSSOP
(240 mil) (25.6 mil)

Ordering Information

93716yGLF-T

Example:

XXXXX y GLF - T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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Revision History

Rev.	Issue Date	Description	Page #
H	9/10/2008	Updated Product Description/Features	1

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