Description

The IDT8S89873I is a high speed Differential-to-LVDS Buffer/Divider with Internal Termination. The IDT8S89873I has a selectable ÷2, ÷4, ÷8, ÷16 output dividers. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components.

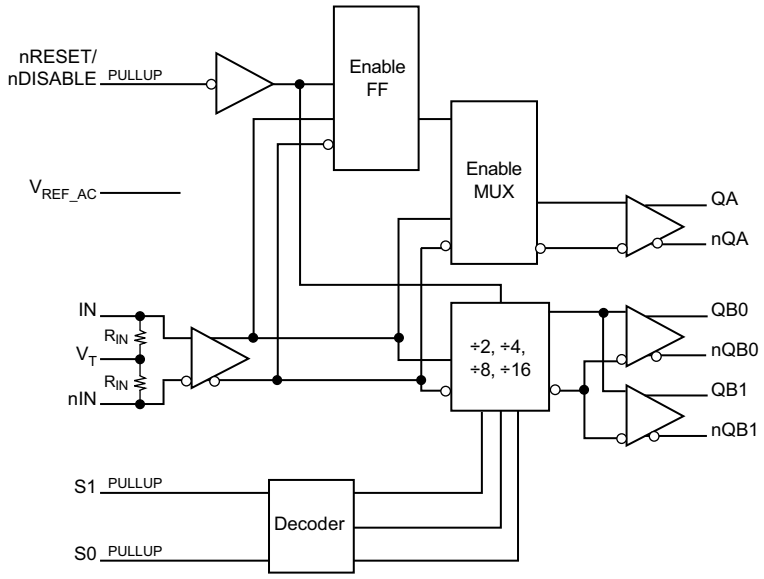
The nRESET/nDISABLE asynchronously resets the QB output bank. QA outputs are synchronously enabled or disabled on the next falling edge of IN, or rising edge of nIN. Please refer to the timing diagram for details.

The device is packaged in a small, 3 x 3 mm VFQFN package, making it ideal for use on space-constrained boards.

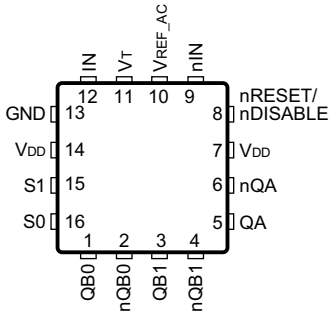
Features

- Three LVDS outputs
- Frequency divide select options: ÷2, ÷4, ÷8, ÷16
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz (maximum) in pass-through mode
- Additive phase jitter: 0.185ps (typical) RMS
- Output skew: 9ps (typical), QBx, nQBx outputs
- Propagation Delay: 540ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



IDT8S89873I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
NL Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVDS interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVDS interface levels.
5, 6	QA, nQA	Output		Differential output pair. LVDS interface levels.
7, 14	V_{DD}	Power		Power supply pins.
8	nRESET/ nDISABLE	Input	Pullup	Output reset and enable/disable pin. When LOW, resets the divider select, and align Bank A and Bank B edges. In addition, when LOW, Bank A and Bank B will be disabled. Input threshold is V_{DD}/2V. Includes an internal 37kΩ pull-up resistor. LVTTL/LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. R_{IN} = 50Ω termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. Equal to V_{DD} – 1.4V (approx.).
11	V_T	Input		Termination input.
12	IN	Input		Non-inverting LVPECL differential clock input. R_{IN} = 50Ω termination to V_T.
13	GND	Power		Power supply ground.
15, 16	S1, S0	Input	Pullup	Select pins. Logic HIGH if left unconnected (÷16 mode). S0 = LSB. Input threshold is V_{DD}/2. 37kΩ internal pull-up resistor. LVCMOS/LVTTL interface levels.

NOTE: *Pull-up* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ
C_{IN}	Input Capacitance			2		pF

Function Tables

Table 3. Truth Table

Inputs			Outputs	
nRESET/nDISABLE	**S1**	**S0**	**Bank A**	**Bank B**
1 (default)	0	0	Input Clock	Input Clock ÷2
1	0	1	Input Clock	Input Clock ÷4
1	1	0	Input Clock	Input Clock ÷8
1	1 (default)	1 (default)	Input Clock	Input Clock ÷16
0	X	X	QA = LOW, nQA = HIGH; NOTE 1	QBx = LOW, nQBx = HIGH; NOTE 2

NOTE 1: On the next negative transition of the input signal.
NOTE 2: Asynchronous reset/disable function.

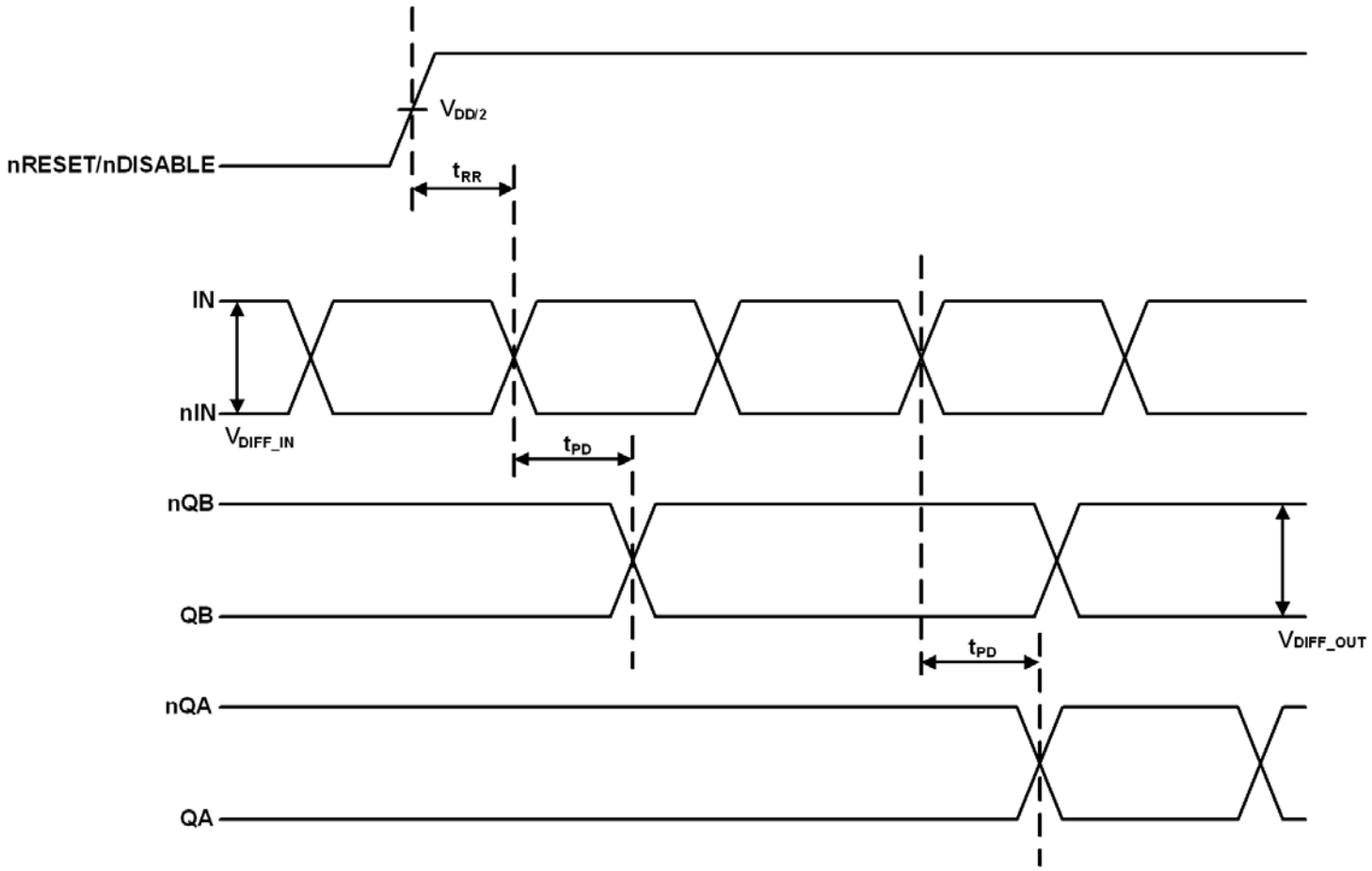


Figure 1. nRESET/nDISABLE Timing Diagram

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
V_{REF_AC} Input Sink/Source, I_{REF_AC}	±2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				100	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			0		0.8	V
I_{IH}	Input High Current	S[1:0], nRESET/nDISABLE	V_{DD} = V_{IN} = 3.6V			10	µA
I_{IL}	Input Low Current	S[1:0], nRESET/nDISABLE	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN, nIN	IN to V_T, nIN to V_T		50		Ω
V_{IH}	Input High Voltage	IN, nIN		0.15		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	IN, nIN		0		V_{DD} – 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.4	V
V_{REF_AC}	Bias Voltage			V_{DD} – 1.4	V_{DD} – 1.425	V_{DD} – 1.34	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing* diagram.
NOTE 2: Guaranteed by design.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OUT}	Output Voltage Swing		370	470	570	mV
V_{OH}	Output High Voltage		1.366	1.500	1.690	V
V_{OL}	Output Low Voltage		0.860	1.040	1.226	V
V_{OCM}	Output Common Mode Voltage		1.125	1.27	1.400	V
ΔV_{OCM}	Change in Common Mode Voltage				50	mV

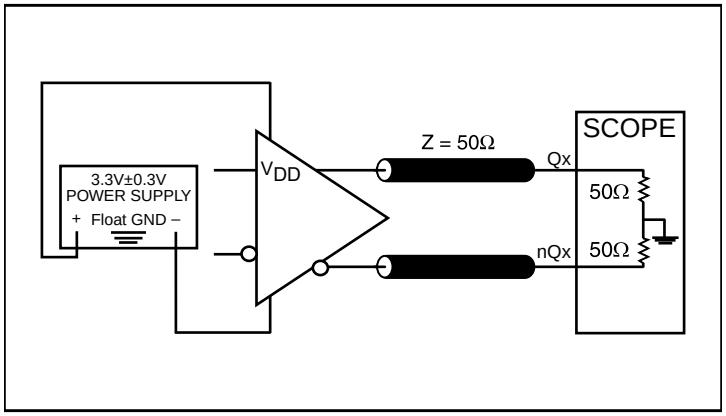
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C

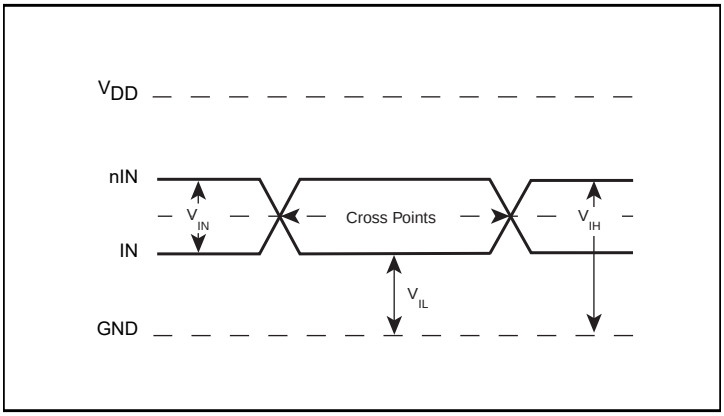
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency; NOTE 5		Output Swing ≥ 200mV			2	GHz
t_{PD}	Propagation Delay; NOTE 1	IN-to-Q	Input Swing: <400mV	430	525	640	ps
			Input Swing: ≥400mV	420	510	620	ps
*t*sk(o)	Output Skew; NOTE 2, 3	QB0-to-QB1			9	40	ps
		QA-to-QBx			12	30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					250	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section; NOTE 5		156.25MHz, Integration Range: 12kHz - 20MHz		0.185	0.220	ps
t_{RR}	Reset Recovery Time			600			ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	45	125	285	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at ≤ 2GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Device is in pass-through mode.

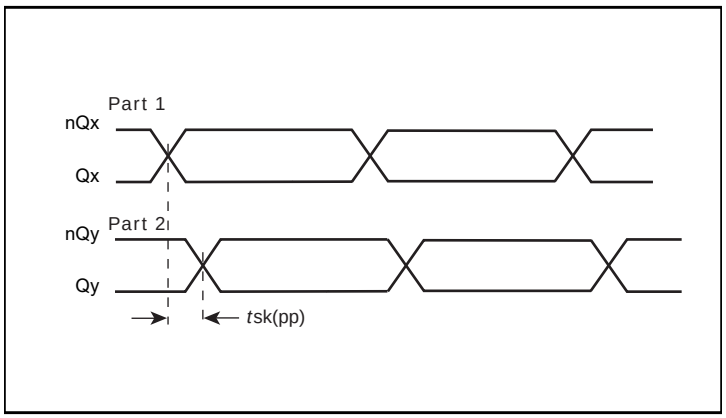
Parameter Measurement Information



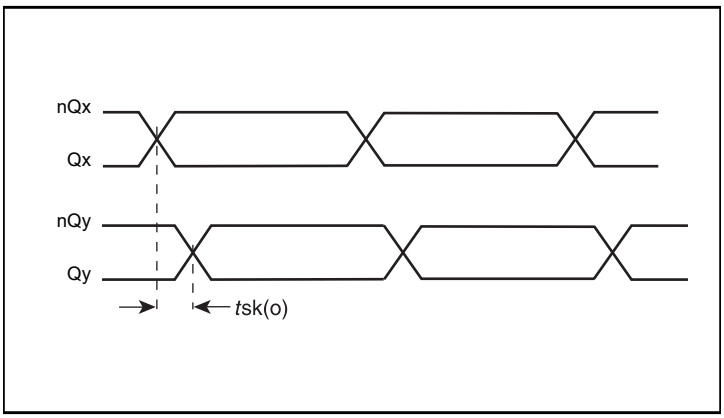
Output Load AC Test Circuit



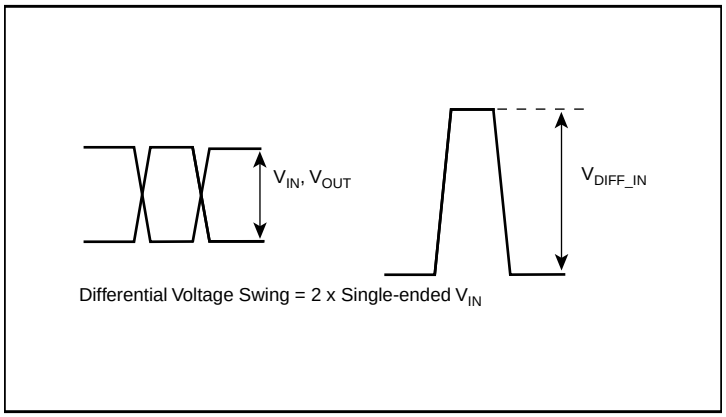
Differential Input Level



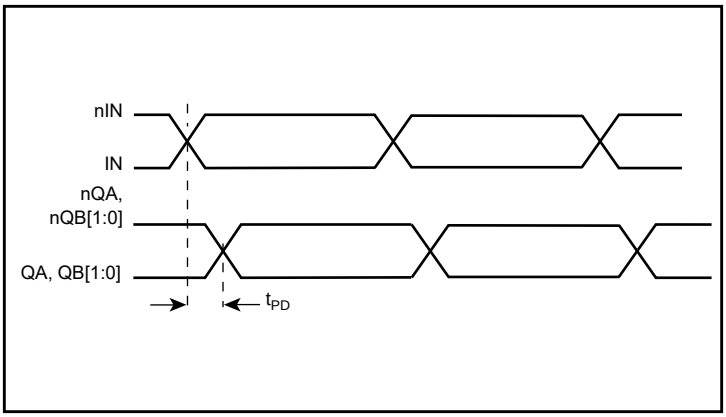
Part-to-Part Skew



Output Skew

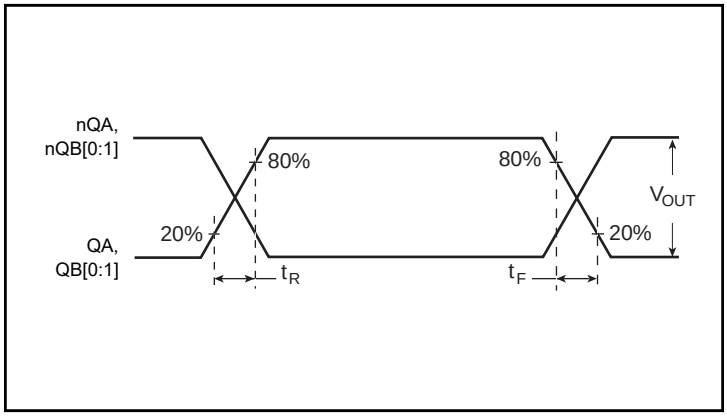


Single-Ended & Differential Voltage Swing

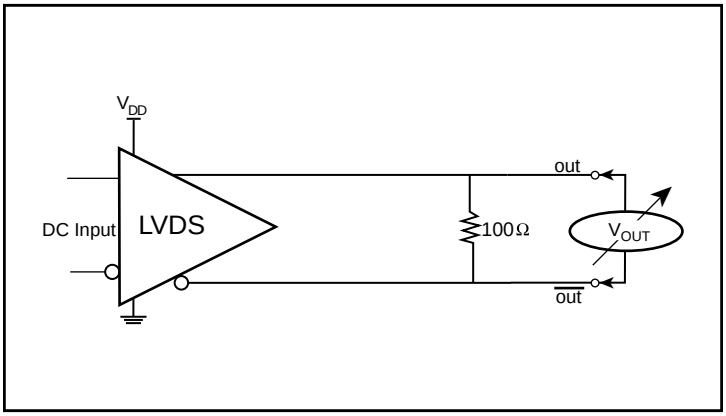


Propagation Delay

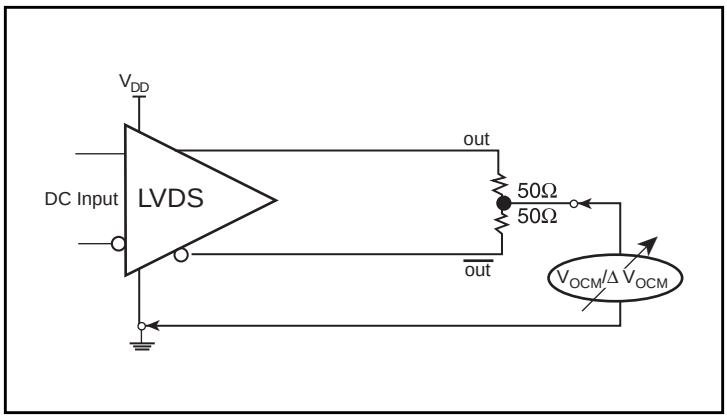
Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

3.3V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

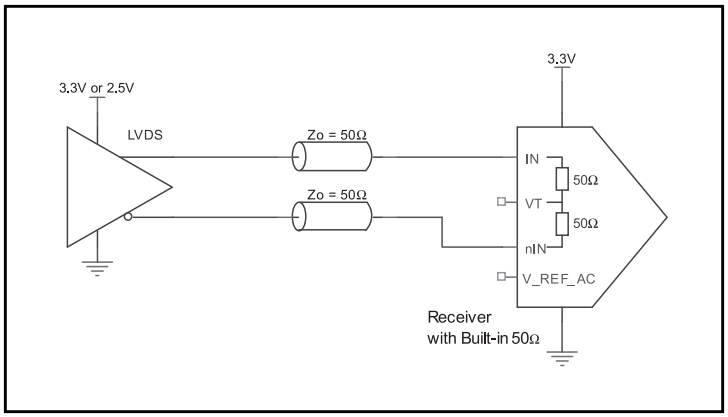


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

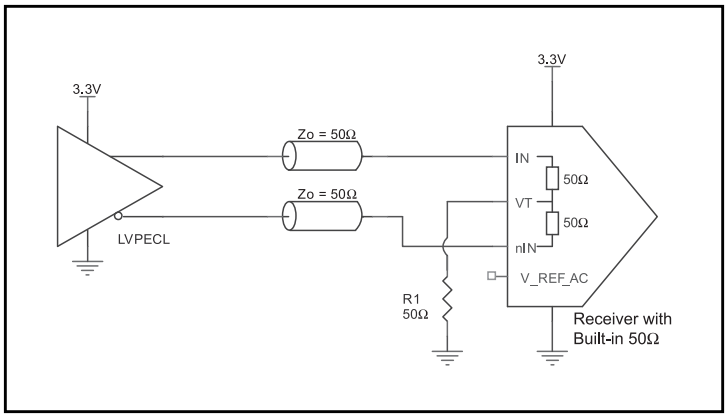


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

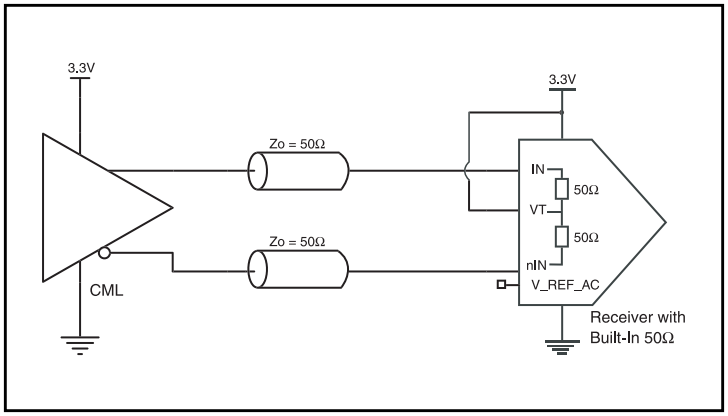


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

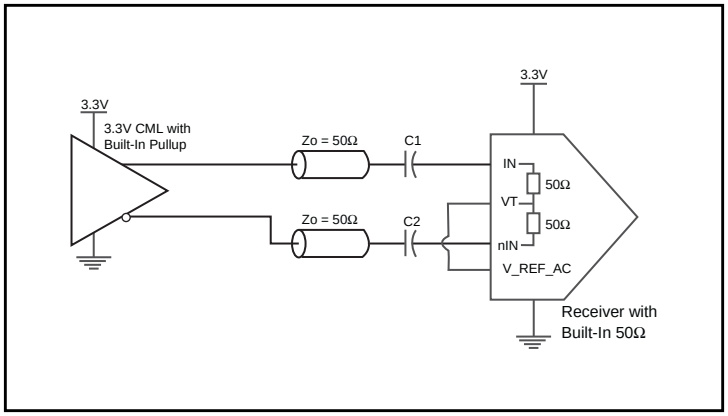


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

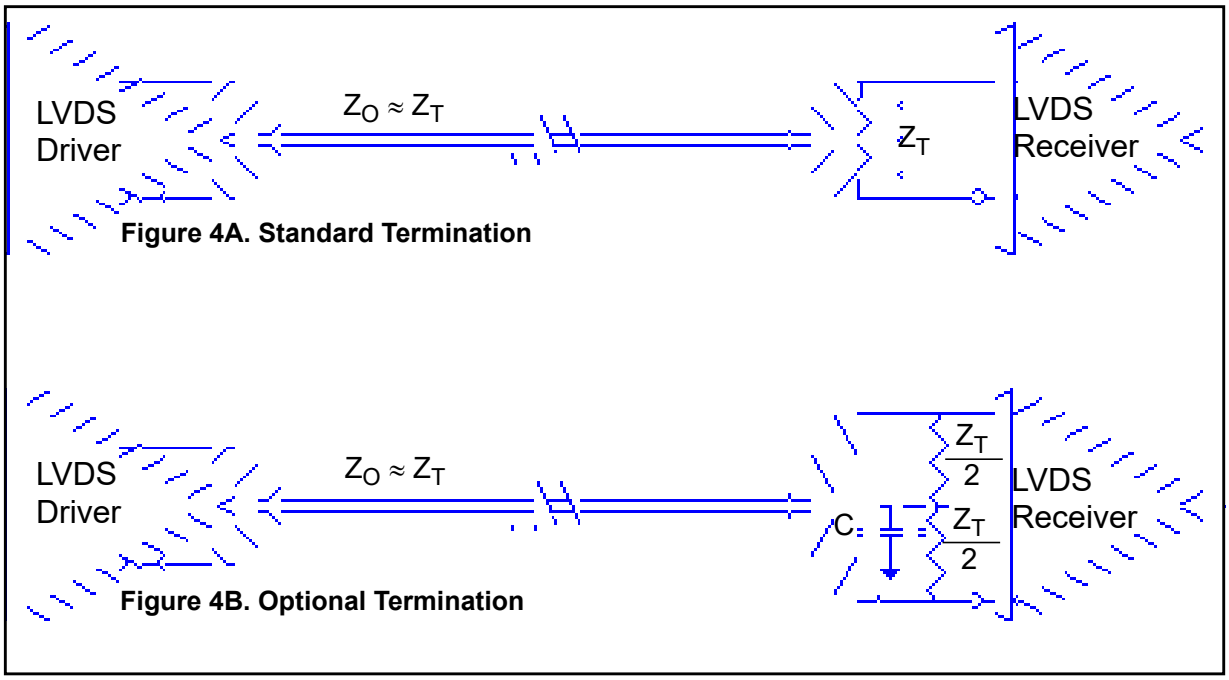


Figure 4A. Standard Termination

Figure 4B. Optional Termination

LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

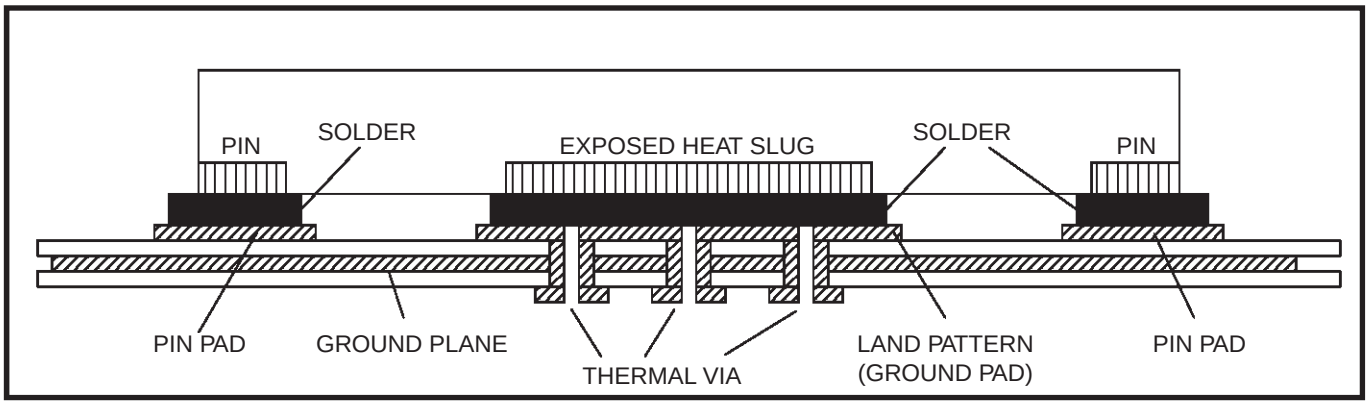


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8S89873I.
Equations and example calculations are also provided.

The maximum current at 85°C is as follows

I_{DD_MAX} = 96.32mA

1. Power Dissipation.

The total power dissipation for the IDT8S89873I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.6V * 100mA = **360mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX}$ = $(V_{IN\_MAX})^2$ / R_{T_MIN} = $(1.2V)^2$ / 80Ω = **18mW**

Total Power$_{_MAX}$ = 360mW + 18mW = **378mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.378W * 74.7°C/W = 113.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for IDT8S89873I is: 415
Pin compatible with ICS889873

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

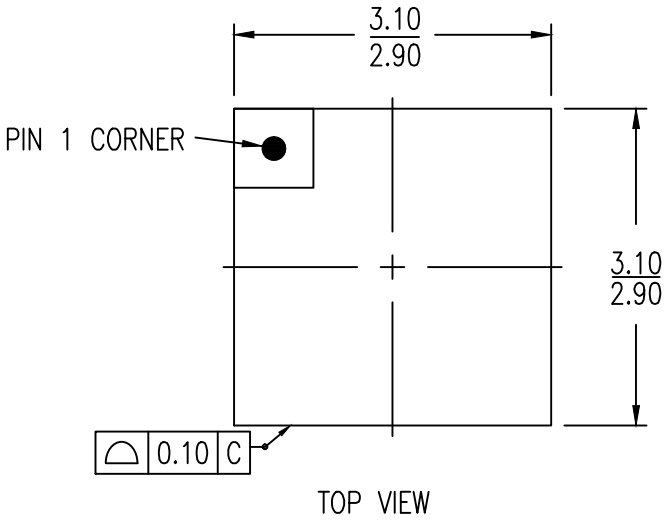
Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89873ANLGI	873AI	“Lead-Free” 16 Lead VFQFN	Tray	-40°C to 85°C
8S89873ANLGI8	873AI	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

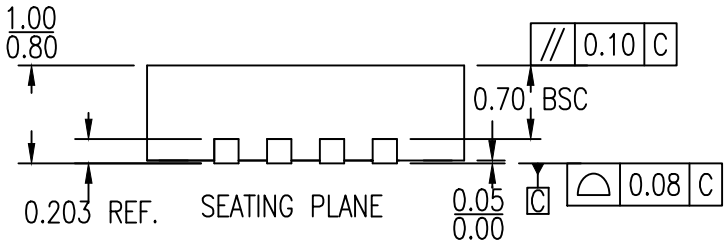
NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

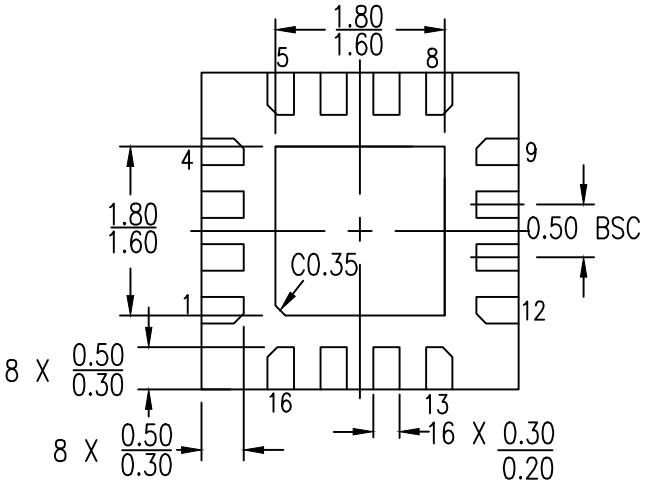
Revision Date	Description of Change
November 29, 2017	Updated the package outline drawings; however, no technical changes Completed other minor changes
July 10, 2012	Initial release.



TOP VIEW

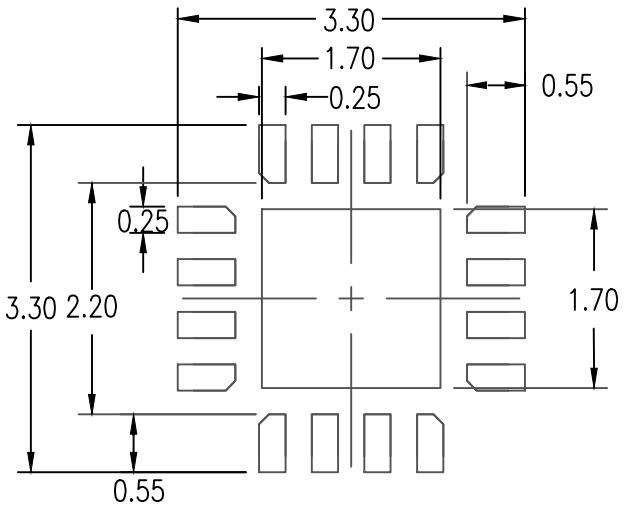


SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Aug 15, 2017	Rev 03	Update Epad Range

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