Overview

This datasheet addendum is to be used in conjunction with the overall 8A34001 datasheet. This addendum indicates the register settings that are pre-configured in the internal One-Time Programmable (OTP) memory of the device by IDT. These register settings represent the default values the registers will take on power-up or reset. Values may be changed at any time afterwards over the serial port, but any such changes will be lost when the device is reset or power-cycled unless programmed into OTP as an additional or replacement configuration.

In addition, there are several other pieces of documentation that describe specific functions or details not covered this document. Table 1 shows related documents.

Table 1. Related Documentation for 8A34001

Document Title	Document Description
8A34001 Datasheet	Contains a functional overview of the device and hardware-design related details including pinouts, AC and DC specifications and applications information related to power filtering and terminations.
8A34046E-001 Datasheet Addendum (this document)	Indicated pre-programmed power-up / reset configurations of this specific ‘dash code’ part number.
8A3xxxx Family Programming Guide	Contains detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.
Evaluation Board Reference Manual	Describes the Evaluation Board. Evaluation boards are available for the 8A34001 (144BGA) or 8A34002 (72QFN) devices. These devices contain a superset of the functionality available in all other members of the 8A3xxxx Family. So they can serve as evaluation tools for any of the less fully-featured family members.
Timing Commander Personality User Manual	Detailed description of how to use IDT’s Timing Commander configuration tool. At this time, a personality file is only available for 8A34001. This personality contains a superset of the functionality available in all other members of the 8A3xxxx family. Since all members of the 8A3xxxx family share register locations and resource numbering, configurations generated using the 8A34001 personality can be used in any member of the 8A3xxxx family. Functionality that is not available on the other family members will of course not respond to any configuration of it that is made.

Device Information Block Contents

GPIO Usage at Reset

GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7
OTP Configuration Selection	OTP Configuration Selection	OTP Configuration Selection	OTP Configuration Selection	Unused[a]	Unused[a]	Unused[a]	Unused[a]

GPIO8	GPIO9	GPIO10 (not bonded out)	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15
Unused[a]	SPI/I2C Selection	EEPROM Load disable	Unused[a]	Unused[a]	Unused[a]	Unused[a]	Unused[a]

[a] Left unused to avoid conflicts with JTAG port accesses while in nTEST mode.

Analog Voltage Used on VDDA_BG, VDDA_LC, VDDA_PDCP and VDDA_XTAL

Voltage Level used on VDDA_BG and VDDA_LC Supplies[a]	Voltage Level used on VDDA_PDCP and VDDA_XTAL Supplies[a]
3.3V	3.3V

[a] Used during device reset period to set regulator parameters for fastest startup time. Can be changed later via register accesses or in configuration data, but that will result in extended startup time while re-calibration occurs.

Device Initial Configuration Information for Configuration 0

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 1

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 2

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 3

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 4

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 5

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 6

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 7

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 8

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 9

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 10

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 11

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 12

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 13

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 14

Present as blank configuration to ensure correct location for Configuration 15.

Device Initial Configuration Information for Configuration 15

Serial Port Mode Main	Serial Port Aux
Selected by GPIO9 58h (7b base I^2C address)	Selected by GPIO9 58h (7b base I^2C address)

Inputs

Crystal Frequency (MHz)	XO_DPLL Input (MHz)	CLK0 (MHz)	CLK1 (MHz)	CLK2 (MHz)	CLK3 (MHz)	CLK8 (MHz)	CLK9 (MHz)	CLK10 (MHz)	CLK11 (MHz)
54	10	25	10	12.5	OFF	25	—	1PPS	—

Outputs

Output	Frequency (MHz)	Type	Enable	Source	Divider	VDDO_Q
Q0	156.25	LVPECL 3.3V	Enabled	DPLL0	4	3.3
Q1	OFF	Disabled	Disabled	DPLL0	50	1.8
Q2	10	CMOS	Enabled	DPLL1	50	3.3
Q3	OFF	Disabled	Disabled	DPLL1	1	1.8

Output	Frequency (MHz)	Type	Enable	Source	Divider	VDDO_Q
Q4	50	LVPECL 3.3V	Enabled	DPLL2	10	3.3
Q5	50	LVPECL 3.3V	Enabled	DPLL2	10	3.3
Q6	4kHz	CMOS	Enabled	DPLL3	125000	3.3
Q7	1PPS	CMOS	Enabled	DPLL3	500000000	3.3
Q8	1PPS	CMOS	Enabled	DPLL4	500000000	3.3
Q9	OFF	Disabled	Disabled	DPLL5	60	1.8
Q10	10	CMOS	Enabled	DPLL6	50	3.3
Q11	50	LVPECL 3.3V	Enabled	DPLL7	10	3.3

PLL Channel Configuration

Channel	Mode	Frequency (MHz)	LockBW	Dampening Factor	Primary Source	Reference Selection
System APLL	Synthesizer	13608.0	—	—	Crystal (doubled)	—
System DPLL	Synthesizer	—	—	—	XO	—
DPLL0	G.8262 EEC option 1	625	1200mHz	< 0.2dB	0	Automatic
DPLL1	Jitter Attenuator	500	25Hz	< 0.2dB	2	Automatic
DPLL2	G.8262 EEC option 2	500	100mHz	< 0.2dB	3	Automatic
DPLL3	Synthesizer	500	0µHz	< 0.2dB	3	Automatic
DPLL4	Synthesizer	500	0µHz	< 0.2dB	3	Automatic
DPLL5	Jitter Attenuator	600	25Hz	Overdamp	0	Automatic
DPLL6	Jitter Attenuator	500	25Hz	Overdamp	0	Automatic
DPLL7	Jitter Attenuator	500	25Hz	Overdamp	0	Automatic

GPIOs

	GPIO0	GPIO1	GPIO2	GPIO3
Enabled	False	False	False	False

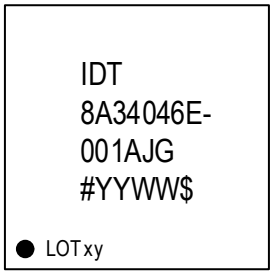
	GPIO4	GPIO5
Enabled Mode Function	True Alert out (out) Alert out (out) (out level: active high	True Lock indicator (out) Lock indicator (out) (SYS DPLL, active hgh)

	GPIO8	GPIO9
Enabled Mode Function	False User control User control (direction: input)	False User control User control (direction: input)

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
8A34046E-001AJG	10 x 10 x 1.2 mm 144-CABGA, 0.8mm ball pitch	3	Tray	-40° to +85°C
8A34046E-001AJG8	10 x 10 x 1.2 mm 144-CABGA, 0.8mm ball pitch	3	Tape and Reel	-40° to +85°C

Marking Diagram



- Line 1 is the part number.
- "-001" denotes dash code.
- "AJG" denotes the package code
- "YYWW" is the last digits of the year and week that the part was assembled.
- "$" denotes mark code.
- "xy" denotes sequential lot number.

Revision History

Revision Date	Description of Change
July 16, 2019	Initial release of the 8A34046E-001 Datasheet Addendum. The configuration was created using Timing Commander Personality 8A34001 v5.1.

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