General Description

The 84330B-03 is a general purpose, dual output high frequency synthesizer. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO and output frequency can be programmed using the I²C interface. The output can be configured to divide the VCO frequency by 1, 2, 3, 4, and 6.

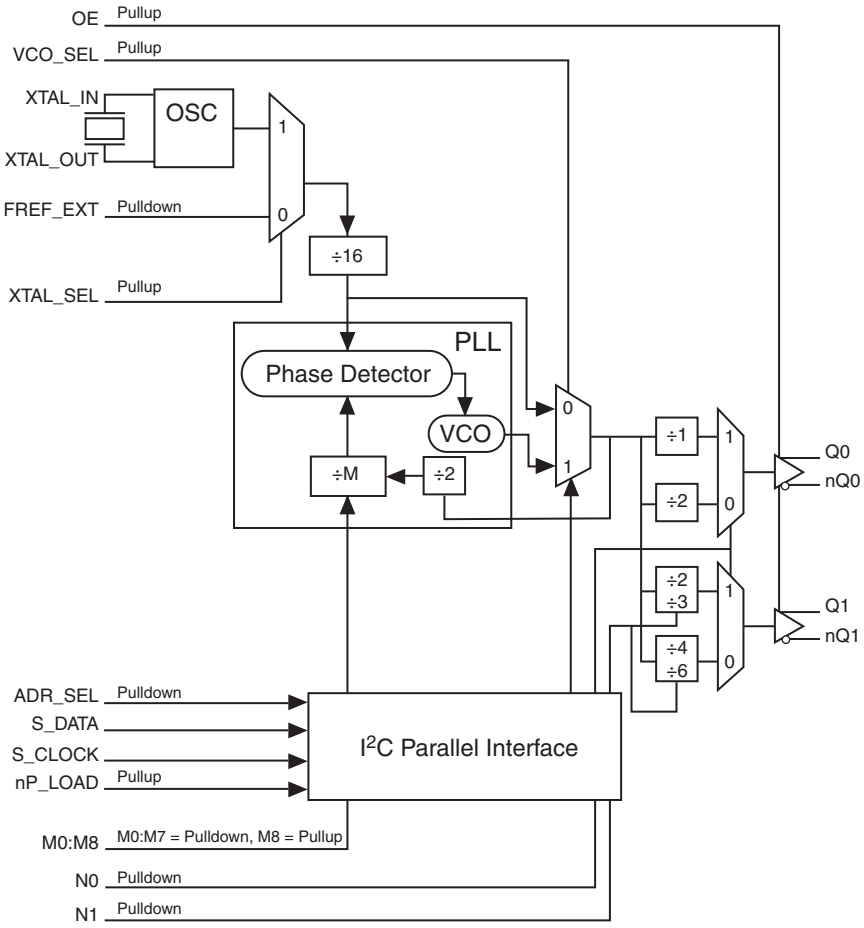
Additionally, the device supports spread spectrum clocking (SSC) for minimizing Electromagnetic Interference (EMI). The low cycle-cycle jitter and broad frequency range of the 84330B-03 make it an ideal clock generator for a variety of demanding applications which require high performance.

Features

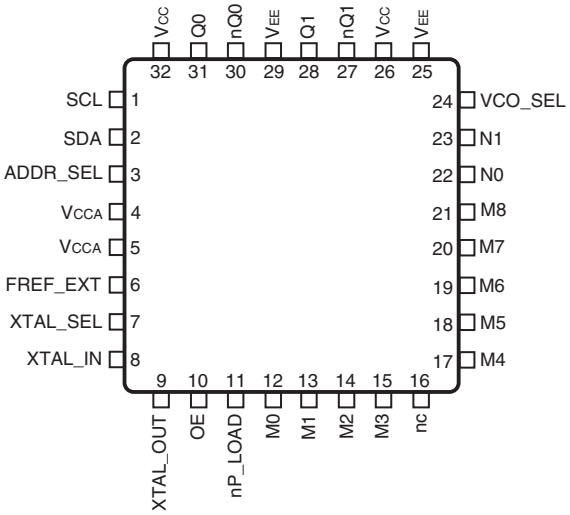
- Fully integrated PLL, no external loop filter requirements
- Two differential 3.3V LVPECL output pairs
- Crystal oscillator interface: 10MHz to 25MHz
- Output frequency range: 41.67MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Parallel or I²C interface for programming M and N dividers during power-up
- Supports Spread Spectrum Clocking (SSC)
  Center spread: selectable ±0.5%, ±1.0%, ±1.5%, ±2%

  Up/Down spread: selectable ±0.5%, ±1.0%, ±1.5%, ±2%, 2.5%, 3.%, 3.5%, 4%
- RMS period jitter: 9ps (maximum)
- Cycle-to-cycle jitter: 40ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



84330B-03
32 Lead LQFP
Y Package
7mm x 7mm x 1.4mm package body
Top View

The 84330B-03 uses either a parallel interface or industry standard I²C interface to control the programming of the internal dividers. The power on defaults are summarized as follows:

	M	Output
Parallel Mode:	256	Q0/nQ0 output at 267MHz (using a 16.667MHz crystal)
SSC Mode:	Off	Q1/nQ1 output at 133MHz (using a 16.667MHz crystal)

The programming mode is controlled by the nP_LOAD pin. When this pin is low, The M, N values are set by the logic values on the M, N pins. If nP_LOAD is HIGH, the M, N dividers can be changed using the I²C serial programming interface.

The I²C control registers are defined below:

Data Byte 0

Control Bit	N1	N0	M8	M7	M6	M5	M4	M3
Power-up Default Value	0	0	1	0	0	0	0	0

Data Byte 1

Control Bit	M2	M1	M0	Not Used	Not Used	Not Used	Not Used	Not Used
Power-up Default Value	0	0	0	X	X	X	X	X

Data Byte 2

Control Bit	Up	Down	SSC5	SSC4	SSC3	SSC2	SSC1	SSC0
Power-up Default Value	0	0	0	0	0	0	0	0

I²C ADDRESSING

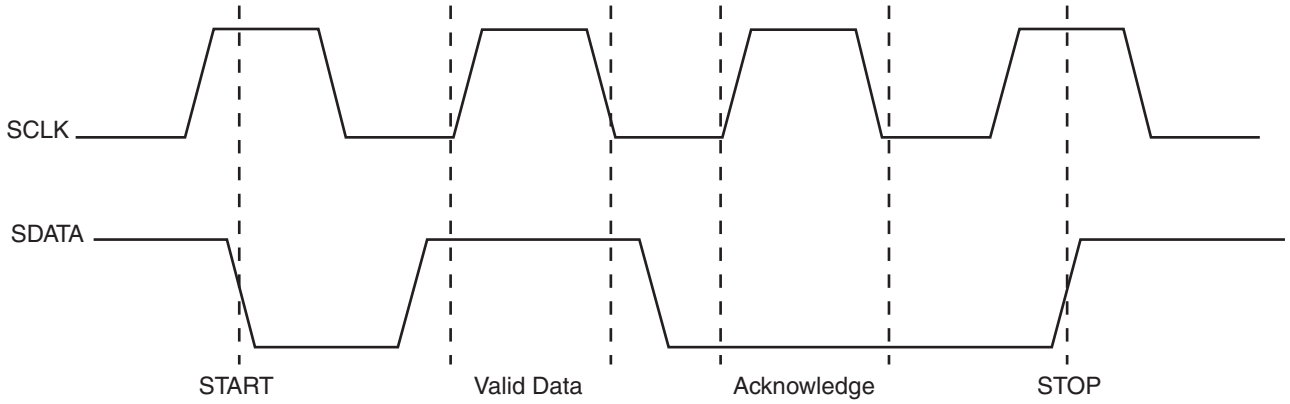
The 84330B-03 can be set to decode one of two addresses to minimize the chance of address conflict on the I²C bus. The address that is decoded is controlled by the setting of the ADDR_SEL pin (pin 3).

ADDR_SEL (pin 3) = 0 Default							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	1	1	0	0	R/W

ADDR_SEL (pin 3) = 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	1	1	1	0	R/W

I²C Interface - Protocol

The 84330B-03 is a slave-only device and uses the standard I²C protocol as shown in the below diagrams. The maximum SCL frequency is greater than 10MHz which is more than sufficient for standard I²C clock speeds.



START (ST) - defined as high-to-low transition on SDA while holding SCL HIGH.

DATA - Between START and STOP cycles, SDA is synchronous with SCL. Data may change only when SCL is LOW and must be stable when SCL is HIGH.

ACKNOWLEDGE (AK) - SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

STOP (SP) - defined as low-to-high transition on SDA while holding SCL HIGH.

I²C Interface - A Write Example

A serial transfer to the 84330B-03 always consists of an address cycle followed by 4 data bytes: 1 dummy byte followed by 3 data bytes. Any additional bytes beyond the 4 data bytes will not be acknowledged and the 84330B-03 will leave the data bus HIGH. These extra bits will not be loaded into the serial control register.

Once the 4 Data bytes are loaded and the master generates a stop condition, the values in the serial control register are latched into the M divider, N divider, and control bits and the device will smoothly slew to the new frequency and any changes to the state of the control bits will take effect.

ST	Slave Address: 7 Bits	R/W	AK
1 Bit	Refer to page 2 for address choices based on ADDR_SEL pin setting	0	0

Dummy Byte 0: 8 Bits								AK
								1 Bit

Data Byte 0: 8 Bits								AK
N1	N0	M8	M7	M6	M5	M4	M3	1 Bit

Data Byte 1: 8 Bits								AK
M2	M1	M0	Not Used	Not Used	Not Used	Not Used	Not Used	1 Bit

Data Byte 2: 8 Bits								AK	SP
Up	Down	SSC5	SSC4	SSC3	SSC2	SSC1	SSC0	1 Bit	1 Bit

Data Byte values latched into control registers here. ↑

Spread Spectrum Operation

NOTE: The functional description that follows used a 16.6667MHz crystal with an M divide value of 160.

Spread Spectrum operation is controlled by I²C Data Byte 2, Spread Spectrum Control Register. Bits SSC0 – SSC5 (SS) of the register are a subtrahend to the M-divider for down-spread, and they are an addend and a subtrahend to the M-divider for center-spread. When the UP bit is HIGH, then up-spread has been selected and the M-divider value will toggle between the programmed M value, and M+SS at a 32kHz rate. When the DN bit is HIGH, then down-spread has been selected and the M-divider value will toggle between the programmed M value, and M-SS at a 32kHz rate. When both the UP and DN bits are HIGH, then center-spread has been selected and the M-divider will toggle between M+SS and M-SS at a 32kHz rate. The table below shows the desired SS value to achieve 0.5%, 1% and 1.5% spread at selected VCO frequencies. To disable Spread Spectrum operation, program both the UP and DN bits to LOW. Spread Spectrum operation will also be disabled when the nP_LOAD input is LOW.

Table 1A. SS Mode Function Table

Register Bits		
SSC7	**SSC6**	**SS Mode**
0	0	Off
0	1	Down-Spread
1	0	Up-Spread
1	1	Center-Spread

Table 1B. Up/Down Spread Configuration

Up- or Down-Spread SS Value						
SSC5	**SSC4**	**SSC3**	**SSC2**	**SSC1**	**SSC0**	**Spread %**
0	0	0	0	0	1	0.50
0	0	0	1	0	0	1.00
0	0	0	1	1	0	1.50
0	0	1	0	0	0	2.00
0	0	1	0	1	0	2.50
0	0	1	1	0	0	3.00
0	0	1	1	1	0	3.50
0	1	0	0	0	0	4.00

Table 1C. Center Spread Configuration

Center-Spread SS Value						
SSC5	**SSC4**	**SSC3**	**SSC2**	**SSC1**	**SSC0**	**Spread (±) %**
0	0	0	0	0	1	0.50
0	0	0	1	0	0	1.00
0	0	0	1	1	0	1.50
0	0	1	0	0	0	2.00

Functional Description

NOTE: The functional description that follows describes operation using a 16.6667MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 7, NOTE 1.

The 84330B-03 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A quartz crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 84330B-03 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and I²C. *Figure 1* shows the timing diagram for parallel mode. In parallel mode the nP_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until an I²C event occurs. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fXTAL}{16} \times 2M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as $120 \leq M \leq 336$. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fXTAL}{16} \times \frac{2M}{N}$$

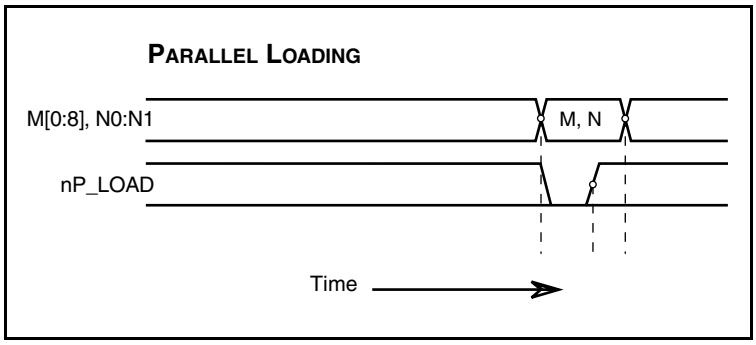


Figure 1. Parallel Load Operations

Table 2. Pin Descriptions

Number	Name	Type		Description
1	SCL	Input	NOTE 1	I²C serial clock input.
2	SDA	Input	NOTE 1	I²C serial data input.
3	ADDR_SEL	Input	Pulldown	Serial address select pin. LVCMOS / LVTTL interface levels.
4, 5	V_{CCA}	Power		Analog supply pin.
6	FREF_EXT	Input	Pulldown	PLL reference input. LVCMOS / LVTTL interface levels.
7	XTAL_SEL	Input	Pullup	Selects between the crystal oscillator or FREF_EXT inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects FREF_EXT when LOW. LVCMOS / LVTTL interface levels.
8, 9	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is an oscillator input, XTAL_OUT is an oscillator output.
10	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels.
11	nP_LOAD	Input	Pullup	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divide value. LVCMOS / LVTTL interface levels.
12, 13, 14, 15, 17, 18, 19, 20	M0, M1, M2 M3, M4, M5 M6, M7	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
21	M8	Input	Pullup	
16	nc	Unused		No connect.
22, 23	N0, N1	Input	Pulldown	Determines N output divider value as defined in Table 4B Function Table. LVCMOS / LVTTL interface levels.
24	VCO_SEL	Input	Pullup	When logic LOW, bypasses PLL. When logic HIGH, PLL is active. LVCMOS/LVTTL interface levels.
25, 29	V_{EE}	Power		Negative supply pins.
26, 32	V_{CC}	Power		Core supply pins.
27, 28	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
30, 31	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.
NOTE 1: Pullup resistor is only active in parallel mode.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 4A. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	120	0	0	1	1	1	1	0	0	0
252	121	0	0	1	1	1	1	0	0	1
254	122	0	0	1	1	1	1	0	1	0
256	123	0	0	1	1	1	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	334	1	0	1	0	0	1	1	1	0
698	335	1	0	1	0	0	1	1	1	1
700	336	1	0	1	0	1	0	0	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 16.6667MHz.

Table 4B. Programmable Output DividerFunction Table

Inputs		Outputs	
N1	N0	Q0/nQ0	Q1/nQ1
0 (default)	0 (default)	÷2	÷4
0	1	÷1	÷2
1	0	÷2	÷6
1	1	÷1	÷3

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.18	3.3	V_{CC}	V
I_{EE}	Power Supply Current				180	mA
I_{CCA}	Analog Supply Current				18	mA

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	M8, OE, nP_LOAD, XTAL_SEL	V_{CC} = V_{IN} = 3.465V			5	µA
		SDA, ADDR_SEL, FREF_EXT, SCL, VCO_SEL, M[0:7], N0, N1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	M8, OE, nP_LOAD, XTAL_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		SDA, ADDR_SEL, FREF_EXT, SCL, VCO_SEL, M[0:7], N0, N1	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 5C. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} -1.4		V_{CC} -0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} -2V.

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Table 7. Input Frequency Characteristics, V_{CC} = 3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL; NOTE 1		10		25	MHz
		SCL				10	MHz
		FREF_EXT; NOTE 2		10			MHz

NOTE 1: For the crystal frequency range, the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz to 700MHz. Using the minimum input frequency of 10MHz, valid values of M are 200 ≤ M ≤ 511. Using the maximum input frequency of 25MHz, valid values of M are 80 ≤ M ≤ 224.
NOTE 2: Maximum frequency on FREF_EXT is dependent on the internal M counter limitations. See Application Information Section for recommendations on optimizing the performance using the FREF_EXT input.

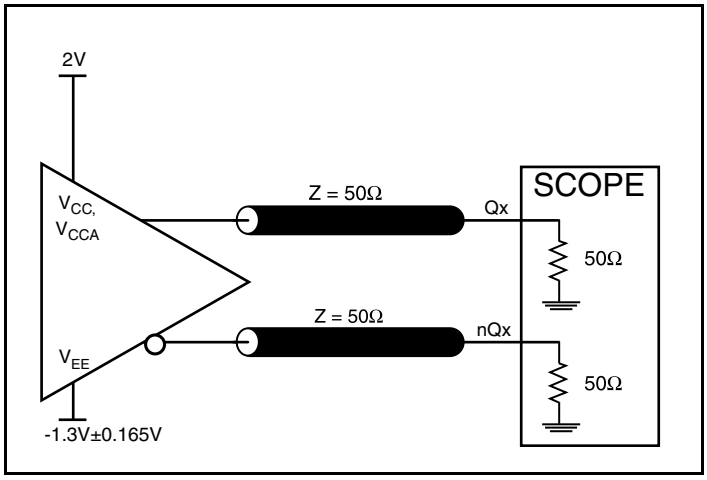
AC Electrical Characteristics

Table 8. AC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

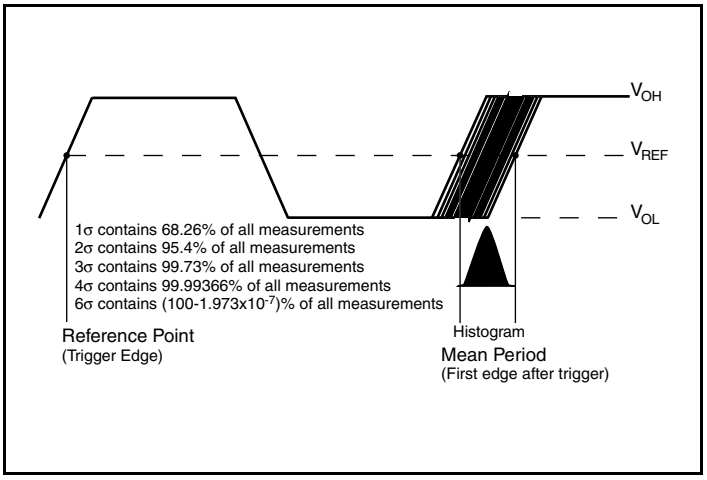
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					700	MHz
*t*jit(per)	Period Jitter, RMS; NOTE 1. 2				3	9	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2				20	40	ps
*t*sk(o)	Output Skew; NOTE 3					80	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_S	Setup Time	SDA to SCL		20			ns
		M, N to nP_LOAD		20			ns
t_H	Hold Time	SDA to SCL		20			ns
		M, N to nP_LOAD		20			ns
F_M	SSC Modulation Frequency; NOTE 4		XTAL_IN = 16.6667MHz	30	32	33.33	kHz
SSC_{RED}	Spectral Reduction; NOTE 4			-7	-10		dB
t_L	PLL Lock Time					10	ms
odc	Output Duty Cycle		N ≠ ÷1	48		52	%
t_{PW}	Output Pulse Width		N = ÷1	t_{PERIOD}/2 - 275	t_{PERIOD}/2	t_{PERIOD}/2 + 275	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information section.
NOTE: Characterized using an XTAL input.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: See Applications section.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured from the output differential cross points.
NOTE 4: Spread Spectrum clocking enabled.

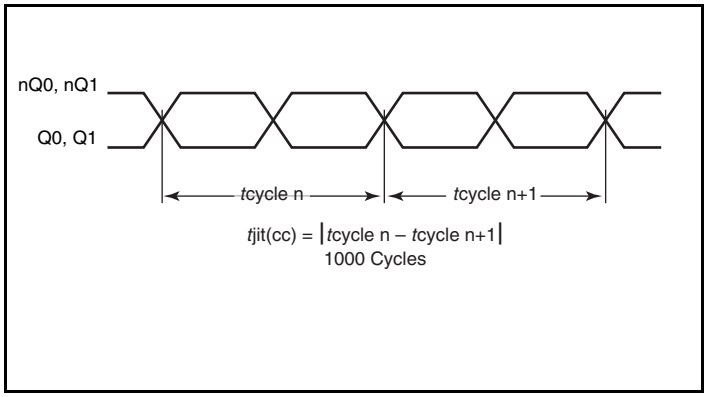
Parameter Measurement Information



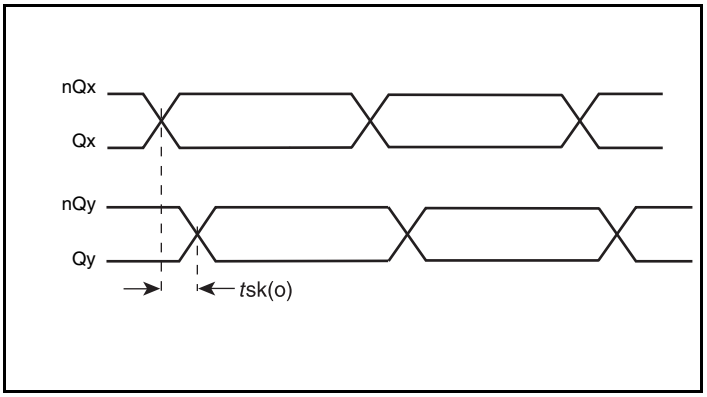
3.3/3.3V LVPECL Output Load AC Test Circuit



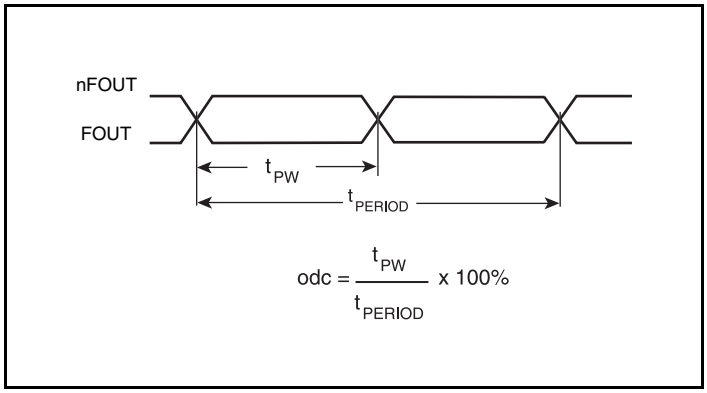
Period Jitter



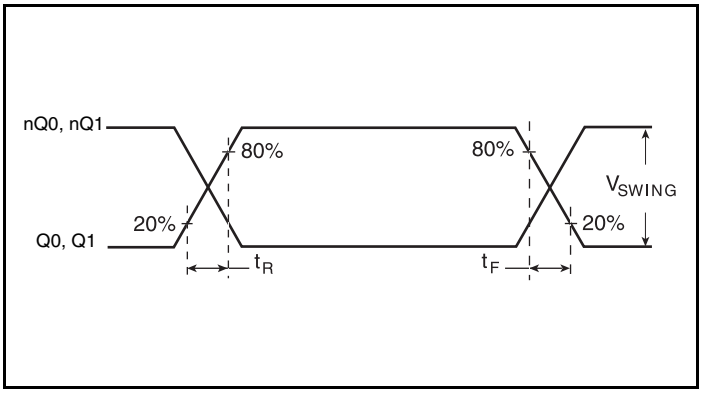
Cycle-to-Cycle Jitter



Output Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 84330B-03 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

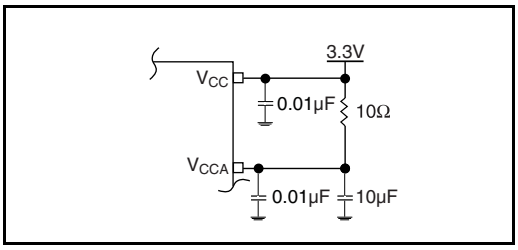


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 84330B-03 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

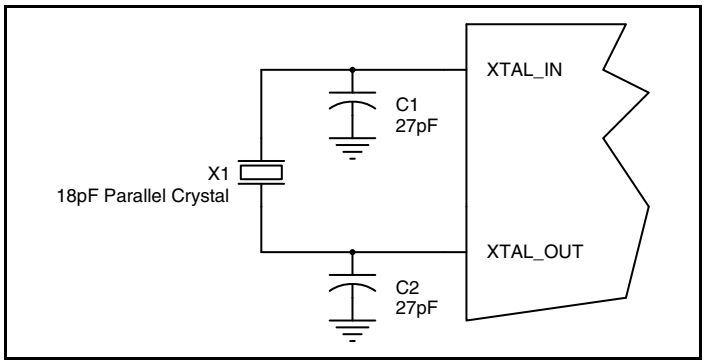


Figure 3. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

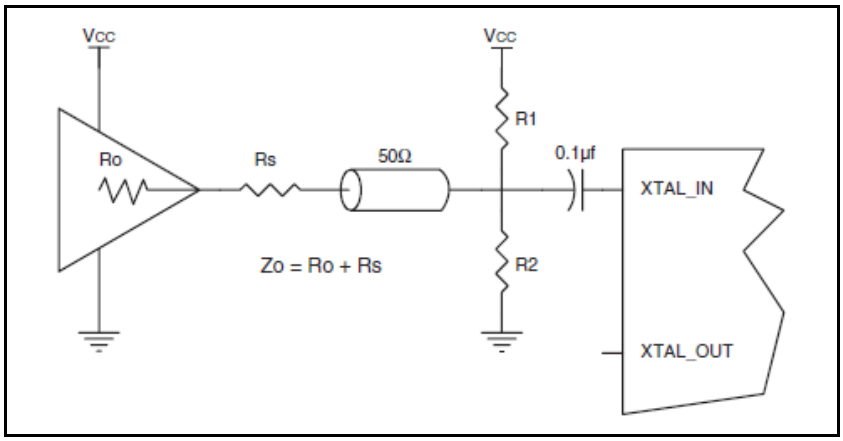


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used from the nominal 333MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 5A* below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread Off mode (333MHz with 16.6667MHz IN)
- Fm = Nominal Modulation Frequency (32kHz)
- δ = Modulation Factor (0.25% down spread)

$$(1-\delta)Fnom + 2fm \times \delta \times Fnom \times t \text{ when } 0 < t < \frac{1}{2fm},$$
$$(1-\delta)Fnom - 2fm \times \delta \times Fnom \times t \text{ when } \frac{1}{2fm} < t < \frac{1}{fm}$$

It is important to note the 84330B-03 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

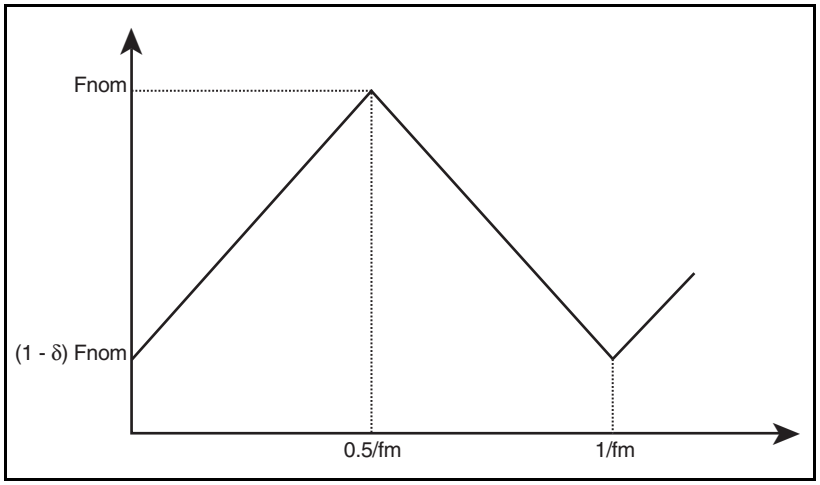


Figure 5A. Triangle Frequency Modulation

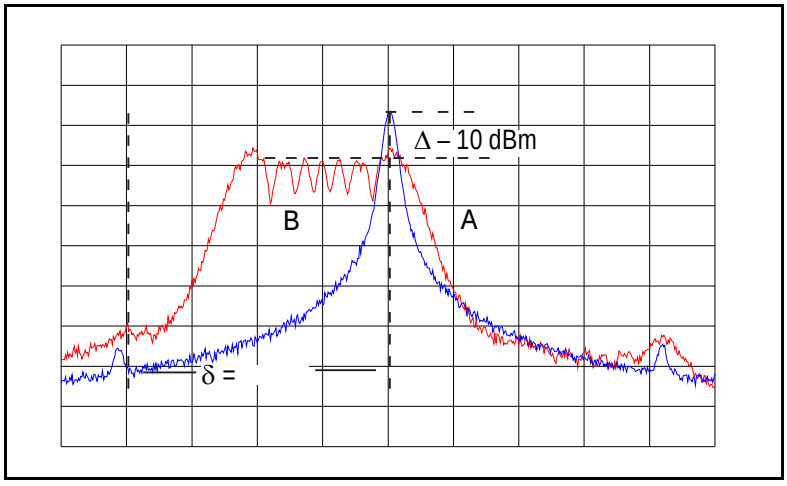


Figure 5B. 333MHz Clock Output In Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Jitter Reduction for FREF_EXT Single-ended Input

If the FREF_EXT input is driven by a 3.3V LVCMOS driver, the jitter performance can be improved by reducing the amplitude swing and slowing down the edge rate. *Figure 6A* shows an amplitude reduction approach for a long trace. The swing will be approx- imately 0.85V for logic low and 2.5V for logic high (instead of 0V to 3.3V). *Figure 6B* shows amplitude reduction approach for a short trace. The circuit shown in *Figure 6C* reduces amplitude swing and also slows down the edge rate by increasing the resistor value.

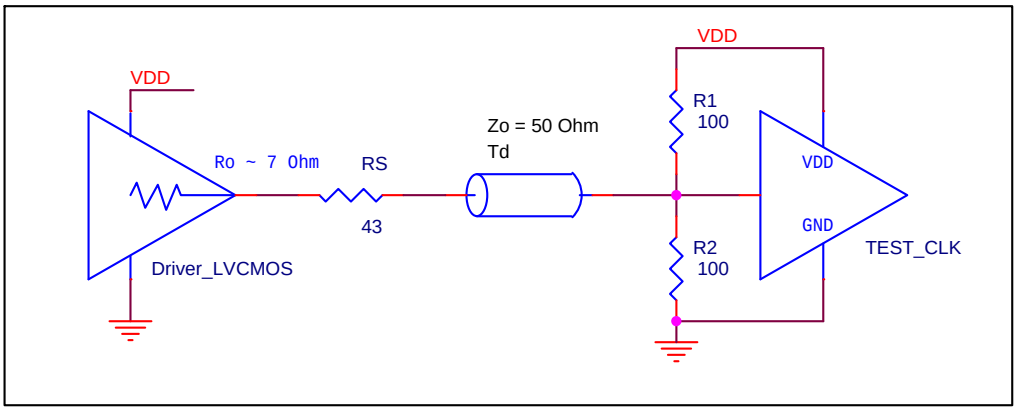


Figure 6A. Amplitude Reduction for Long Trace

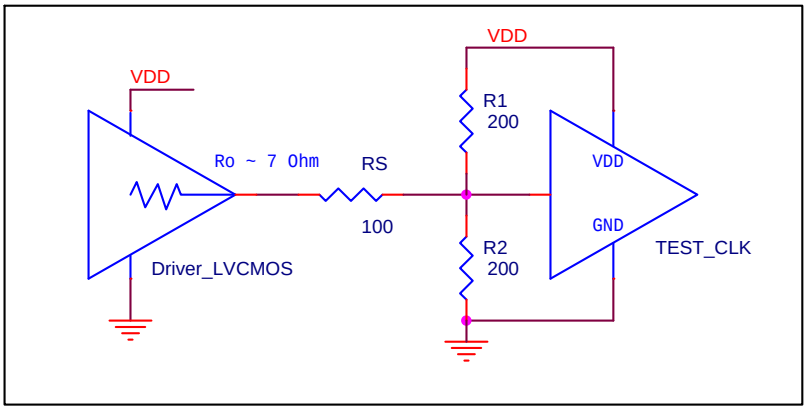


Figure 6B. Amplitude Reduction for Short Trace

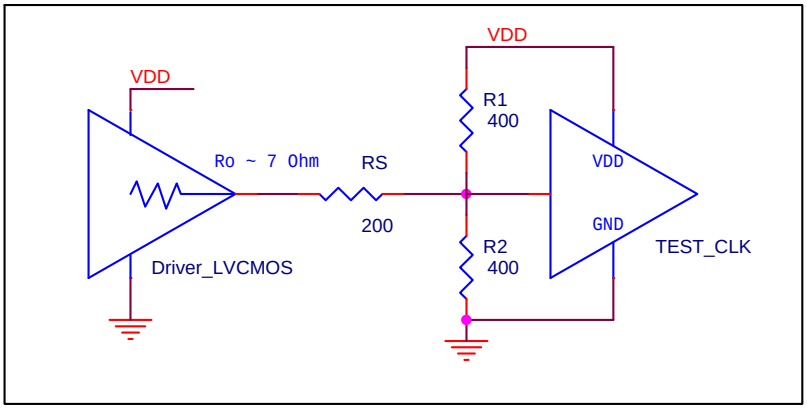


Figure 6C. The Edge Rate can be slow further by increasing the resistor value

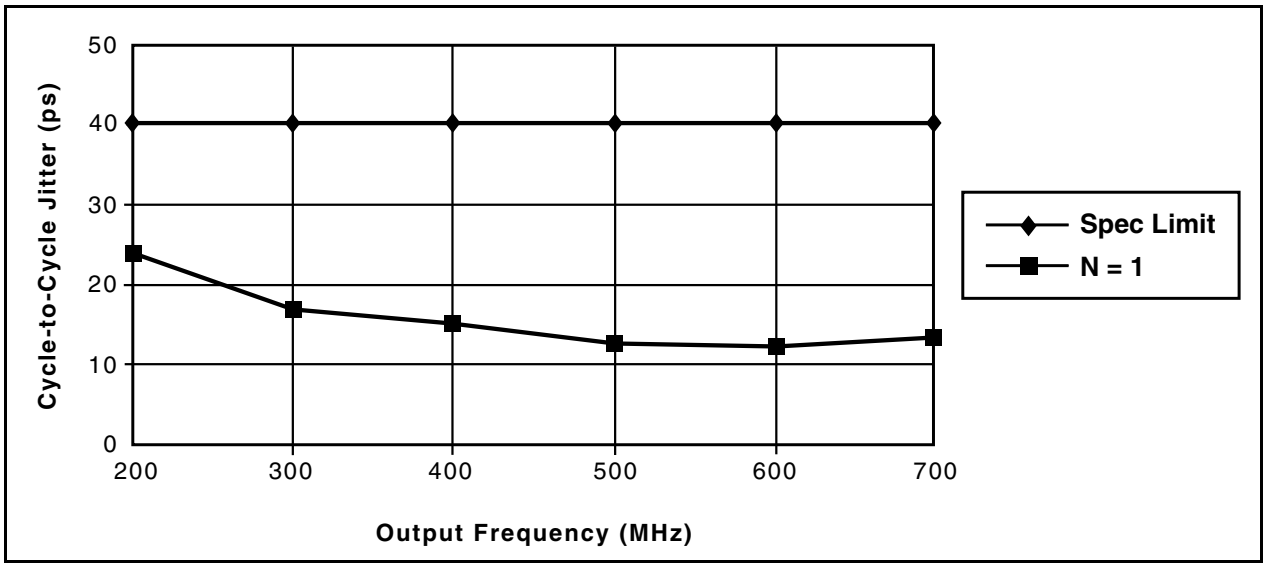


Figure 7. Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz crystal)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

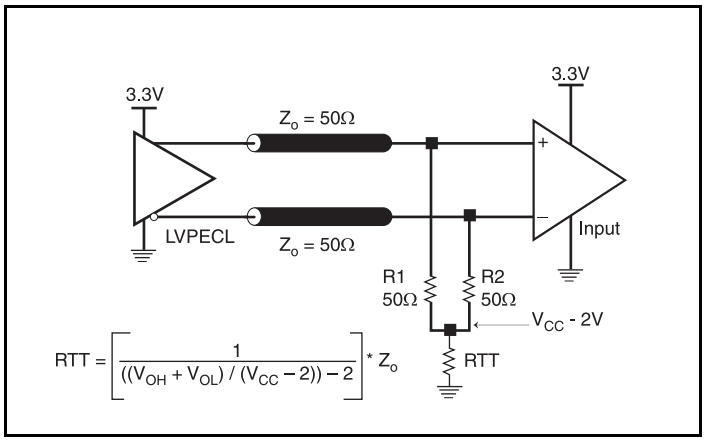


Figure 8A. 3.3V LVPECL Output Termination

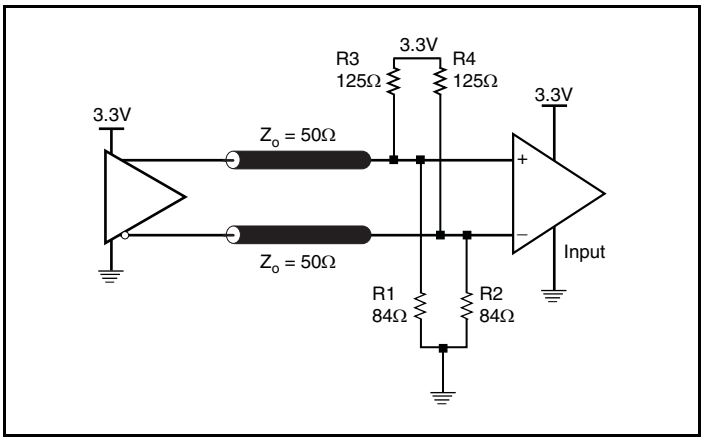


Figure 8B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 84330B-03.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 84330B-03 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 180mA = **623.7mW**
- Power $(outputs)_{MAX}$ = **30.mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

  Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 623.7mW + 60mW = **683.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.684W * 42.1°C/W = 98.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 9.*

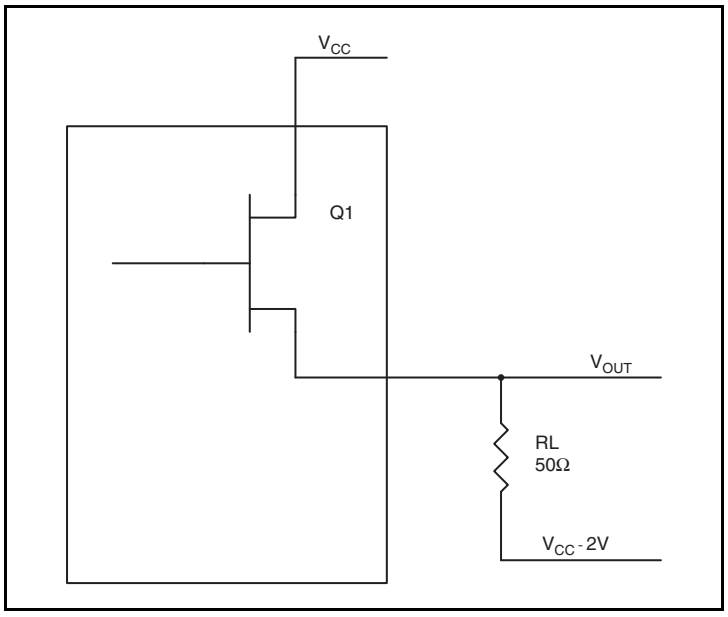


Figure 9. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX}}$ **-0.9V**
  $(V_{CC\_MAX} - V_{OH\_MAX})$ = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX}}$ **-1.7V**
  $(V_{CC\_MAX} - V_{OL\_MAX})$ = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_{L]} * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 10. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Transistor Count

The transistor count for 84330B-03 is: 9304

Package Outline and Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

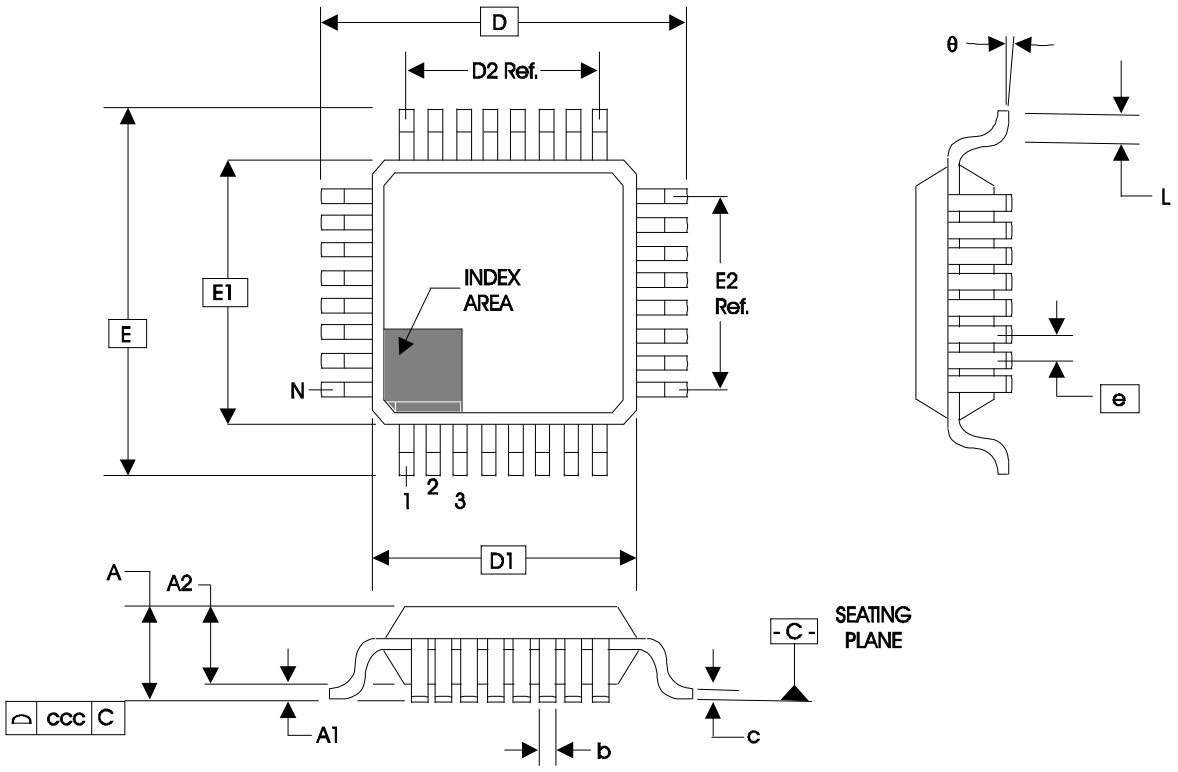


Table 11. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBA All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 12. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
84330BY-03LF	ICS84330B03L	“Lead-Free” 32 Lead LQFP	Tray	0°C to 70°C
84330BY-03LFT	ICS84330B03L	“Lead-Free” 32 Lead LQFP	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5A	9	Power Supply DC Characteristics Table - changed V_{CCA} row from 3.135V min. to V_{CC} - 0.15 and 3.465V max. to V_{CC}. Converted datasheet format.	2/10/09
B	T2	7	Pin Description Table - added pin 24 VCO_SEL description.	2/26/09
C	T2 T5A T5B T12	7 9 9 21	Pin Description Table - corrected pins 23 & 23 (N0, N1) from Pullup to Pulldown. Power DC Characteristics Table - I_{CCA} spec changed from 15mA to 18mA. Changed I_{CC} to I_{EE}. LVCMOS DC Characteristics Table - moved N0, N1 to I_{IH}/I_{IL} Pulldown rows (150µA). Ordering Information Table - changed ordering revision from “A” to “B” in marking and part order number.	8/20/09
C		6	Changed part number from ICS84330-03 to ICS84330B-03 throughout the datasheet. Functional Description - changed wording in 3rd paragraph, 2nd sentece from the end. “On the LOW-to-HIGH transition...”	9/14/09
C	1A	5	SS Mode Function Table - corrected SSC6 column row 3 to “0” instead of 1 and row 4 to “1” instead of 0.	12/1/09
C	T12	1 20	Removed ICS from the part number where needed. General Description - removed ICS chip. Ordering Information - remove 1000 from Tape and Reel and removed the LF note below the table. Updated data sheet header and footer.	1/15/16

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