FemtoClock® Crystal-to-3.3V LVPECL Frequency Synthesizer

843204I-01

DATA SHEET

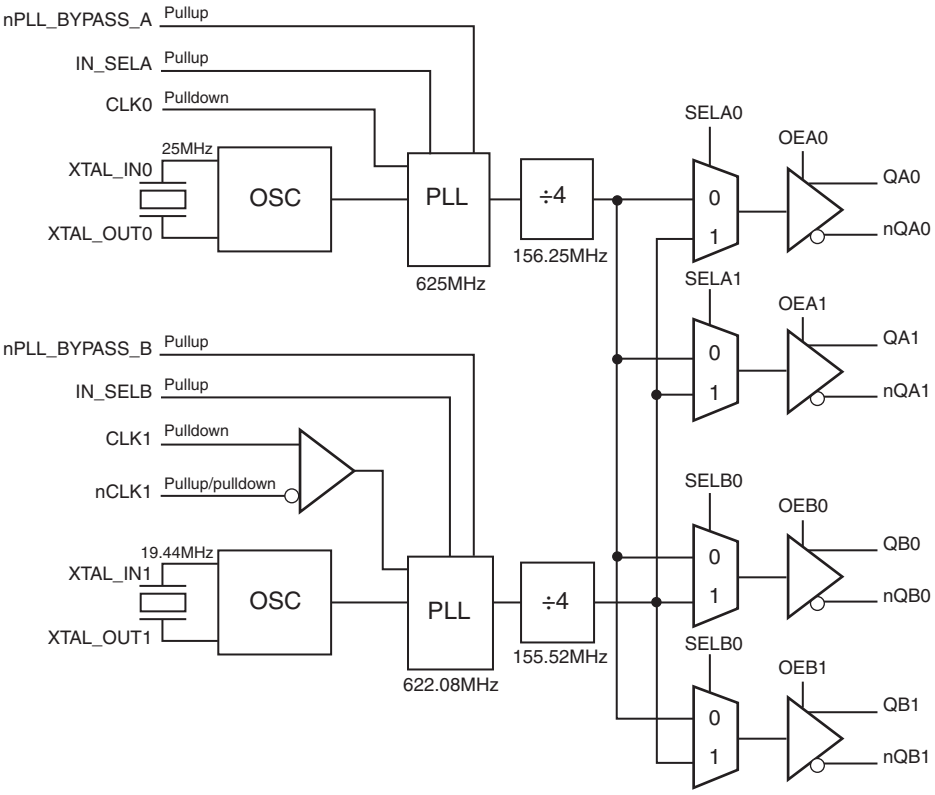
General Description

The 843204I-01 is a 4 output LVPECL Synthe-sizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The 843204I-01 uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter.

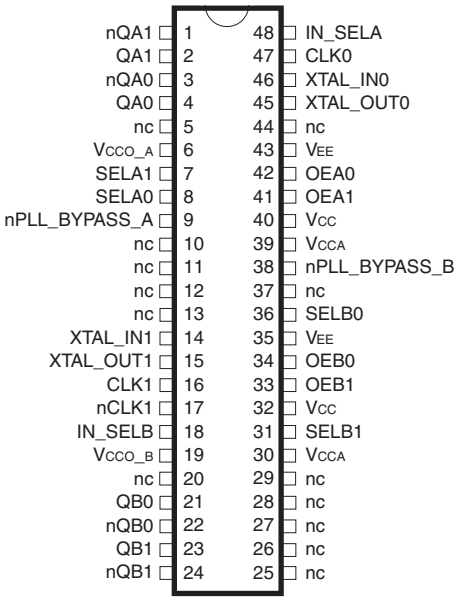
Features

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or clock inputs
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz - 13MHz): 0.6ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.7ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part us 8T49N285

Block Diagram



Pin Assignment



843204I-01
48 Lead TSSOP
6.1mm x 12.5mm x 0.925mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
3, 4	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
5, 10, 11, 12, 13, 20, 25, 26, 27, 28, 29, 37, 44	nc	Unused		No connect.
6	V_{CCO_A}	Power		Output supply pin for Bank A outputs.
7	SELA1	Input	Pulldown	Select pin. When HIGH, selects QA1/nQA1 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels.
8	SELA0	Input	Pulldown	Select pin. When HIGH, selects QA0/nQA0 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels.
9	nPLL_BYPASS_A	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active.
14, 15	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
16	CLK1	Input	Pulldown	Non-inverting differential clock input.
17	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
18	IN_SELB	Input	Pullup	Select pin. When HIGH, selects XTAL1 inputs. When LOW, selects CLK1, nCLK1 inputs. LVCMOS/LVTTL interface levels.
19	V_{CCO_B}	Power		Output supply pin for Bank B outputs.
21, 22	QB0, nQB0	Ouput		Differential output pair. LVPECL interface levels.
23, 24	QB1, nQB1	Ouput		Differential output pair. LVPECL interface levels.
30, 39	V_{CCA}	Power		Analog supply pins.
31	SELB1	Input	Pullup	Select pin. When HIGH, selects QB1/nQB1 at 155.52MHz. When LOW, selects QB1/nQB1 at 156.25MHz. LVCMOS/LVTTL interface levels.
32, 40	V_{CC}	Power		Core supply pins.
33	OEB1	Input	Pullup	Output enable pin. QB1/nQB1 outputs are enable. LVCMOS/LVTTL interface levels.
34	OEB0	Input	Pullup	Output enable pin. QB0/nQB0 outputs are enabled. LVCMOS/LVTTL interface levels.
35, 43	V_{EE}	Power		Negative supply pins.
36	SELB0	Input	Pullup	Select pin. When HIGH, selects QB0/nQB0 at 155.52MHz. When LOW, selects QB0/nQB0 at 156.25MHz. LVCMOS/LVTTL interface levels.
38	nPLL_BYPASS_B	Input	Pullup	When LOW, PLL is bypassed. When HIGH, PLL output is active.
41	OEA1	Input	Pullup	Output enable pin. QA1/nQA1 outpus are enabled. LVCMOS/LVTTL interface levels.
42	OEA0	Input	Pullup	Output enable pin. QA0/nQA0 outputs are enabled. LVCMOS/LVTTL interface levels.
45, 46	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
47	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input.
48	IN_SELA	Input	Pullup	Select pin. When HIGH, selects XTAL0 inputs. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k
R_{PULLUP}	Input Pullup Resistor			51		k

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	54.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.22	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				165	mA
I_{CCA}	Analog Supply Current				22	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK0, SELA0, SELA1	$V_{CC} = V_{IN}$ = 3.63V			150	µA
		nPLL_BYPASS_A, nPLL_BYPASS_B, IN_SELA, IN_SELB, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1	$V_{CC} = V_{IN}$ = 3.63V			5	µA
I_{IL}	Input Low Current	CLK0, SELA0, SELA1	V_{CC} = 3.63V, V_{IN} = 0V	-5			µA
		nPLL_BYPASS_A, nPLL_BYPASS_B, IN_SELA, IN_SELB, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1	V_{CC} = 3.63V, V_{IN} = 0V	-150			µA

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V±10%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK1, nCLK1	V_{IN} = V_{CC} = 3.63V			150	µA
I_{IL}	Input Low Current	nCLK1	V_{IN} = 0V, V_{CC} = 3.63V	-150			µA
		CLK1	V_{IN} = 0V, V_{CC} = 3.63V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 3D. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V±10%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 to V_{CCO} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	XTAL0			25		MHz
	XTAL1			19.44		MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

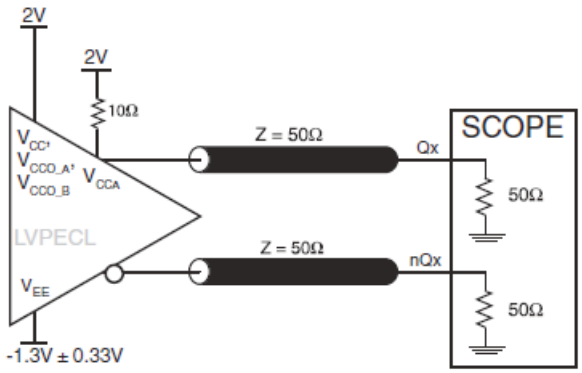
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V±10%, V_{EE} = 0V, TA = -40°C TO 85°C

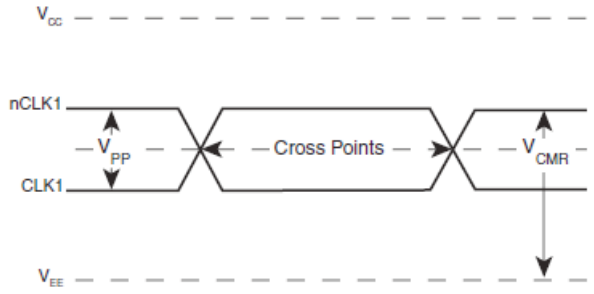
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	SELB0 = 1; OEB0 = 1		155.52		MHz
		SELA0 = 0; OEA0 = 1		156.25		MHz
tsk(b)	Bank Skew; NOTE 1, 2				60	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	155.52MHz, (12kHz - 1.3MHz)		0.6		ps
		156.25MHz, (1.875MHz - 20MHz)		0.7		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		47		53	%

NOTE 1: Defined as skew within a bank of outputs at the same supply voltags and with equal load conditions.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: See Phase Noise plot.

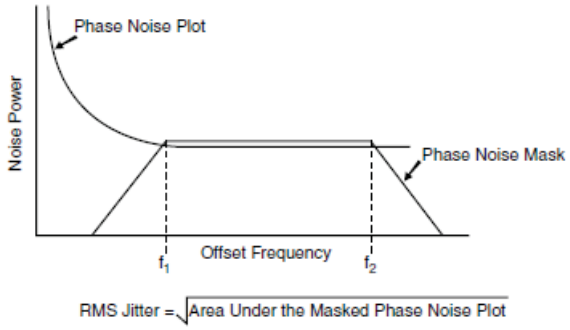
PARAMETER MEASUREMENT INFORMATION



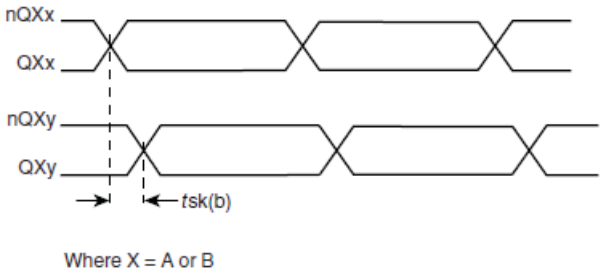
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



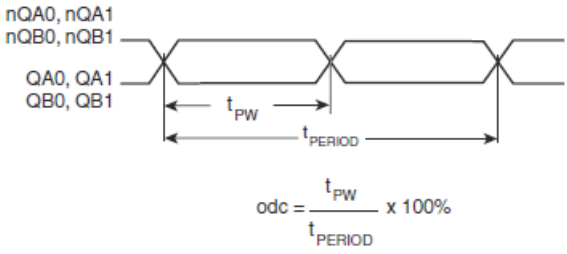
DIFFERENTIAL INPUT LEVEL



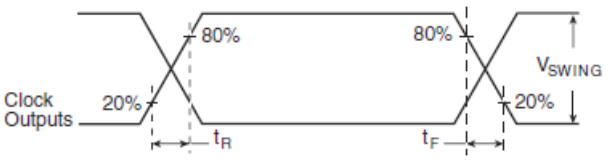
RMS PHASE JITTER



BANK SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843204I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

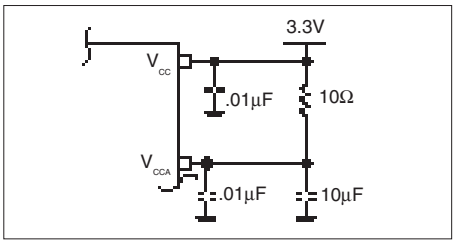


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 843204I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

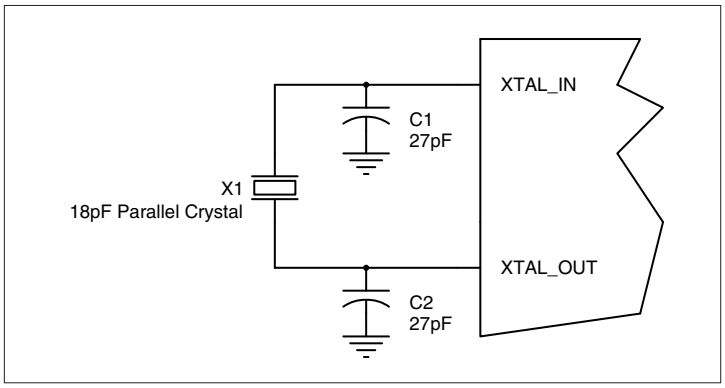


FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

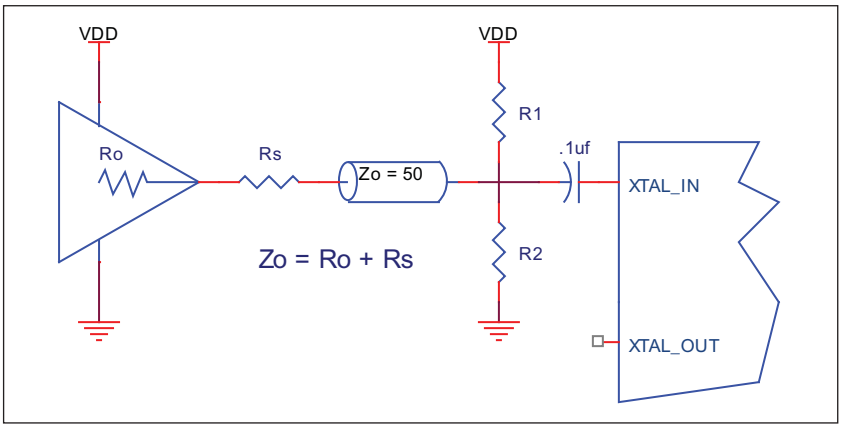


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single Ended Levels

Figure 4 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{cc}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{cc} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

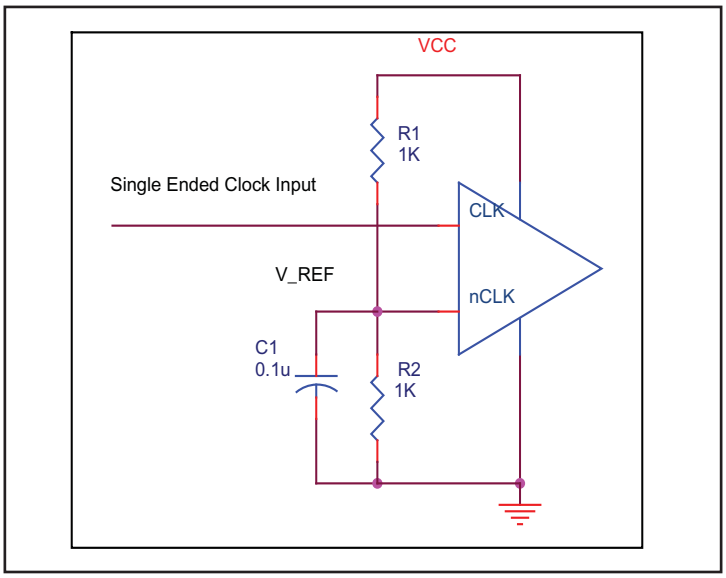


Figure 4. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

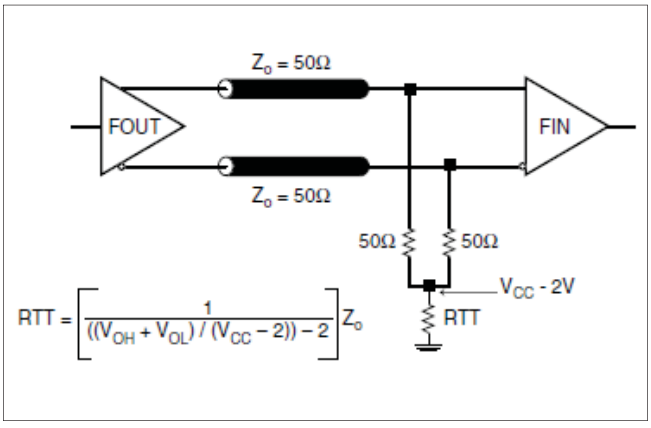


Figure 5A. LVPECL Output Termination

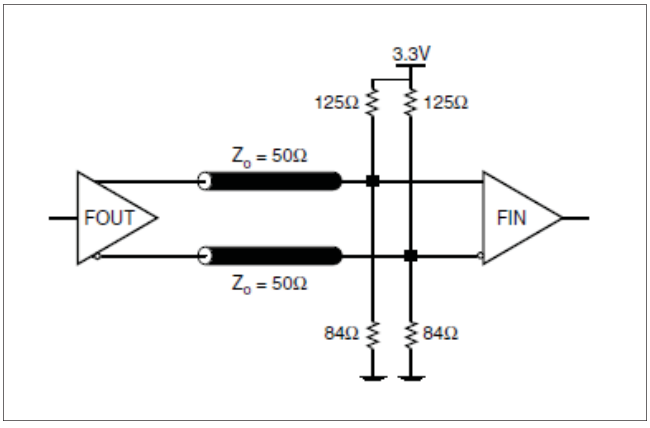


Figure 5B. LVPECL Output Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843204I-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843204I-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 165mA = **598.95mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power $_{MAX}$ (3.63V, with all outputs switching) = 598.95mW + 120mW = **718.95mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assumig no air flow and a multi-layer board, the appropriate value is 54.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.719W * 54.8°C/W = 124.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	54.8°C/W	51.0°C/W	49.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

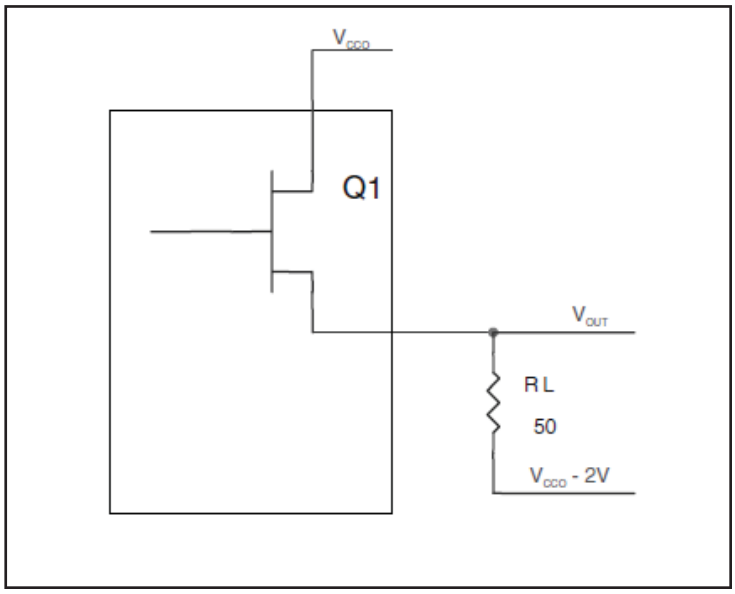


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 48 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	54.8°C/W	51.0°C/W	49.1°C/W

Transistor Count

The transistor count for 843204I-01 is: 3974

Package Outline - G Suffix for 48 Lead TSSOP

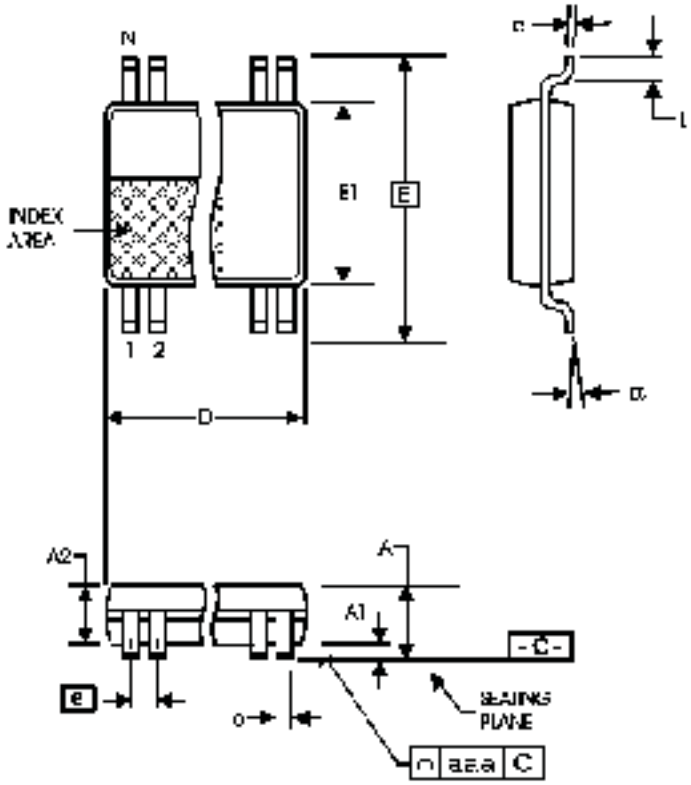


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	48	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.17	0.27
c	0.09	0.20
D	12.40	12.60
E	8.10 BASIC	
E1	6.00	6.20
e	0.50 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843204AGI-01LF	ICS843204AI01L	48 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
843204AGI-01LFT	ICS843204AI01L	48 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	1 12	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05. Ordering Information - Removed leaded devices and ICS from orderable part number. Updated data sheet format.	11/5/15

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