Low Skew, 1-to-24 Differential-to-LVCMOS/LVTTL Fanout Buffer

ICS8344I-01

DATA SHEET

General Description

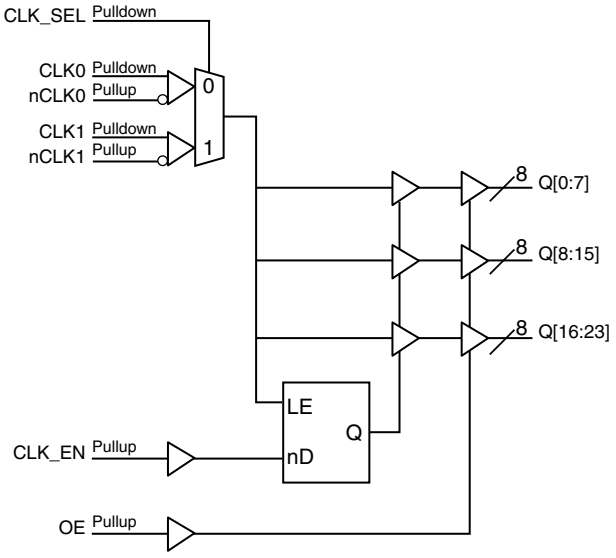
The ICS8344I-01 is a low voltage, low skew fanout buffer. The ICS8344I-01 has two selectable clock inputs. The CLKx, nCLKx pairs can accept most standard differential input levels. The ICS8344I-01 is designed to translate any differential signal level to LVCMOS/LVTTL levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock inputs which also facilitate board level testing. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The outputs are driven low when disabled. The ICS8344I-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

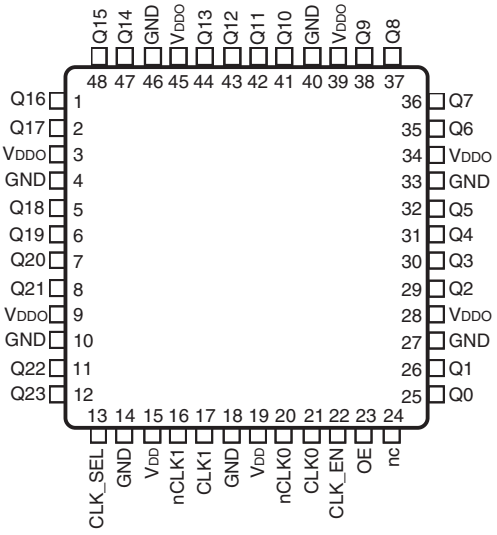
Features

- Twenty-four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Two selectable differential CLKx, nCLKx inputs
- CLK0, nCLK0 and CLK1, nCLK1 pairs can accept the following input levels: LVDS, LVPECL, LVHSTL, HCSL
- Maximum output frequency: 100MHz
- Translates any single ended input signal to LVCMOS/LVTTL with resistor bias on nCLK input
- Synchronous clock enable
- Additive phase jitter, RMS: 0.21ps (typical)
- Output skew: 200ps (maximum)
- Part-to-part skew: 900ps (maximum)
- Bank skew: 180ps (maximum)
- Propagation delay: 5ns (maximum)
- Output supply modes:
  Core/Output
  3.3V/3.3V
  2.5V/2.5V
  3.3V/2.5V
- -40°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8344I-01

48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 5, 6, 7, 8, 11, 12	Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23	Output		Single-ended clock outputs. 7Ω typical output Impedance. LVCMOS/LVTTL interface levels.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins.
4, 10, 14, 18, 27, 33, 40, 46	GND	Power		Power supply ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK inputs, When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
15, 19	V_{DD}	Power		Power supply pins.
16	nCLK1	Input	Pullup	Inverting differential clock input.
17	CLK1	Input	Pulldown	Non-inverting differential clock input.
20	nCLK0	Input	Pullup	Inverting differential clock input.
21	CLK0	Input	Pulldown	Non-inverting differential clock input.
22	CLK_EN	Input	Pullup	Synchronizing control for enabling and disabling clock outputs. LVCMOS / LVTTL interface levels.
23	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q[0:23]. LVCMOS / LVTTL interface levels.
24	nc	Unused		No connect.
25, 26, 29, 30, 31, 32, 35, 36	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	Output		Single-ended clock outputs. 7Ω typical output Impedance. LVCMOS/LVTTL interface levels.
37, 38, 41, 42, 43, 44, 47, 48	Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15	Output		Single-ended clock outputs. 7Ω typical output Impedance. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = V_{DDO} = 3.465V		23		pF
		V_{DD} = V_{DDO} = 2.625V		16		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V±5% or 2.5V±5%		7		Ω

Function Tables

Table 3A. Output Enable Function Table

Control Input		Outputs
OE	**CLK_EN**	**Q[0:23]**
0	X	High-Impedance
1	0	Disabled in Logic LOW state; NOTE 1
1	1	Enabled; NOTE 1

NOTE 1: The clock enable and disable function is synchronous to the falling edge of the selected reference clock.

Table 3A. Clock Select Function Table

Control Input	Clock	
CLK_SEL	**CLK0, nCLK0**	**CLK1, nCLK1**
0	Selected	De-selected
1	De-selected	Selected

Table 3C. Clock Input Function Table

Inputs			Outputs		
OE	**CLK0, CLK1**	**nCLK0, nCLK1**	**Q[0:23]**	**Input to Output Mode**	**Polarity**
1 (default)	0 (default)	1 (default)	LOW	Differential to Single-Ended	Non-Inverting
1	1	0	HIGH	Differential to Single-Ended	Non-Inverting
1	0	Biased; NOTE 1	LOW	Single-Ended to Single-Ended	Non-Inverting
1	1	Biased; NOTE 1	HIGH	Single-Ended to Single-Ended	Non-Inverting
1	Biased; NOTE 1	0	HIGH	Single-Ended to Single-Ended	Inverting
1	Biased; NOTE 1	1	LOW	Single-Ended to Single-Ended	Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	53.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, or V_{DD} = V_{DDO} = 2.5V ± 5%, or V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		3.8	V
			V_{DD} = 2.625V	2		2.9	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.8	V
I_{IH}	Input High Current	OE, CLK_EN	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE, CLK_EN	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.135V, I_{OH} = -36mA	2.7			V
			V_{DDO} = 2.375V, I_{OH} = -27mA	1.9			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.135V, I_{OL} = 36mA			0.5	V
			V_{DDO} = 2.375V, I_{OL} = 27mA			0.5	V

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, or $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, or $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.9		2.0	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

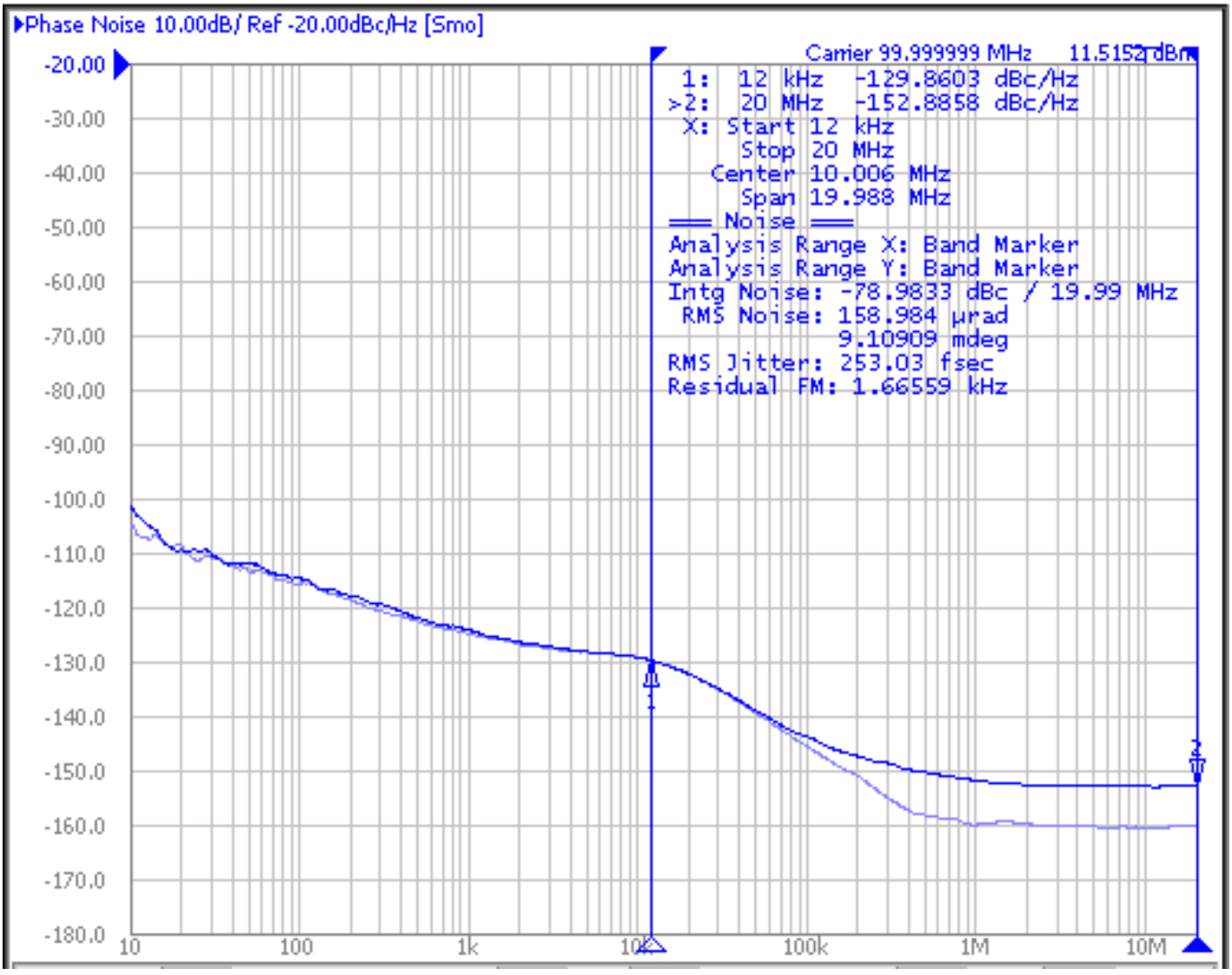
Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, or $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, or $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					100	MHz
t_{PD}	Propagation Delay; NOTE 1		f ≤ 100MHz	2.5		5	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		100MHz, Integration Range: 12kHz – 20MHz		0.21		ps
*t*sk(b)	Bank Skew; NOTE 2, 6	Q[0:7]	Measured on the rising edge of $V_{DDO}/2$			155	ps
		Q[8:15]				180	ps
		Q[16:23]				140	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the rising edge of $V_{DDO}/2$			200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6		Measured on the rising edge of $V_{DDO}/2$			900	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		30% to 70%	200		800	ps
t_{EN}	Output Enable Time; NOTE 5		f = 10MHz			5	ns
t_{DIS}	Output Disable Time; NOTE 5		f = 10MHz			4	ns
odc	Output Duty Cycle		f ≤ 100MHz	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at ≤100MHz and V_{PP}_typ unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

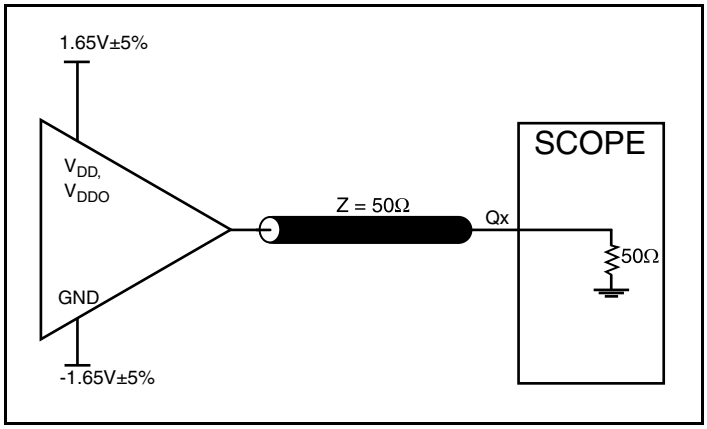
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



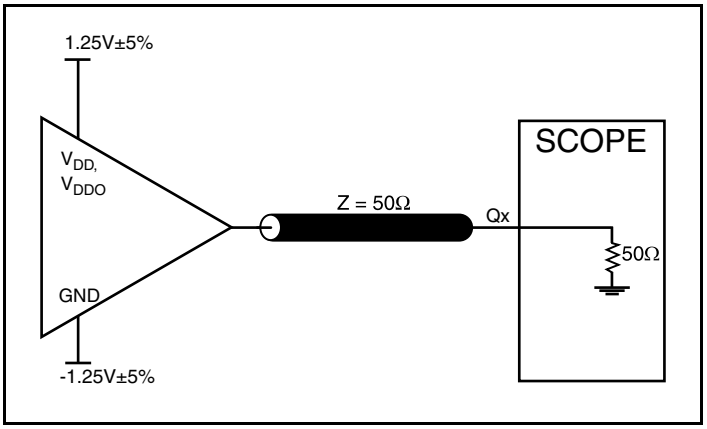
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, "Agilent E5052A Signal Source Analyzer".

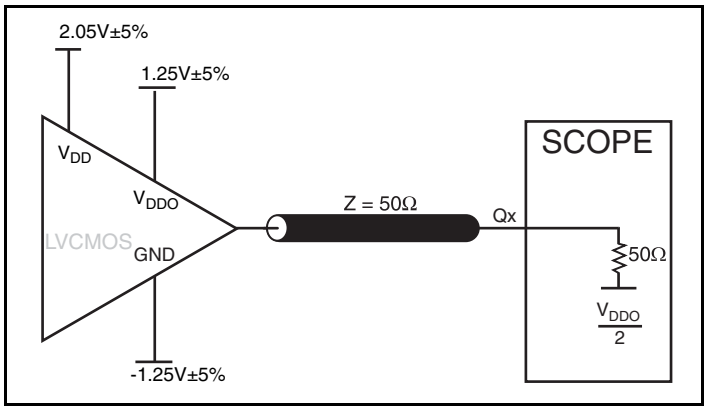
Parameter Measurement Information



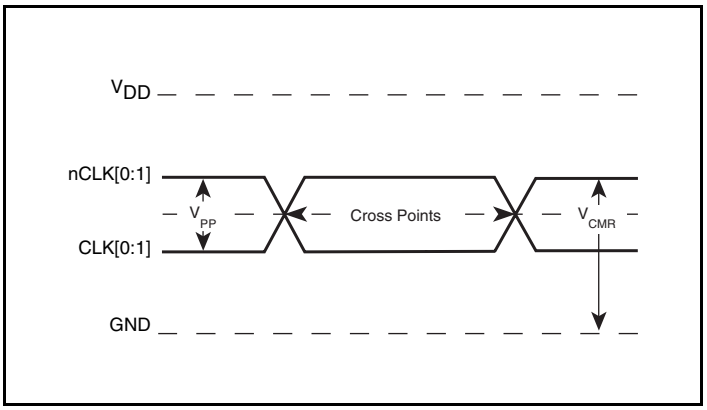
3.3V Output Load AC Test Circuit



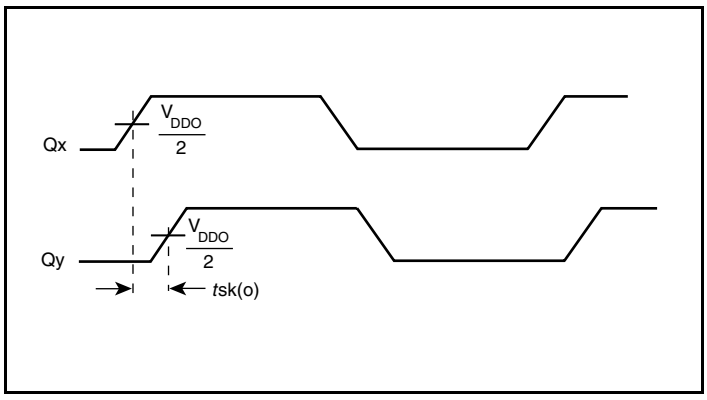
2.5V Output Load AC Test Circuit



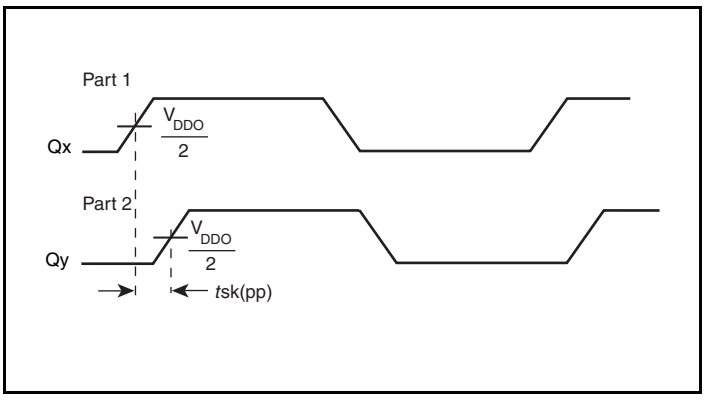
3.3V Core/2.5V Output Load AC Test Circuit



Differential Input Level

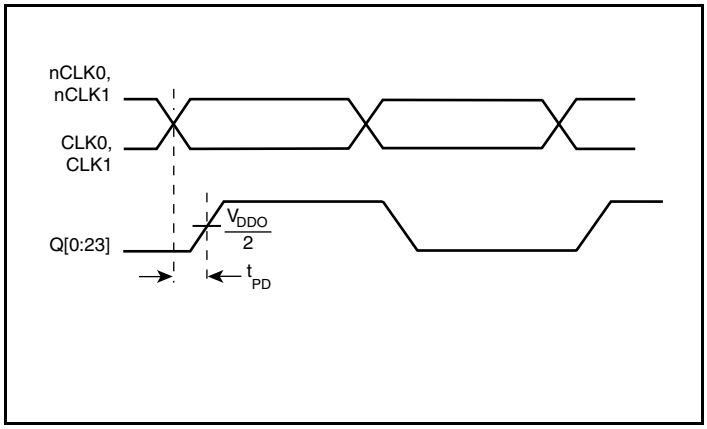


Output Skew

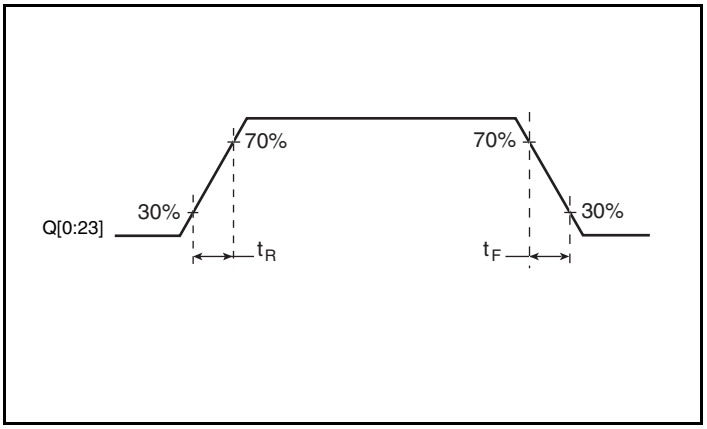


Part-to-Part Skew

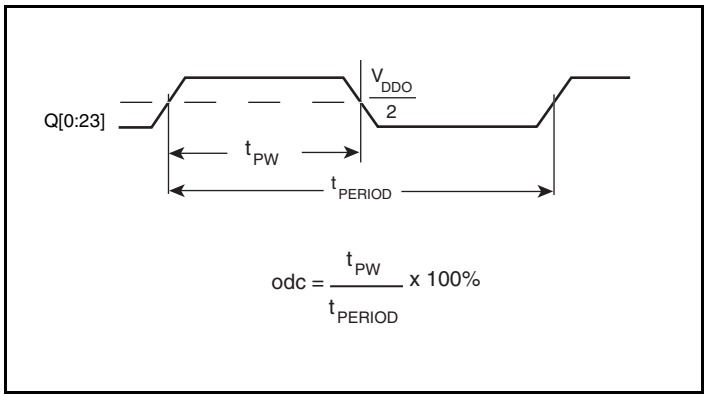
Parameter Measurement Information, continued



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

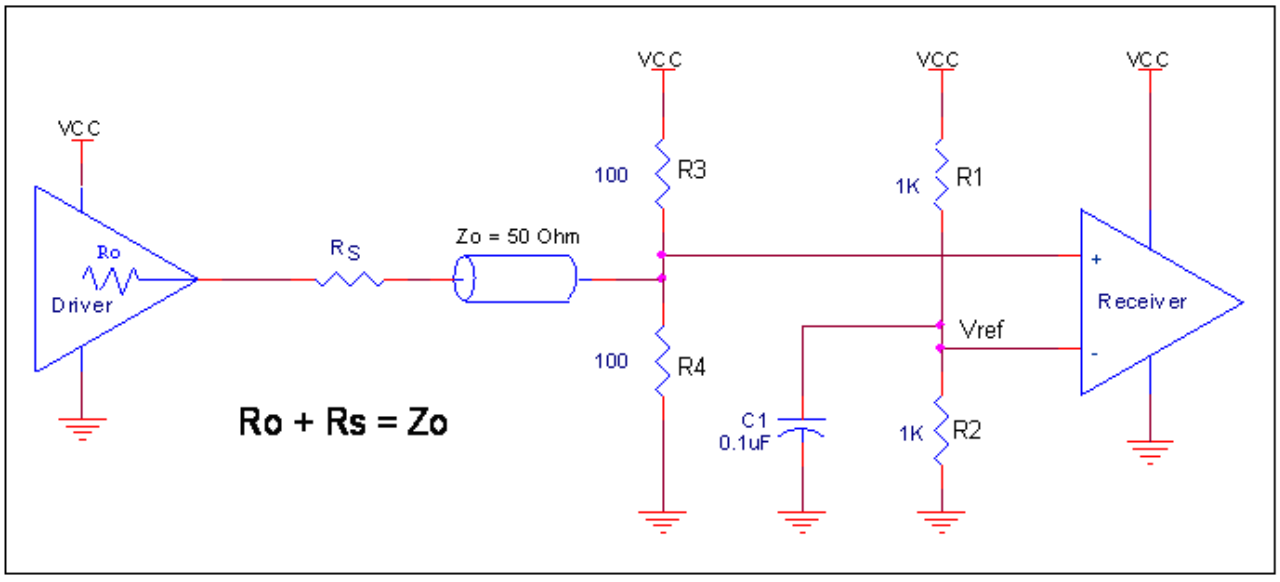


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLKx /nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

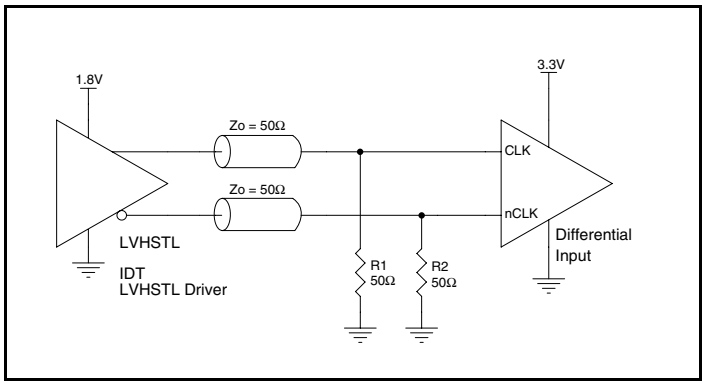


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

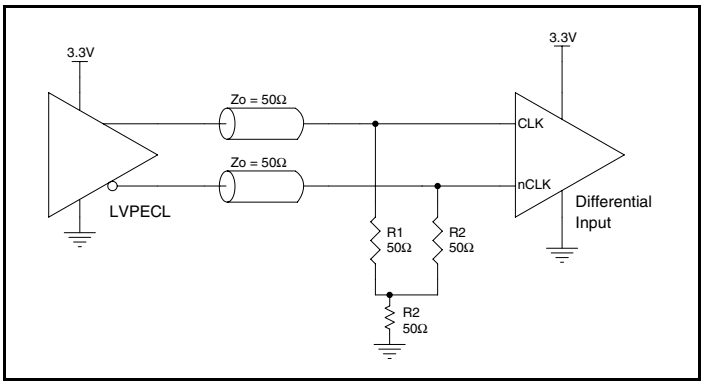


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

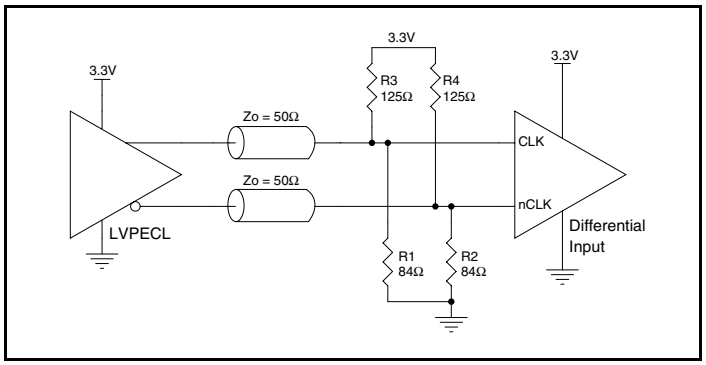


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

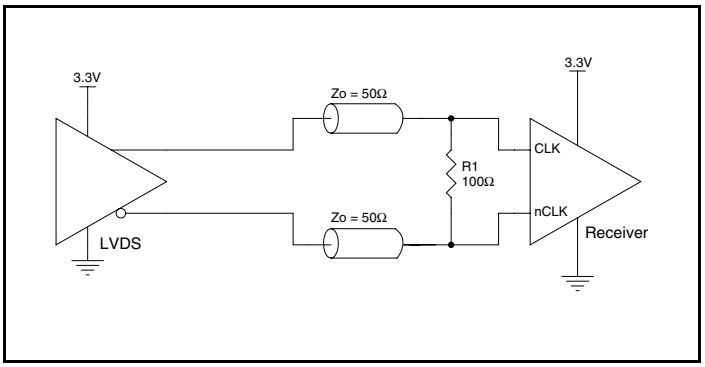


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

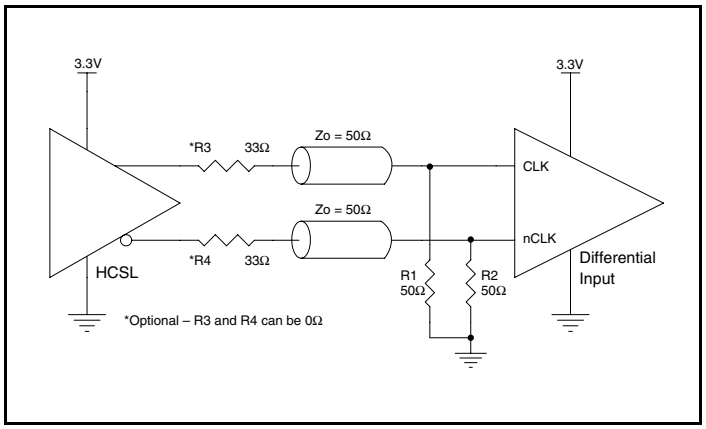


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8344I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8344I-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.465V *95mA = **329.2mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 7Ω)] = **30.4mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 7Ω * (30.4mA)^2 = **6.47mW per output**
- Total Power (R_{OUT}) = 6.47mW * 24 = **155mW**

Dynamic Power Dissipation at 100MHz

Power (100MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 16pF * 100MHz * (3.465V)^2 = **19.2mW per output**

Total Power (100MHz) = 19.2mW * 24 = **461mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (100MHz)
  = 329.2mW + 155mW + 461mW
  = 945.2mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.945W *53.9°C/W = 120.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	53.9°C/W	47.7°C/W	45.0°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 48 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	53.9°C/W	47.7°C/W	45.0°C/W

Transistor Count

The transistor count for ICS8344I-01 is: 1503

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead LQFP

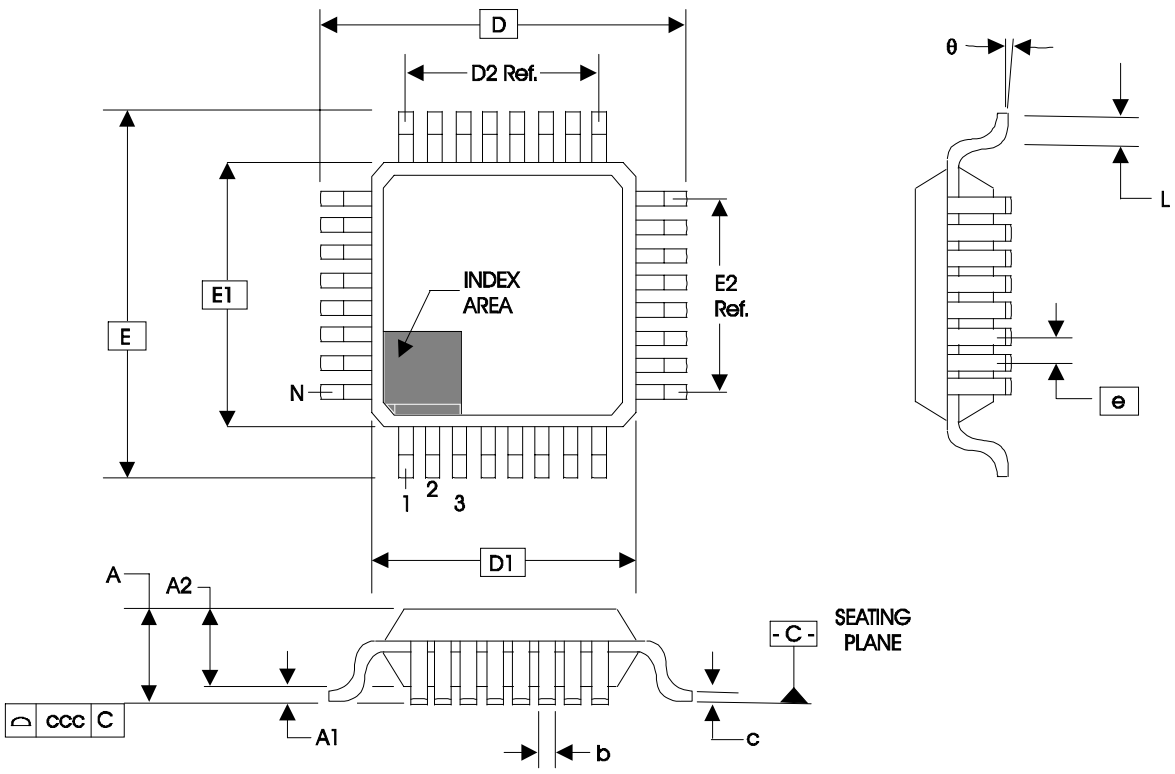


Table 7. Package Dimensions for 48 Lead LQFP

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
c	0.09	0.15	0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
e		0.50 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8344AYI-01LF	ICS8344AI01L	“Lead-Free” 48 Lead LQFP	Tray	-40°C to 70°C
8344AYI-01ILFT	ICS8344AI01L	“Lead-Free” 48 Lead LQFP	1000 Tape & Reel	-40°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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