

FEATURES:

- 2.3V to 2.7V Operation
- SSTL_2 Class I style data inputs/outputs
- Differential CLK input
- RESET control compatible with LVCMS levels
- Flow-through architecture for optimum PCB design
- Drive up to equivalent of 14 SDRAM loads
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in TSSOP package

DESCRIPTION:

The SSTVF16857 is a 14-bit registered buffer designed for 2.3V-2.7V VDD and supports low standby operation. All data inputs and outputs are SSTL_2 level compatible with JEDEC standard for SSTL_2.

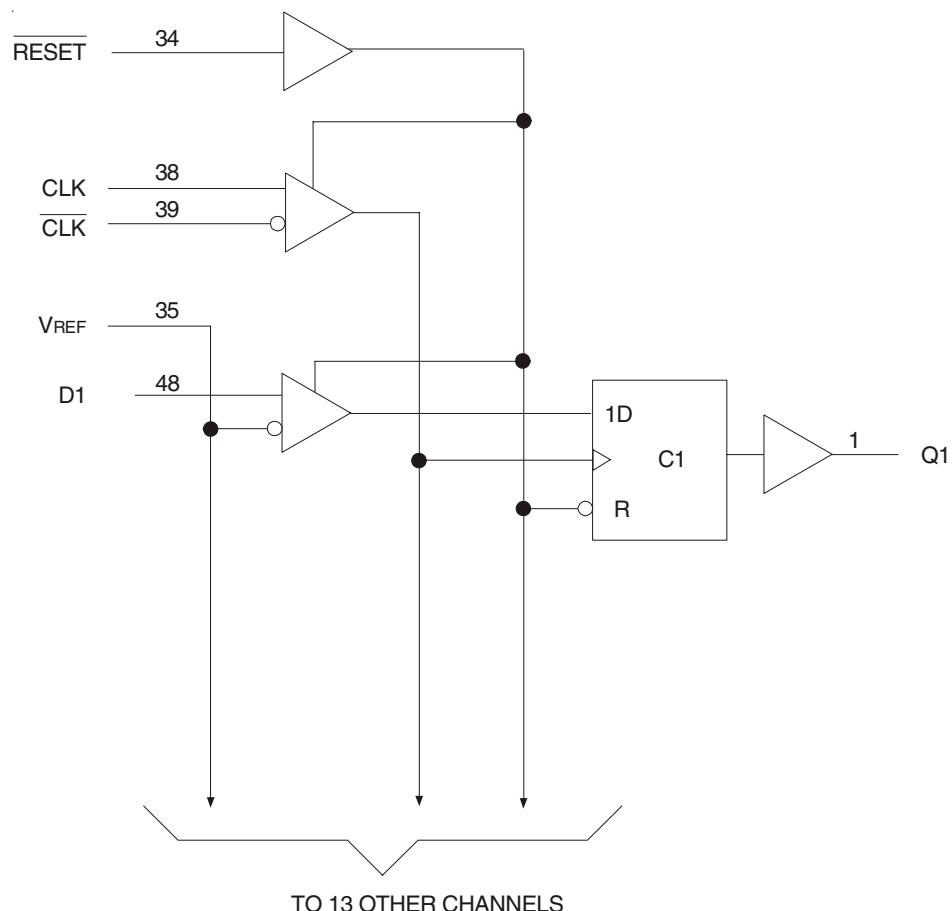
RESET is an LVCMS input since it must operate predictably during the power-up phase. RESET, which can be operated independent of CLK and CLK, must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

RESET, when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of RESET.

APPLICATIONS:

- Along with CSPT857C, Zero Delay PLL Clock buffer, provides complete solution for DDR1 DIMMs

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Q1	1	48	D1
Q2	2	47	D2
GND	3	46	GND
VDDQ	4	45	VDD
Q3	5	44	D3
Q4	6	43	D4
Q5	7	42	D5
GND	8	41	D6
VDDQ	9	40	D7
Q6	10	39	CLK
Q7	11	38	CLK
VDDQ	12	37	VDD
GND	13	36	GND
Q8	14	35	VREF
Q9	15	34	RESET
VDDQ	16	33	D8
GND	17	32	D9
Q10	18	31	D10
Q11	19	30	D11
Q12	20	29	D12
VDDQ	21	28	VDD
GND	22	27	GND
Q13	23	26	D13
Q14	24	25	D14

TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VDD or VDDQ	Supply Voltage Range	-0.5 to 3.6	V
Vi ⁽²⁾	Input Voltage Range	-0.5 to VDD + 0.5	V
Vo ⁽³⁾	Output Voltage Range	-0.5 to VDDQ + 0.5	V
Iik	Input Clamp Current, Vi < 0	-50	mA
Iok	Output Clamp Current, Vo < 0 or Vo > VDDQ	±50	mA
Io	Continuous Output Current, Vo = 0 to VDDQ	±50	mA
VDD	Continuous Current through each VDD, VDDQ or GND	±100	mA
TSTG	Storage Temperature Range	-65 to +150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. The output current will flow if the following conditions are observed:
 - a) Output in HIGH state
 - b) Vo = VDDQ

FUNCTION TABLE (1)

Input				Q Outputs
RESET	CLK	CLK	D	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q0 ⁽²⁾
L	X	X	X	L

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2. Q0 = Output level before the indicated steady-state conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 2.5V \pm 0.2V$, $V_{DDQ} = 2.5V \pm 0.2V$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs	$V_{DD} = 2.3V$, $I_I = -18\text{mA}$	—	—	-1.2	V
V_{OH}		$V_{DD} = 2.3V$ to $2.7V$, $I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2$	—	—	V
		$V_{DD} = 2.3V$, $I_{OH} = -8\text{mA}$	1.95	—	—	
V_{OL}		$V_{DD} = 2.3V$ to $2.7V$, $I_{OL} = 100\mu\text{A}$	—	—	0.2	V
		$V_{DD} = 2.3V$, $I_{OL} = 8\text{mA}$	—	—	0.35	
I_I	All Inputs	$V_{DD} = 2.7V$, $V_I = V_{DD}$ or GND	—	—	± 5	μA
I_{DD}	Static Standby	$I_O = 0$, $V_{DD} = 2.7V$, $\overline{\text{RESET}} = \text{GND}$	—	—	0.01	mA
	Static Operating	$I_O = 0$, $V_{DD} = 2.7V$, $\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH}$ (AC) or V_{IL} (AC)	—	6	—	
I_{DDD}	Dynamic Operating (Clock Only)	$I_O = 0$, $V_{DD} = 2.7V$, $\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH}$ (AC) or V_{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.	—	—	—	$\mu\text{A/Clock}$ MHz
	Dynamic Operating (Per Each Data Input)	$I_O = 0$, $V_{DD} = 2.7V$, $\overline{\text{RESET}} = V_{DD}$, $V_I = V_{IH}$ (AC) or V_{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	—	—	$\mu\text{A/Clock}$ MHz/Data Input
C_I	Data Inputs	$V_{DD} = 2.5V$, $V_I = V_{REF} \pm 310\text{mV}$	2.5	—	3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR} = 1.25V$, $V_I(\text{PP}) = 360\text{mV}$	2.5	—	3.5	
	$\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND	—	—	—	

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$ (1)

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Unit	
V_{DD}	Supply Voltage	V_{DDQ}	—	2.7	V	
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V	
V_{REF}	Reference Voltage ($V_{REF} = V_{DDQ}/2$)	1.15	1.25	1.35	V	
V_{TT}	Termination Voltage	$V_{REF} - 40\text{mV}$	V_{REF}	$V_{REF} + 40\text{mV}$	V	
V_I	Input Voltage	0	—	V_{DD}	V	
V_{IH}	AC High-Level Input Voltage	$V_{REF} + 310\text{mV}$	—	—	V	
V_{IL}	AC Low-Level Input Voltage	Data Inputs	—	$V_{REF} - 310\text{mV}$	V	
V_{IH}	DC High-Level Input Voltage	Data Inputs	$V_{REF} + 150\text{mV}$	—	V	
V_{IL}	DC Low-Level Input Voltage	Data Inputs	—	$V_{REF} - 150\text{mV}$	V	
V_{IH}	High-Level Input Voltage	$\overline{\text{RESET}}$	1.7	—	V	
V_{IL}	Low-Level Input Voltage	$\overline{\text{RESET}}$	—	0.7	V	
V_{ICR}	Common-Mode Input Range	CLK, $\overline{\text{CLK}}$	0.97	—	1.53	V
$V_I(\text{PP})$	Peak-to-Peak Input Voltage	CLK, $\overline{\text{CLK}}$	360	—	—	mV
I_{OH}	High-Level Output Current	—	—	-20	mA	
I_{OL}	Low-Level Output Current	—	—	20		
T_A	Operating Free-Air Temperature	0	—	+70	$^\circ\text{C}$	

NOTE:

1. The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter	$V_{DD} = 2.5V \pm 0.2V$		Unit
		Min.	Max.	
CLOCK	Clock Frequency	—	200	MHz
tw	Pulse Duration, CLK, \bar{CLK} HIGH or LOW	2.5	—	ns
tACT	Differential Inputs Active Time ⁽¹⁾	—	22	ns
tINACT	Differential Inputs Inactive Time ⁽²⁾	—	22	ns
tsu	Setup Time, Fast Slew Rate ^(3,5)	Data Before CLK↑, CLK↓	0.75	ns
	Setup Time, Slow Slew Rate ^(4,5)		0.9	ns
tH	Hold Time, Fast Slew Rate ^(3,5)	Data Before CLK↑, CLK ↓	0.75	ns
	Hold Time, Slow Slew Rate ^(2,5)		0.9	ns

NOTES:

1. Data inputs must be low a minimum time of tACT max., after \bar{RESET} is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of tINACT max., after \bar{RESET} is taken LOW.
3. For data signal input slew rate is $\geq 1V/ns$.
4. For data signal input slew rate is $\geq 0.5V/ns$ and $< 1V/ns$.
5. CLK, CLK signal input slew rates are $\geq 1V/ns$.

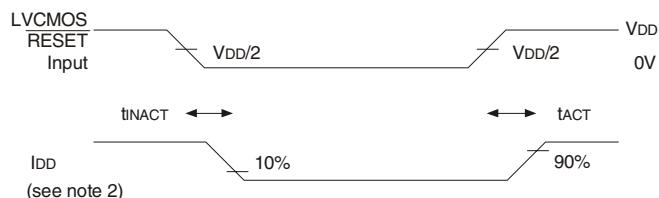
SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

Symbol	Parameter	$V_{DD} = 2.5V \pm 0.2V$		Unit
		Min	Max.	
fMAX		200	—	MHz
tPD	CLK and \bar{CLK} to Q	1.1	2.8	ns
tPHL	RESET to Q	—	5	ns

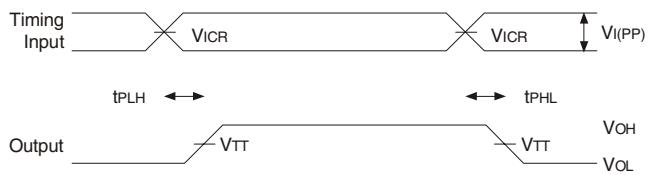
TEST CIRCUITS AND WAVEFORMS (VDD = 2.5V ± 0.2V)



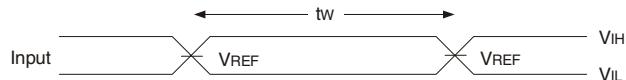
Load Circuit



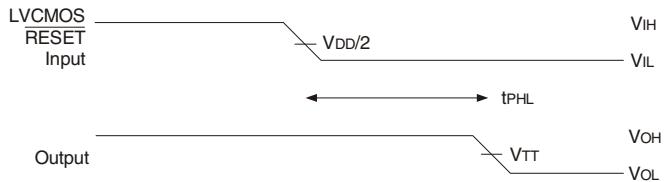
*Voltage and Current Waveforms
Inputs Active and Inactive Times*



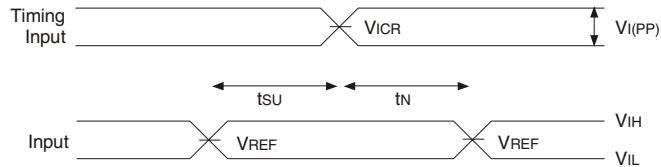
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Setup and Hold Times

NOTES:

1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_o = 0\text{mA}$.
3. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{MHz}$, $Z_o = 50\Omega$, input slew rate = 1 V/ns $\pm 20\%$ (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF} + 310\text{mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMS input.
7. $V_{IL} = V_{REF} - 310\text{mV}$ (AC voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVCMS input.
8. t_{PLH} and t_{PHL} are the same as t_{PD} .

ORDERING INFORMATION

IDT	XX	SSTV	XX	XXXX	XX	
Temp. Range		Family		Device Type	Package	
					PA	Thin Shrink Small Outline Package
					PAG	TSSOP - Green
				857		14-Bit Registered Buffer with SSTL I/O
				16		Double-Density
				74		0°C to +70°C

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