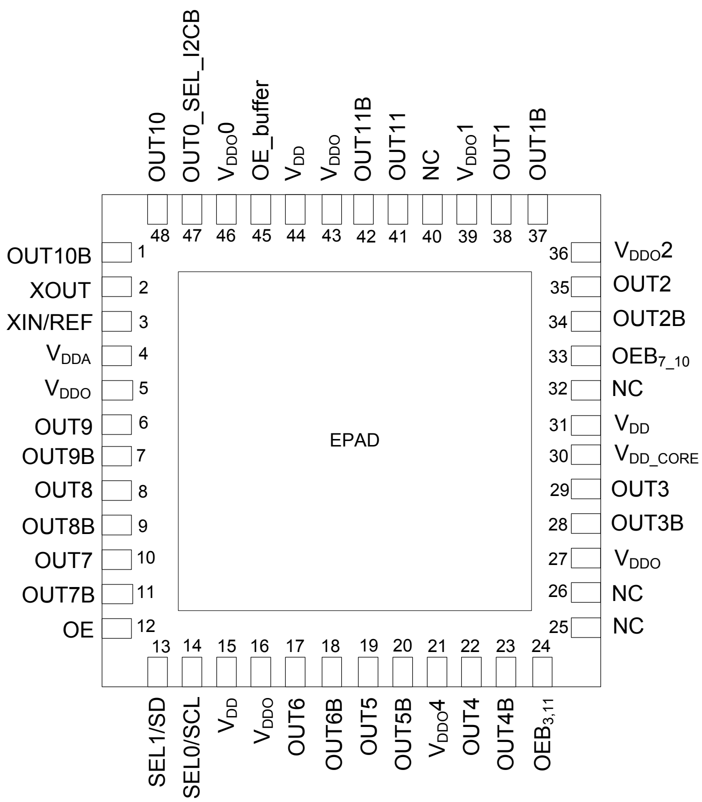
DATASHEET

## Description

The 6P41505 is a system clock generator intended for high performance consumer, networking, industrial, computing, and data-communications applications.

The frequencies are generated from a single reference clock or crystal.

## Pin Assignment

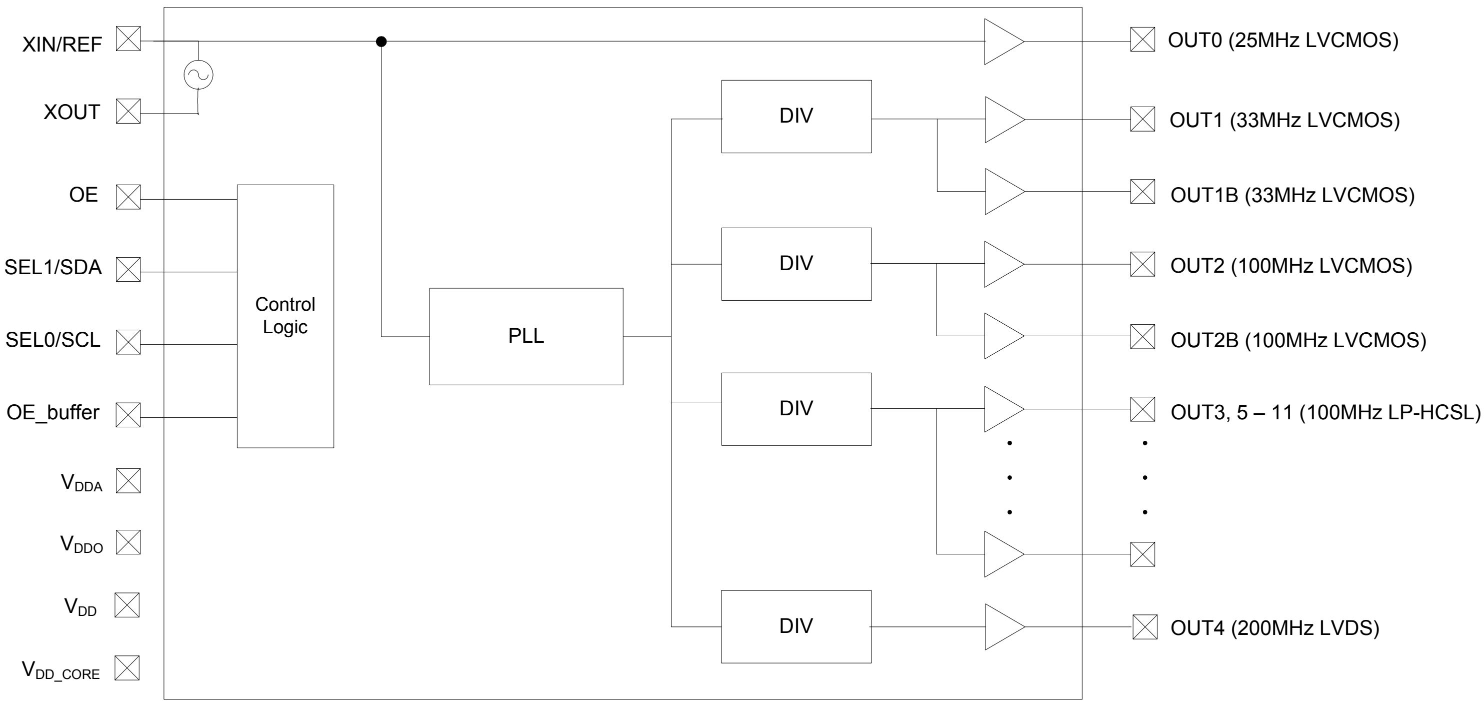



48-pin VFQFPN

## Features

- Default output clocks and frequencies:
  - OUT0: 25MHz LVCMOS. VDDO0 = 3.3V.
  - OUT1: 33MHz or 14.318MHz (6P41505B) LVCMOS x 2(phase aligned). VDDO1=3.3V.
  - OUT2: 100MHz or 48MHz (6P41505B) LVCMOS x 2 (180° phase difference). VDDO2 = 3.3V.
  - OUT3, 5–11: 100MHz PCIe Gen1/2/3 compliant differential LP-HCSL outputs x 8. VDDO3 = 1.8V.
  - OUT4: 200MHz differential LVDS. VDDO4 = 3.3V.
- High performance, low phase noise PLL, < 0.7 ps RMS typical phase jitter on outputs:
  - PCIe Gen1, 2, 3 compliant clock capability
  - USB 3.0 compliant clock capability
  - 1GbE and 10GbE
- Independent Spread Spectrum capability
- $I^2C$ serial programming interface
- 25MHz crystal as input reference
- Power-down mode
- Mixed voltage operation:
  - 1.8V core
  - 1.8V VDDO for 8 LP-HCSL outputs
  - 1.8V to 3.3V VDDO for other outputs (3 differential outputs and 1 reference output)
  - See Pin Descriptions for details
- Available in 48-VFQFPN package
- -40° to +85°C industrial temperature operation

## Functional Block Diagram




## Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1GbE and 10GbE

## Table 1:Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | OUT10B | Output | | Complementary Output Clock 10. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 2 | XOUT | Input | | Crystal Oscillator interface output. |
| 3 | XIN/REF | Input | | Crystal Oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is 1.2V max. Refer to the section “Overdriving the XIN/REF Interface”. |
| 4 | VDDA | Power | | Analog functions power supply pin. Connect to 1.8V. |
| 5 | VDDO | Power | | Connect to 1.8V. Power pin for outputs 3, 5-11 |
| 6 | OUT9 | Output | | Output Clock 9. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 7 | OUT9B | Output | | Complementary Output Clock 9. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 8 | OUT8 | Output | | Output Clock 8. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 9 | OUT8B | Output | | Complementary Output Clock 8. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe application |
| 10 | OUT7 | Output | | Output Clock 7. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe application |
| 11 | OUT7B | Output | | Complementary Output Clock 7. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe application |
| 12 | OE | Input | Internal Pull-down | Active Low Output Enable pin for all outputs.<br>1=disable outputs, 0=enable outputs. This pin has internal pull-down. |
| 13 | SEL1/SDA | Input | Internal Pull-down | Configuration select pin, or I2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor. |
| 14 | SEL0/SCL | Input | Internal Pull-down | Configuration select pin, or I2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull down resistor. |
| 15 | VDD | Power | | Connect to 1.8V |
| 16 | VDDO | Power | | Connect to 1.8V. Power pin for outputs 3, 5-11 |
| 17 | OUT6 | Output | | Output Clock 6. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 18 | OUT6B | Output | | Complementary Output Clock 6. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 19 | OUT5 | Output | | Output Clock 5. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 20 | OUT5B | Output | | Complementary Output Clock 5. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 21 | VDDO4 | Power | | Connect to 3.3V. VDD supply for OUT4 |
| 22 | OUT4 | Output | | Output Clock 4. 200MHz LVDS output. Please refer to the Output Drivers section for more |
| 23 | OUT4B | Output | | Complementary Output Clock 4. 200MHz LVDS output. Please refer to the Output Drivers section for more details. |
| 24 | $OEB_{3,11}$ | Input | Internal Pull-down | Active low Output Enable pin for Outputs 3, 5, 6, 11.<br>1=disable outputs, 0=enable outputs. This pin has internal pull-down. |
| 25 | NC | Input | — | Do not connect |
| 26 | NC | Input | — | Do not connect |
| 27 | VDDO | Power | | Connect to 1.8V. Power pin for outputs 3, 5-11 |
| 28 | OUT3B | Output | | Complementary Output Clock 3. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 29 | OUT3 | Output | | Output Clock 3. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications |
| 30 | VDD_Core | Power | | Connect to 1.8V |
| 31 | VDD | Power | | Connect to 1.8V |
| 32 | NC | Input | | Do not connect |
| 33 | $OEB_{7\_10}$ | Input | Internal Pull-down | Active low Output Enable pin for Outputs 7-10.<br>1=disable outputs, 0=enable outputs. This pin has internal pull-down. |
| 34 | OUT2B | Output | | Complementary Output Clock 2. 100MHz 3.3V LVCMOS output. 180° phase difference with OUT2. Please refer to the Output Drivers section for more details. |
| 35 | OUT2 | Output | | Output Clock 2. 100MHz 3.3V LVCMOS output. Please refer to the Output Drivers section for more details. |

# Pin Descriptions (cont.)

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 36 | VDDO2 | Power | | Connect to 3.3V. VDD supply for OUT2 |
| 37 | OUT1B | Output | | Complementary Output Clock 1. 100MHz 3.3V LVCMOS output. In phase with OUT1. Please refer to the Output Drivers section for more details. |
| 38 | OUT1 | Output | | Output Clock 1. 100MHz 3.3V LVCMOS output. Please refer to the Output Drivers section for more details. |
| 39 | VDDO1 | Power | | Connect to 3.3V. VDD supply for OUT1 |
| 40 | NC | Input | — | Do not connect |
| 41 | OUT11 | Output | | Output Clock 11. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 42 | OUT11B | Output | | Complementary Output Clock 11. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| 43 | VDDO | Power | | Connect to 1.8V. Power pin for outputs 3, 5-11 |
| 44 | VDD | Power | | Connect to 1.8V |
| 45 | OE_buffer | Input | Internal Pull-up | Active High Output enable for outputs 3, 5-11. 0=disable outputs. 1=enable outputs. This pin has internal pull-up. |
| 46 | VDDO0 | Power | | Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0. |
| 47 | OUT0_SEL_I2CB | Output | Internal Pull-down | Latched input/LVCMOS Output. At power up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 13 and 14. If a weak pull up (10Kohms) is placed on OUT0_SEL_I2CB, pins 13 and 14 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull down (10Kohms) is placed on OUT0_SEL_I2CB or it is left floating, pins 13 and 14 will act as the SDA and SCL pins of an I2C interface. After power up, the pin acts as a 3.3V LVCMOS reference output. |
| 48 | OUT10 | Output | | Output Clock 10. 100MHz Low-Power HCSL (LP-HCSL) output for PCIe applications. |
| ePAD | GND | GND | | Connect to ground pad |

# PLL Features and Descriptions

## Spread Spectrum

To help reduce electromagnetic interference (EMI), the 6P41505 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The 6P41505 implements spread spectrum using the Fractional-N output divide, to achieve controllable modulation rate and spreading magnitude. The Spread spectrum can be applied to any output divider and any spread amount from ±0.25% to ±2.5% center spread and -0.5% to -5% down spread.

## Table 2: Loop Filter

PLL loop bandwidth range depends on the input reference frequency (Fref) and can be set between the loop bandwidth range as shown in the table below.

| Input Reference Frequency–Fref (MHz) | Loop Bandwidth Min (kHz) | Loop Bandwidth Max (kHz) |
|---|---|---|
| 5 | 40 | 126 |
| 350 | 300 | 1000 |

## Crystal Input (XIN/REF)

The crystal used should be a fundamental mode quartz crystal; overtone crystals should not be used.

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa so for an accurate oscillation frequency you need to make sure to match the oscillator load capacitance with the crystal load capacitance.

To set the oscillator load capacitance there are two tuning capacitors in the IC, one at XIN and one at XOUT. They can be adjusted independently but commonly the same value is used for both capacitors. The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register. Adjustment of the crystal tuning capacitors allows for maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

### XTAL[5:0] Tuning Capacitor Characteristics

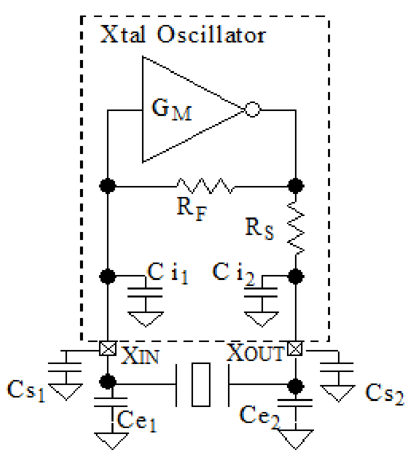
| Parameter | Bits | Step (pF) | Min (pF) | Max (pF) |
|---|---|---|---|---|
| XTAL | 6 | 0.5 | 9 | 25 |

The capacitance at each crystal pin inside the chip starts at 9pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.5pF.

You can write the following equation for this capacitance:

$Ci = 9pF + 0.5pF \times XTAL[5:0]$

The PCB where the IC and the crystal will be assembled adds some stray capacitance to each crystal pin and more capacitance can be added to each crystal pin with additional external capacitors.




You can write the following equations for the total capacitance at each crystal pin:

$C_{XIN} = Ci_1 + Cs_1 + Ce_1$
$C_{XOUT} = Ci_2 + Cs_2 + Ce_2$

$Ci_1$ and $Ci_2$ are the internal, tunable capacitors. $Ci_1$ and $Cs_2$ are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.

$Ce_1$ and $Ce_2$ are additional external capacitors that can be added to increase the crystal load capacitance beyond the tuning range of the internal capacitors. However, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding $Ce_1$ and/or $Ce_2$ to avoid crystal startup issues. $Ce_1$ and $Ce_2$ can also be used to adjust for unpredictable stray capacitance in the PCB.

The final load capacitance of the crystal:

$CL = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$

For most cases it is recommended to set the value for capacitors the same at each crystal pin:

$C_{XIN} = C_{XOUT} = Cx \longrightarrow CL = Cx / 2$

The complete formula when the capacitance at both crystal pins is the same:

$CL = (9pF + 0.5pF \times XTAL[5:0] + Cs + Ce) / 2$

**Example 1**: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs=1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:

$8pF = (9pF + 0.5pF \times XTAL[5:0] + 1.5pF) / 2 \longrightarrow$
$0.5pF \times XTAL[5:0] = 5.5pF \longrightarrow XTAL[5:0] = 11$ (decimal)

**Example 2**: The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. For now we use Cs + Ce = 5pF and the right value for Ce can be determined later to make 5pF together with Cs.

$12pF = (9pF + 0.5pF \times XTAL[5:0] + 5pF) / 2 \longrightarrow$
$XTAL[5:0] = 20$ (decimal)

## OE Pins and Function

### Table 3: OE Pin Function Table

| Pin # | Pin Name | Description | Functions |
|---|---|---|---|
| 12 | OE | OE pin for all outputs. | 1=disable outputs, 0=enable outputs. This pin has internal pull-down. Outputs enabled as default. |
| 24 | OEB3,11 | OE pin for Outputs 3, 5, 6, 11 | 1=disable outputs, 0=enable outputs. This pin has internal pull-down. Outputs enabled as default. |
| 33 | OEB7_10 | OE pin for Outputs 7-10 | 1=disable outputs, 0=enable outputs. This pin has internal pull-down. Outputs enabled as default. |
| 45 | OE_buffer | OE pin for Outputs 3, 5-11 | 0=disable outputs. 1=enable outputs. This pin has internal pull-up. Outputs enabled as default. |

## Output Divides

Each output divide block has a synchronizing POR pulse to provide startup alignment between outputs divides. This allows alignment of outputs for low skew performance. This low skew would also be realized between outputs that are both integer divides from the VCO frequency. This phase alignment works when using configuration with SEL1, SEL0. For $I^2C$ programming, $I^2C$ reset is required.

An output divide bypass mode (divide by 1) will also be provided, to allow multiple buffered reference outputs.

Each of the four output divides are comprised of a 12 bit integer counter, and a 24 bit fractional counter. The output divide can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate a clock frequency accurate to 50 ppb.

Each of the output divides also have structures capable of independently generating spread spectrum modulation on the frequency output.

The Output Divide also has the capability to apply a spread modulation to the output frequency. Independent of output frequency, a triangle wave modulation between 30 and 63kHz may be generated.

For all outputs, there is a bypass mode, to allow the output to behave as a buffered copy of the input.

## Output Skew

For outputs that share a common output divide value, there will be the ability to skew outputs by quadrature values to minimize interaction on the PCB. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. So, for 100 MHz output and a 2800 MHz VCO, you can select how many 11.161pS units you want added to your skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

## Output Drivers

The OUT1 to OUT4 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels

The operating voltage ranges of each output is determined by its independent output power pin ($V_{DDO}$) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential HCSL, LVPECL operation, and 1. 8V, 2.5V, or 3.3V are supported for LVCMOS and differential LVDS operation.

Each output may be enabled or disabled by register bits. When disabled an output will be in a logic 0 state as determined by the programming bit table shown on page 6.

### LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the OUTx and OUTxB outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the OUTx and OUTxB pins. The OUTx and OUTxB outputs can be selected to be phase-aligned with each other or inverted relative to one another by register programming bits. Selection of phase-alignment may have negative effects on the phase noise performance of any part of the device due to increased simultaneous switching noise within the device.

## Device Start-up & Reset Behavior

The 6P41505 has an internal power-up reset (POR) circuit. The POR circuit will remain active for a maximum of 10ms after device power-up.

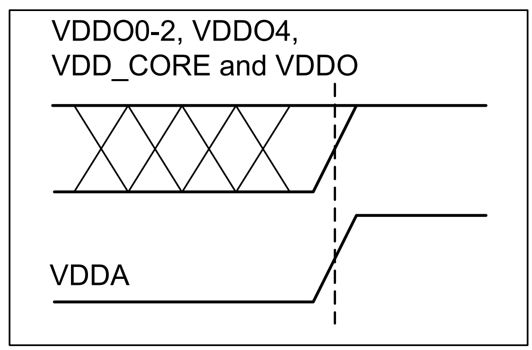
Upon internal POR circuit expiring, the device will exit reset and begin self-configuration.

The device will load internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the selected source and begin operation.

## Power Up Ramp Sequence

VDDA and VDD must ramp up together. VDD0-1, VDDO4, VDD_CORE and VDDO must ramp up before, or concurrently with, VDD0-1, VDDO4, VDD_CORE and VDDO. All power supply pins must be connected to a power rail even if the output is unused. All power supplies must ramp in a linear fashion and ramp monotonically.



## $I^2C$ Mode Operation

The device acts as a slave device on the $I^2C$ bus using one of the two $I^2C$ addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical $I^2C$ compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-down resistors have a size of 100kΩ typical.


## $I^2C$ Slave Read and Write Cycle Sequencing

## Table 4: $I^2C$ Bus DC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | | 0.7xVDD | | | V |
| $V_{IL}$ | Input LOW Level | | | | 0.3xVDD | V |
| $V_{HYS}$ | Hysteresis of Inputs | | 0.05xVDD | | | V |
| $I_{IN}$ | Input Leakage Current | | -1 | | 30 | µA |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 3 mA | | | 0.4 | V |

## Table 5: $I^2C$ Bus AC Characteristics

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | Serial Clock Frequency (SCL) | | 10 | | 400 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START | | 1.3 | | | µs |
| $t_{SU:START}$ | Setup Time, START | | 0.6 | | | µs |
| $t_{HD:START}$ | Hold Time, START | | 0.6 | | | µs |
| $t_{SU:DATA}$ | Setup Time, data input (SDA) | | 100 | | | ns |
| $t_{HD:DATA}$ | Hold Time, data input (SDA) [1] | | 0 | | | µs |
| $t_{OVD}$ | Output data valid from clock | | | | 0.9 | µs |
| $C_B$ | Capacitive Load for Each Bus Line | | | | 400 | pF |
| $t_R$ | Rise Time, data and clock (SDA, SCL) | | 20 + 0.1x$C_B$ | | 300 | ns |
| $t_F$ | Fall Time, data and clock (SDA, SCL) | | 20 + 0.1x$C_B$ | | 300 | ns |
| $t_{HIGH}$ | HIGH Time, clock (SCL) | | 0.6 | | | µs |
| $t_{LOW}$ | LOW Time, clock (SCL) | | 1.3 | | | µs |
| $t_{SU:STOP}$ | Setup Time, STOP | | 0.6 | | | µs |

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH}$(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

## Table 6: Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 6P41505. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DDA}$, $V_{DDD}$, $V_{DDO}$ | 3.465V |
| Inputs<br>XIN/REF | <br>0V to 1.2V voltage swing |
| Outputs, $V_{DDO}$ (LVCMOS) | -0.5V to VDDO+ 0.5V |
| Outputs, $I_O$ (SDA) | 10mA |
| Package Thermal Impedance, $\Theta_{JA}$ | 42°C/W (0 mps) |
| Package Thermal Impedance, $\Theta_{JC}$ | 41.8°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |

## Table 7: Recommended Operation Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDx}$ | Power supply voltage for supporting 1.8V outputs | 1.71 | 1.8 | 1.89 | V |
| $V_{DDA}$ | Analog power supply voltage. Use filtered analog power supply if available. | 1.71 | | 1.89 | V |
| $T_A$ | Operating temperature, ambient | -40 | | 85 | °C |
| $C_{LOAD\_OUT}$ | Maximum load capacitance (3.3V LVCMOS only) | | | 15 | pF |
| $F_{IN}$ | External reference crystal | 8 | | 40 | MHz |
| $t_{PU}$ | Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | | 5 | ms |

## Table 8: Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance ($T_A$ = +25 °C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CIN | Input Capacitance (SD/OE, SEL1/SDA, SEL0/SCL) | | 3 | 7 | pF |
| Pull-down Resistor | | 100 | | 300 | kΩ |
| ROUT | LVCMOS Output Driver Impedance (VDDO = 1.8V, 2.5V, 3.3V) | | 17 | | Ω |
| XIN/REF | Programmable capacitance at XIN/REF | 9 | | 25 | pF |
| XOUT | Programmable capacitance at XOUT | 9 | | 25 | pF |

## Table 9: Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 8 | 25 | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | 10 | 100 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Load Capacitance (CL) @ <=25 MHz | | 6 | 8 | 12 | pF |
| Load Capacitance (CL) >25M to 40M | | 6 | | 8 | pF |
| Maximum Crystal Drive Level | | | | 100 | µW |

## Table 10: DC Electrical Characteristics

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Iddcore[3] | Core Supply Current | 100 MHz on all outputs, 25 MHz REFCLK | | 44 | | mA |
| Iddox | Output Buffer Supply Current | LVPECL, 350 MHz, 3.3V VDDOx | | 42 | 47 | mA |
| | | LVPECL, 350 MHz, 2.5V VDDOx | | 37 | 42 | mA |
| | | LVDS, 350 MHz, 3.3V VDDOx | | 18 | 21 | mA |
| | | LVDS, 350 MHz, 2.5V VDDOx | | 17 | 20 | mA |
| | | LVDS, 350 MHz, 1.8V VDDOx | | 16 | 19 | mA |
| | | HCSL, 250 MHz, 3.3V VDDOx, 2 pF load | | 29 | 33 | mA |
| | | HCSL, 250 MHz, 2.5V VDDOx, 2 pF load | | 28 | 33 | mA |
| | | LVCMOS, 50 MHz, 3.3V, VDDOx [1,2] | | 16 | 18 | mA |
| | | LVCMOS, 50 MHz, 2.5V, VDDOx [1,2] | | 14 | 16 | mA |
| | | LVCMOS, 50 MHz, 1.8V, VDDOx [1,2] | | 12 | 14 | mA |
| | | LVCMOS, 200 MHz, 3.3V VDDOx[1] | | 36 | 42 | mA |
| | | LVCMOS, 200 MHz, 2.5V VDDOx[1,2] | | 27 | 32 | mA |
| | | LVCMOS, 200 MHz, 1.8V VDDOx[1,2] | | 16 | 19 | mA |
| Iddpd | Power Down Current | SD asserted, I2C Programming | | 10 | 14 | mA |

1. Single CMOS driver active.
2. Measured into a 5” 50 Ohm trace with 2 pF load.
3. Iddcore = IddA+ IddD, no loads.

## Table 11: DC Electrical Characteristics for 3.3V LVCMOS ($V_{DDO}$ = 3.3V±5%, TA = -40°C to +85°C)[1]

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = -15mA | 2.4 | | VDDO | V |
| VOL | Output LOW Voltage | IOL = 15mA | | | 0.4 | V |
| IOZDD | Output Leakage Current (OUT1,2,4) | Tri-state outputs, VDDO = 3.465V | | | 5 | μA |
| IOZDD | Output Leakage Current (OUT0) | Tri-state outputs, VDDO = 3.465V | | | 30 | μA |
| VIH | Input HIGH Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | 0.7xVDDO | | VDDD + 0.3 | V |
| VIL | Input LOW Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | GND - 0.3 | | 0.8 | V |
| VIH | Input HIGH Voltage | Single-ended input OUT0_SEL_I2CB | 2 | | VDDO0 + 0.3 | V |
| VIL | Input LOW Voltage | Single-ended input OUT0_SEL_I2CB | GND - 0.3 | | 0.4 | V |
| VIH | Input HIGH Voltage | Single-ended input - XIN/REF | 0.8 | | 1.2 | V |
| VIL | Input LOW Voltage | Single-ended input - XIN/REF | GND - 0.3 | | 0.4 | V |
| TR/TF | Input Rise/Fall Time | SD/OE, SEL1/SDA, SEL0/SCL | | | 300 | nS |

1. See “Recommended Operating Conditions” table.

## Table 12: DC Electrical Characteristics for 2.5V LVCMOS ($V_{DDO}$ = 2.5V±5%, TA = -40°C to +85°C)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = -12mA | 0.7xVDDO | | | V |
| VOL | Output LOW Voltage | IOL = 12mA | | | 0.4 | V |
| IOZDD | Output Leakage Current (OUT1,2,4) | Tri-state outputs, VDDO = 2.625V | | | 5 | μA |
| IOZDD | Output Leakage Current (OUT0) | Tri-state outputs, VDDO = 2.625V | | | 30 | μA |
| VIH | Input HIGH Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | 1.7 | | VDDD + 0.3 | V |
| VIL | Input LOW Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | GND - 0.3 | | 0.8 | V |
| VIH | Input HIGH Voltage | Single-ended input OUT0_SEL_I2CB | 1.7 | | VDDO0 + 0.3 | V |
| VIL | Input LOW Voltage | Single-ended input OUT0_SEL_I2CB | GND - 0.3 | | 0.4 | V |
| VIH | Input HIGH Voltage | Single-ended input - XIN/REF | 0.8 | | 1.2 | V |
| VIL | Input LOW Voltage | Single-ended input - XIN/REF | GND - 0.3 | | 0.4 | V |
| TR/TF | Input Rise/Fall Time | SD/OE, SEL1/SDA, SEL0/SCL | | | 300 | nS |

## Table 13: DC Electrical Characteristics for 1.8V LVCMOS ($V_{DDO}$ = 1.8V±5%, TA = -40°C to +85°C)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | IOH = -8mA | 0.7 x$V_{DDO}$ | | $V_{DDO}$ | V |
| $V_{OL}$ | Output LOW Voltage | IOL = 8mA | | | 0.25 x $V_{DDO}$ | V |
| $I_{OZDD}$ | Output Leakage Current (OUT1,2,4) | Tri-state outputs, VDDO = 3.465V | | | 5 | μA |
| | Output Leakage Current (OUT0) | Tri-state outputs, VDDO = 3.465V | | | 30 | |
| $V_{IH}$ | Input HIGH Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | 0.65 * $V_{DDD}$ | | $V_{DDD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | Single-ended inputs - SD/OE, SEL1/SDA, SEL0/SCL | GND - 0.3 | | 0.35 * $V_{DDD}$ | V |
| $V_{IH}$ | Input HIGH Voltage | Single-ended input OUT0_SEL_I2CB | 0.65 * $V_{DDD}$ | | $V_{DDD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | Single-ended input OUT0_SEL_I2CB | GND - 0.3 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | Single-ended input - XIN/REF | 0.8 | | 1.2 | V |
| $V_{IL}$ | Input LOW Voltage | Single-ended input - XIN/REF | GND - 0.3 | | 0.4 | V |
| TR/TF | Input Rise/Fall Time | SEL0/SCL | | | 300 | nS |

## Table 14: DC Electrical Characteristics for LVDS ($V_{DDO}$ = 3.3V±5% or 2.5V±5%, TA = -40°C to +85°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OT}$ (+) | Differential Output Voltage for the TRUE binary state | 247 | | 454 | mV |
| $V_{OT}$ (-) | Differential Output Voltage for the FALSE binary state | -247 | | -454 | mV |
| $\triangle V_{OT}$ | Change in $V_{OT}$ between Complimentary Output States | | | 50 | mV |
| $V_{OS}$ | Output Common Mode Voltage (Offset Voltage) | 1.125 | 1.25 | 1.375 | V |
| $\triangle V_{OS}$ | Change in $V_{OS}$ between Complimentary Output States | | | 50 | mV |
| $I_{OS}$ | Outputs Short Circuit Current, $V_{OUT}$+ or $V_{OUT}$ - = 0V or $V_{DDO}$ | | 9 | 24 | mA |
| $I_{OSD}$ | Differential Outputs Short Circuit Current, $V_{OUT}$+ = $V_{OUT}$ - | | 6 | 12 | mA |

## Table 15: DC Electrical Characteristics for LVDS ($V_{DDO}$ = 1.8V±5%, TA = -40°C to +85°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OT}$ (+) | Differential Output Voltage for the TRUE binary state | 247 | | 454 | mV |
| $V_{OT}$ (-) | Differential Output Voltage for the FALSE binary state | -247 | | -454 | mV |
| $\Delta V_{OT}$ | Change in VOT between Complimentary Output States | | | 50 | mV |
| $V_{OS}$ | Output Common Mode Voltage (Offset Voltage) | 0.8 | 0.875 | 0.95 | V |
| $\Delta V_{OS}$ | Change in VOS between Complimentary Output States | | | 50 | mV |
| $I_{OS}$ | Outputs Short Circuit Current, $V_{OUT}$+ or $V_{OUT}$ - = 0V or $V_{DD}$ | | 9 | 24 | mA |
| $I_{OSD}$ | Differential Outputs Short Circuit Current, $V_{OUT}$+ = $V_{OUT}$ - | | 6 | 12 | mA |

## Table 16: Electrical Characteristics – DIF 0.7V Regular HCSL Outputs (TA = -40°C to +85°C)

(For OUT1, OUT2 and OUT4 programmable differential output pairs when configured as HCSL outputs.),

TA = $T_{COM}$ or $T_{IND;}$ Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | Trf | Scope averaging on | 1 | | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | | 20 | % | 1, 2, 4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | | 850 | mV | 1,7 |
| Voltage Low | $V_{LOW}$ | | -150 | | 150 | | 1,7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | | | mV | 1,2,7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | | 550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | | 140 | mV | 1, 6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Table 17: Electrical Characteristics–Low Power HCSL (LP-HCSL) Outputs

(For OUT3 and OUT5–11 LP-HCSL differential output pairs.)

TA = TAMB; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | $t_{RF}$ | Scope averaging on | 1 | 2.5 | 4 | V/ns | 1,2,3 |
| Slew rate matching | dV/dt | Slew rate matching, Scope averaging on | | 7 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 0 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | 0 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 0 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | 0 | | | 7 |
| Vswing | Vswing | Scope averaging off | 300 | 0 | | mV | 1,2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 0 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 0 | 140 | mV | 1,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

# Table 18: AC Timing Electrical Characteristics

($V_{DDO}$ = 1.8V ±5%, TA = -40°C to +85°C)
(Spread Spectrum Generation = OFF)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ [1] | Input Frequency | Input frequency limit (XIN) | 8 | | 40 | MHz |
| | | Input frequency limit (REF) | 1 | | 200 | MHz |
| $f_{OUT}$ | Output Frequency | Single ended clock output limit (LVCMOS) | 1 | | 200 | MHz |
| | | Differential clock output limit | 1 | | 350 | |
| $f_{VCO}$ | VCO Frequency | VCO operating frequency range | 2500 | 2800 | 3000 | MHz |
| $f_{PFD}$ | PFD Frequency | PFD operating frequency range | 1 [1] | | 150 | MHz |
| $f_{BW}$ | Loop Bandwidth | Input frequency = 25MHz | 0.06 | | 0.9 | MHz |
| t2 | Input Duty Cycle | Duty Cycle | 45 | | 55 | % |
| t3 | Output Duty Cycle | All differential outputs except Reference output | 45 | 50 | 55 | % |
| | | Measured at VDD/2, all outputs except Reference output 2.5V and 3.3V | 45 | 50 | 55 | % |
| | | Measured at VDD/2, all outputs except Reference output 1.8V | 40 | 50 | 60 | % |
| | | Measured at VDD/2, Reference output (150.1MHz - 200MHz) with 50% input | 40 | 50 | 60 | % |
| | | Measured at VDD/2, Reference output(s) (120.1MHz - 200MHz) | 30 | 50 | 70 | % |
| t4 | Slew Rate, SLEW[1:0] = 00 | Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDD=3.3V | 1.5 | 2.6 | 4.0 | V/ns |
| | Slew Rate, SLEW[1:0] = 01 | | 1.3 | 2.4 | 3.8 | |
| | Slew Rate, SLEW[1:0] = 10 | | 1.2 | 2.3 | 3.7 | |
| | Slew Rate, SLEW[1:0] = 11 | | 1.0 | 2.2 | 3.6 | |
| | Slew Rate, SLEW[1:0] = 00 | Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDD=2.5V | 1.0 | 1.7 | 2.7 | |
| | Slew Rate, SLEW[1:0] = 01 | | 0.8 | 1.5 | 2.5 | |
| | Slew Rate, SLEW[1:0] = 10 | | 0.7 | 1.4 | 2.45 | |
| | Slew Rate, SLEW[1:0] = 11 | | 0.6 | 1.3 | 2.39 | |
| | Slew Rate, SLEW[1:0] = 00 | Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of VDDO (Output Load = 5 pF) VDD=1.8V | 1.5 | 2.6 | 4.0 | |
| | Slew Rate, SLEW[1:0] = 01 | | 1.3 | 2.4 | 3.8 | |
| | Slew Rate, SLEW[1:0] = 10 | | 1.2 | 2.3 | 3.75 | |
| | Slew Rate, SLEW[1:0] = 11 | | 1.0 | 2.2 | 3.67 | |
| t5 | Rise Times | LVDS, 20% to 80% | | 300 | | ps |
| | Fall Times | LVDS, 80% to 20% | | 300 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| t6 | Clock Jitter | Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs | | 46 | | ps |
| | | Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs | | 74 | | ps |
| | | RMS Phase Jitter (12kHz to 5MHz integration range) reference clock (OUT0), 25 MHz LVCMOS outputs | | 0.5 | | ps |
| | | RMS Phase Jitter (12kHz to 20MHz integration range) differential output, 25MHz crystal, 156.25MHz on OUT2, and 100MHz LP-HCSL outputs on OUT3, OUT5-11. | | 0.75 | 1.5 | ps |
| t7 | Output Skew between OUT1, OUT2, OUT4 | Skew between the same frequencies , with outputs using the same driver format and phase delay set to 0 ns. | | 75 | | ps |
| | Output Skew between OUT3 and OUT5-11 | Skew between outputs at same frequency and conditions | 49.5 | | 84 | ps |
| t8 [3] | Lock Time | PLL lock time from power-up | | 10 | 20 | ms |
| t9 [4] | Lock Time | PLL lock time from shutdown mode | | 3 | 4 | ms |

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.
4. Actual PLL lock time depends on the loop configuration.
5. Spread Spectrum generation is off unless otherwise stated.

## Table 19: PCI Express Jitter Specifications ($V_{DDO}$ = 1.8V ±5%, $T_A$ = -40°C to +85°C)

(For LP-HCSL(OUT3, OUT5-11) outputs)

| Symbol | Parameter | Conditions | Min | Typ | Max | PCIe Industry Specification | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| $t_J$ (PCIe Gen1) | Phase Jitter Peak-to-Peak | ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 23.85 | | 86 | ps | 1,4 |
| $t_{REFCLK\_HF\_RMS}$ (PCIe Gen2) | Phase Jitter RMS | ƒ = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 1.83 | | 3.1 | ps | 2,4 |
| $t_{REFCLK\_LF\_RMS}$ (PCIe Gen2) | Phase Jitter RMS | ƒ = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 0.54 | | 3 | ps | 2,4 |
| $t_{REFCLK\_RMS}$ (PCIe Gen3) | Phase Jitter RMS | ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.51 | | 1 | ps | 3,4 |

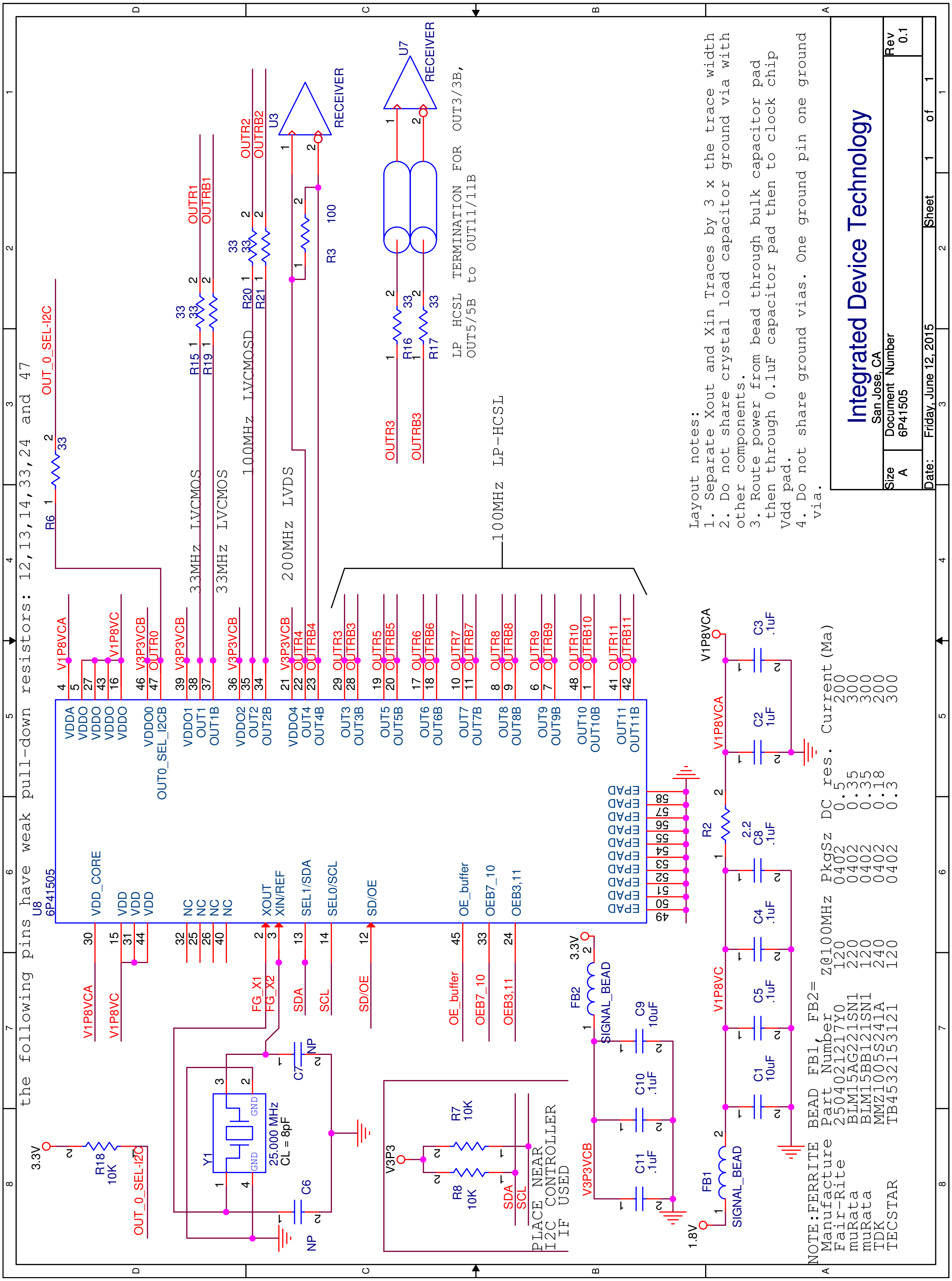
Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

1. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1.
2. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
3. RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI_Express_Base_r3.0 10 Nov, 2010 specification, and is subject to change pending the final release version of the specification.
4. This parameter is guaranteed by characterization. Not tested in production.

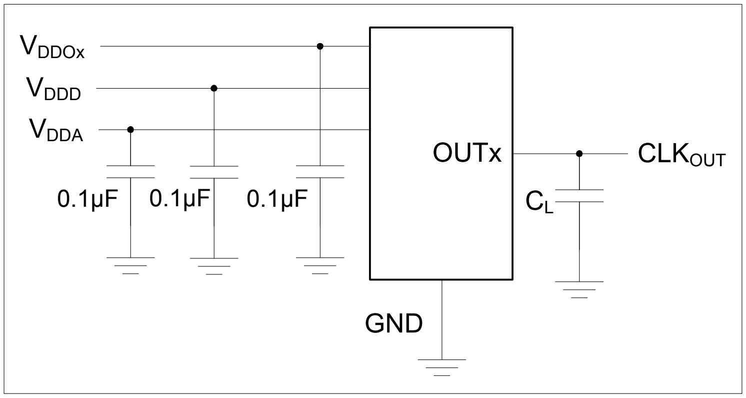
## Table 20: Spread Spectrum Generation Specifications

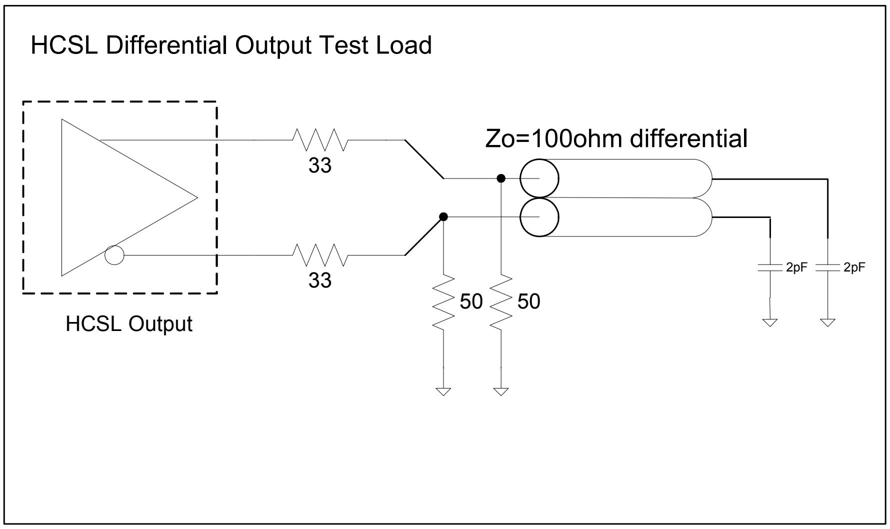
| Symbol | Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Output Frequency Range | 1 | | 300 | MHz |
| $f_{MOD}$ | Mod Frequency | Modulation Frequency | 30 to 63 | | | kHz |
| $f_{SPREAD}$ | Spread Value | Amount of Spread Value (programmable) - Center Spread | ±0.25% to ±2.5% | | | $\%f_{OUT}$ |
| | | Amount of Spread Value (programmable) - Down Spread | -0.5% to -5% | | | |

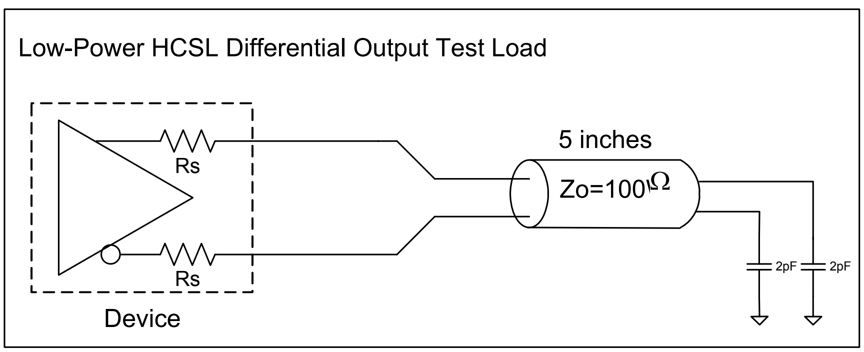
# 6P41505 Reference Schematic



## Test Circuits and Loads



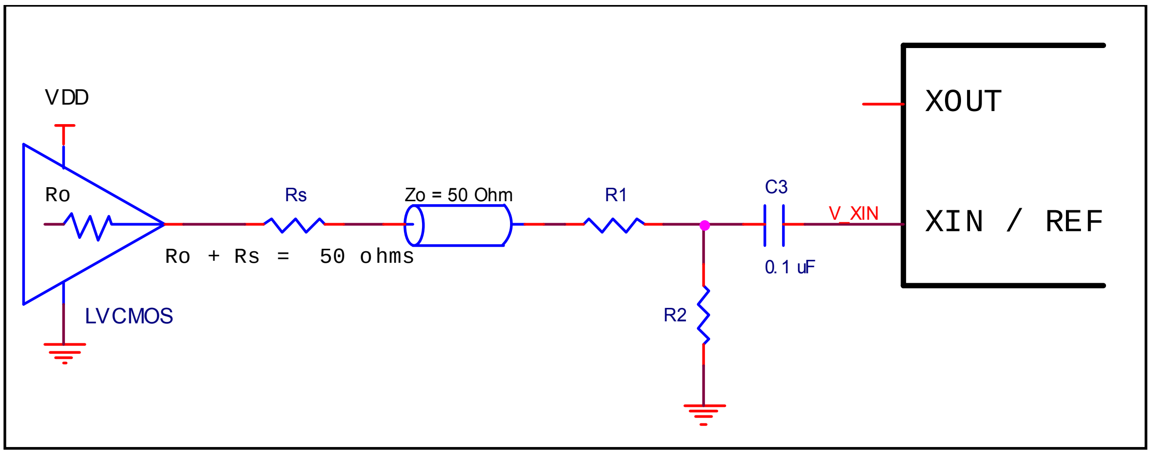



# Overdriving the XIN/REF Interface

## LVCMOS Driver

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V and the slew rate should not be less than 0.2V/ns. Figure General Diagram for LVCMOS Driver to XTAL Input Interface shows an example of the interface diagram for a LVCMOS driver.

This configuration has three properties; the total output impedance of Ro and Rs matches the 50 ohm transmission line impedance, the Vrx voltage is generated at the CLKIN inputs which maintains the LVCMOS driver voltage level across the transmission line for best S/N and the R1-R2 voltage divider values ensure that the clock level at XIN is less than the maximum value of 1.2V.




**General Diagram for LVCMOS Driver to XTAL Input Interface**

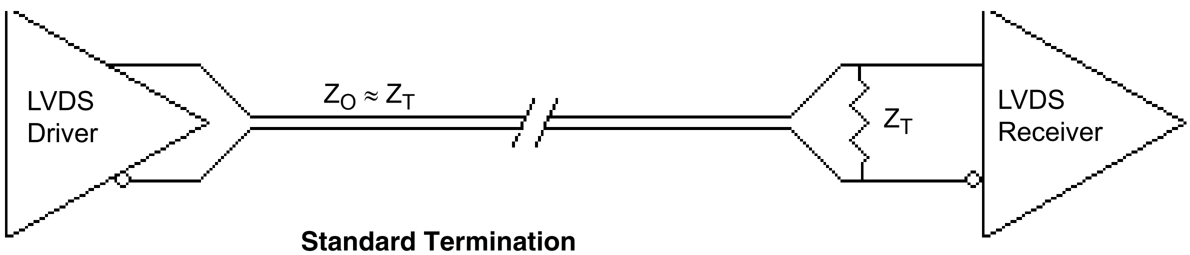
Table 21 *Nominal Voltage Divider Values vs LVCMOS VDD for XIN* shows resistor values that ensure the maximum drive level for the XIN/REF port is not exceeded for all combinations of 5% tolerance on the driver VDD, the VersaClock VDDA and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the voltage divider attenuation as long as the minimum drive level is maintained over all tolerances. To assist this assessment, the total load on the driver is included in the table.

### Table 21: Nominal Voltage Divider Values vs LVCMOS VDD for XIN

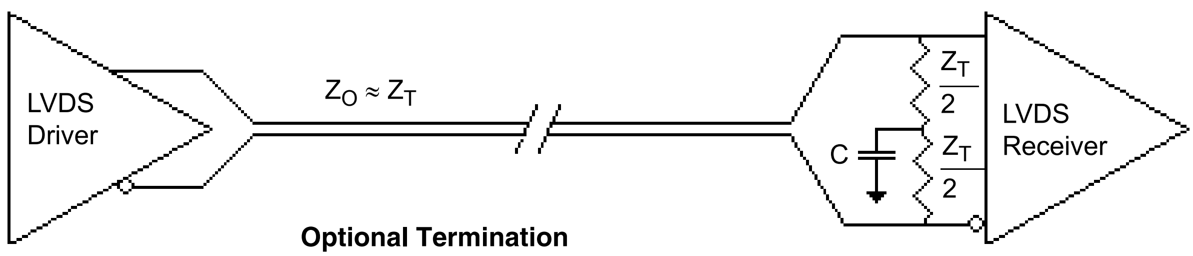
| LVCMOS Driver VDD | Ro+Rs | R1 | R2 | V_XIN (peak) | Ro+Rs+R1+R2 |
|---|---|---|---|---|---|
| 3.3 | 50.0 | 130 | 75 | 0.97 | 255 |
| 2.5 | 50.0 | 100 | 100 | 1.00 | 250 |
| 1.8 | 50.0 | 62 | 130 | 0.97 | 242 |

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω. and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω. differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure *Standard Termination* or the termination of figure *Optional Termination* can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the IDT LVDS output. If using a non-standard termination, it is recommended to contact IDT and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100 ohm shunt load. If AC coupling is required, the coupling caps must be placed between the 100 ohm shunt termination and the receiver. In this manner the termination of the LVDS output remains DC coupled




**Standard Termination**




**Optional Termination**

# PCI Express Application Note

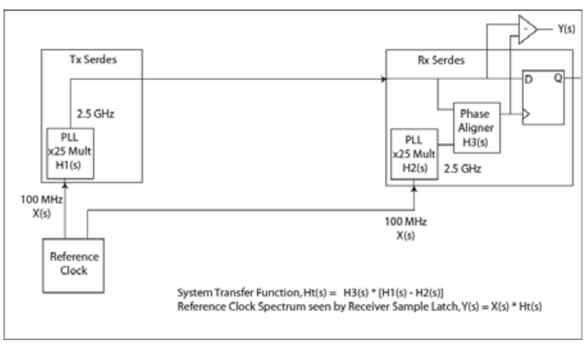
PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used Common Clock Architecture in which a copy of the reference clock is provided to both ends of the PCI Express Link. In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

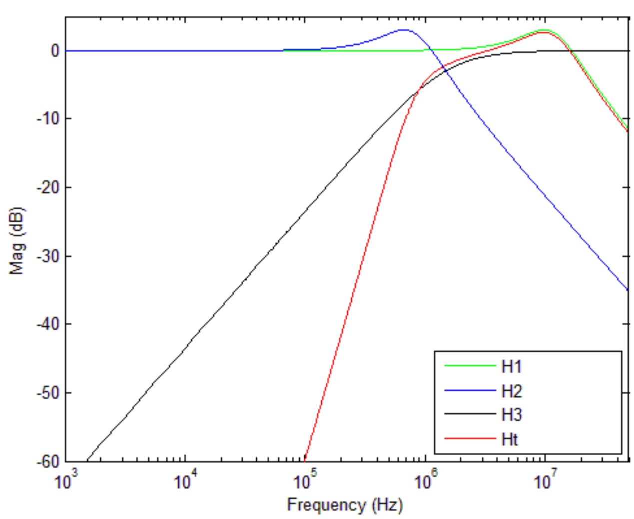
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



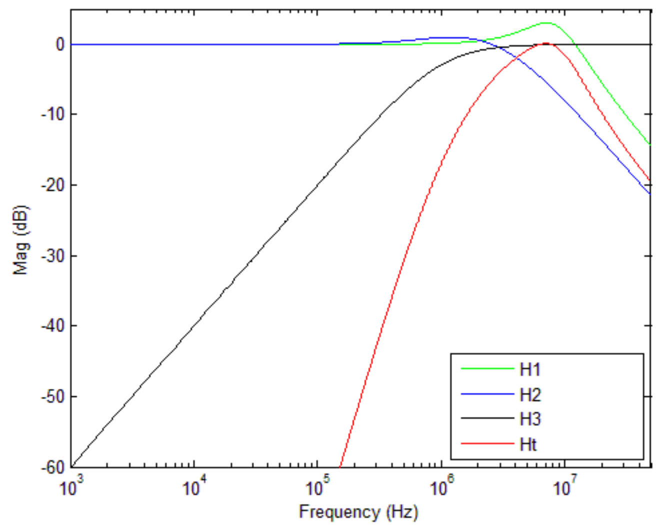

### PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

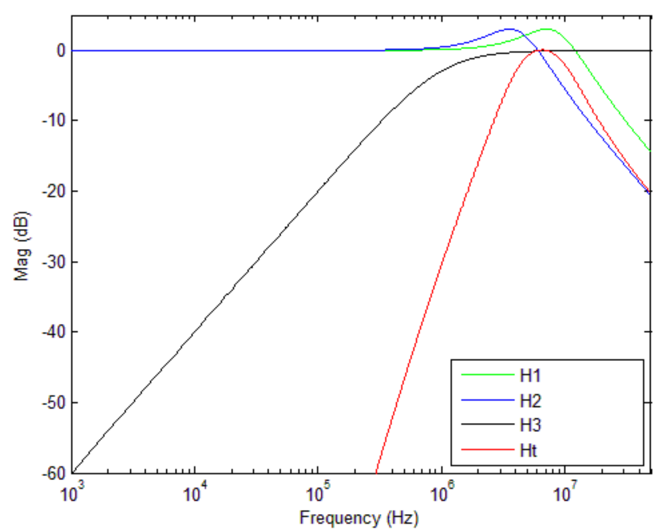



### PCIe Gen1 Magnitude of Transfer Function

For PCI Express Gen2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

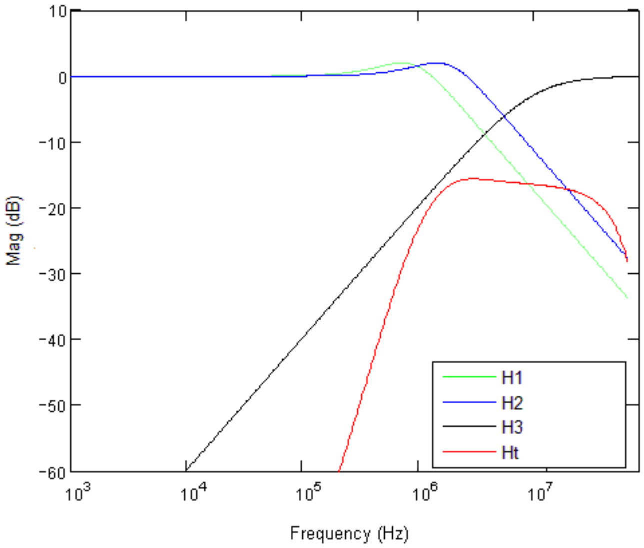



### PCIe Gen2A Magnitude of Transfer Function




### PCIe Gen2B Magnitude of Transfer Function

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.




**PCIe Gen3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note PCI Express Reference Clock Requirements.

## Marking Diagrams

| IDT6P41505NDGI | IDT6P41505BNDGI |
|---|---|
| IDT6P415<br>05NDGI<br>YYWW$<br>● LOT | IDT6P415<br>05BNDGI<br>YYWW$<br>● LOT |

1. “G” denotes RoHS compliance.
2. “I” denotes industrial temperature.
3. “YYWW” is the two last digits of the year and week that the part was assembled.
4. “$” denotes mark code.
5. “LOT” denotes lot number.

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 6P41505NDGI | Trays | 48-VFQFPN | -40° to +85°C |
| 6P41505NDGI8 | Tape and Reel | 48-VFQFPN | -40° to +85°C |
| 6P41505BNDGI | Trays | 48-VFQFPN | -40° to +85°C |
| 6P41505BNDGI8 | Tape and Reel | 48-VFQFPN | -40° to +85°C |

**"ddd" denotes the dash code.**
**"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.**

## Revision History

| Date | Description of Change |
|---|---|
| May 1, 2019 | • Updated Features bullets to include frequencies for 6P41505B.<br>• Updated Ordering Information.<br>• Added package outline drawings link. |
| March 24, 2016 | Released to final. |

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