IDT82V2048L Data Sheet Change Notice

Supplemental Information

This notice describes the differences between the updated version and its previous version of the IDT82V2048L Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
July 29, 2005	-	-	28 - 1

Changed Items

July 29, 2005

Item 28: Added IDT Green package options for PBGA and TQFP. (Page 1, 48)

Item 27: Updated MCn pin description in Table-1 ‘Pin Description’. (Page 9)

Item 26: Updated the description of TCK pin and added TDO pin in Table-1 ‘Pin Description’. (Page 9, 10)

Item 25: Updated T1 VDDT supply specification in Table-1 ‘Pin Description’, Table-6 ‘External Component Values’, section ‘Transmit Driver Power Supply’ and ‘Recommended Operating Conditions’ table and ‘Power Consumption’ table. (Page 10, 15, 35, 36)

Item 24: Updated the description of CLKE pin for RDPn, RDNn, SCLK and SDO pins in Table-1 ‘Pin Description’, and section 'Clock Edges'; updated Table-3 ‘Active Clock Edge and Active Level’ (Page 4, 5, 7, 8, 13)

Item 23: Updated LOS declare/clear value in Table-4 ‘LOS Condition’ and Table ‘Receiver Characteristics’; added a note in Table-4 ‘LOS Condition’. (Page 13, 38)

Item 22: Updated section ‘Power Driver Failure Monitor’. (Page 15)

Item 21: Added ‘Transmit Line Side Short Circuit’ section. (Page 15)

Item 20: Updated section ‘Reset’ and changed the headline ‘Reset’ into ‘Software Reset’. (Page 17)

Item 19: Updated section ‘Power Up’ and changed the headline ‘Power Up’ into ‘Power on Reset’.(Page 17)

Item 18: Updated section ‘Interrupt Handling’ and ‘Register List and Map’. (Page 19, 20)

Item 17: Updated section ‘Reserved and Test Registers’. (Page 20)

Item 16: Added Remote Loopback option in section ‘G.772 Monitoring’, ‘Register List and Map’, Table-9 ‘Primary Register List’ and Table-11 ‘Primary Register Map’. (Page 16, 20, 22)

Item 15: Updated bit 0-7 description of register ‘GCF’ and ‘OE’ in Table-11 ‘Primary Register Map’. (Page 22, 23)

Item 14: Removed a note about register ‘DF’. (Page 25)

Item 13: Updated the description of register ‘e-AFE’. (Page 28)

Item 12: Updated bit #85 from ‘RDN5’ to ‘RDN6’ and bit #87 from ‘HZEN’ to ‘HZEN6’ in Table-15 ‘Boundary Scan Register Description’. (Page 32)

Item 11: Updated ‘Iin’ section in ‘Absolute Maximum Rating’ table. (Page 35)

Item 10: Updated typical ‘Isc’ value and Note 3 in ‘Transmitter Characteristics’ table. (Page 37)

Item 9: Changed the table title from ‘DC Characteristics’ to ‘Receiver Characteristics’. (Page 38)

Item 8: Extended ‘IA’ value and ‘SIR’ value; changed Note 2 in ‘Receiver Characteristics’ table (Page 38)

Item 7: Changed the unit for ‘SRE’ from ‘dB’ to ‘%’ in ‘Receiver Characteristics’ table. (Page 38)

Item 6: Updated Note 1 and 2; removed Note 3 and 4 from ‘Transceiver Timing Characteristics’ table. (Page 39)

Item 5: Updated MCLK frequency in ‘Transceiver Timing Characteristics’ table. (Page 39)

Item 4: Updated receive path timing 't4' to 't9' in 'Transceiver Timing Characteristics' table; updated Figure-15 Receive System Interface Timing. (Page 39, 40)

Item 3: Changed 'A[7:0]' into 'A[4:0]' for non-multiplexed read/write timing in Figure-17, Figure-19, Figure-21 and Figure-23. (Page 43, 44, 45, 46)

Item 2: Updated 't8' and 't9' timing in Figure-22 'Multiplexed Motorola Mode Read Timing'. (Page 45)

Item 1: Changed 't10' value in 'Serial Host Interface Timing Characteristics' table and added 't10' in Serial Interface Read Timing figures Figure-26 and Figure-27. (Page 47)

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2024 Renesas Electronics Corporation. All rights reserved.