IDT82P2284 Data Sheet Change Notice

Supplemental Information

This notice describes the differences between the updated version (Version 6, dated Feb 25, 2008) and its previous version (Version 5, dated April 6, 2007) of the IDT82P2284 Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
Feb 25, 2008	-	-	26
April 6, 2007	-	-	25 - 15
April 27, 2004	-	-	14
March 22, 2004	T-0403-06	Zyyww	13 - 4
March 22, 2004		Zbyyww	13 - 1

Changed Items

Feb 25, 2008

Item 26: Updated Figure 21~24 and Figure 28~31 to clarify the F-bit in T1/J1 mode. (Page 74, 75, 76, 83, 84, 85)

April 6, 2007

Item 25: Removed the functional descriptions of the SS7 protocol support. (Page 11, 59, 61, 62, 95, 201, 202, 205, 208, 209, 213, 303, 304, 307, 310, 311, 315)

Item 24: Added section '3.2.1 Line Monitor'. (Page 24, 25, 26)

Item 23: Changed the E1 mode 'CRCM, SIGEN, GENCRC' bite control table to text description. (Page 285)

Item 22: Changed the figure 'Read Operation In SPI Mode' and figure 'Write Operation In SPI Mode'. (Page 117)

Item 21: Added line driver setting to '3.27.2.6 Analog Loopback'. (Page 112)

Item 20: Changed the paragragh about transmit clock slave mode and transmit clock master mode in '3.18.1 T1/J1 MODE'. (Page 80)

Item 19: Changed the paragragh about non-multiplexed mode in '3.17.2 E1 MODE' & '3.18.2 E1 MODE'. (Pages 77, 86)

Item 18: Changed the paragragh about receive clock slave mode and receive clock master mode in '3.17.1 T1/J1 MODE'. (Page 71)

Item 17: Re-wrote PMON counters description in '3.9.1 T1/J1 MODE' & '3.9.2 E1 MODE'. (Page 53, 56)

Item 16: Added bit 'REFH_LOS' row to Table 5. (Page 27)

Item 15: Changed the pin description of REFA_OUT and REFB_OUT. (Page 17)

April 27, 2004

Item 14: The value of Tprop is changed. (Page 357)

March 22, 2004

Item 13: The description of the DDSINV bit (b3, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit DDS pattern and this bit is cleared when the inversion is completed. (Page 70, 167)

Item 12: The description of the CRCINV bit (b2, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC pattern and this bit is cleared when the inversion is completed. (Page 70, 167)

Item 11: The description of the FsINV bit (b1, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one Fs bit in SF and T1 DM formats, invert one Frame Alignment bit in ESF format or invert one Synchronization Fs bit in SLC-96 format and this bit is cleared when the inversion is completed. (Page 167)

Item 10: The description of the FtINV bit (b0, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one Ft bit in SF, T1 DM and SLC-96 formats and this bit is cleared when the inversion is completed. (Page 167)

Item 9: The description of the CRCINV bit (b5, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert all 4 calculated CRC bits in one Sub-Multi-Frame and this bit is cleared when the inversion is completed. (Page 72, 292)

Item 8: The description of the CRCPINV bit (b4, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 72, 292)

Item 7: The description of the CASPINV bit (b3, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 4-bit Signaling Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 72, 292)

Item 6: The description of the NFASINV bit (b2, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one NFAS bit and this bit is cleared when the inversion is completed. (Page 72, 292)

Item 5: The description of the FASALLINV bit (b1, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 7-bit FAS pattern and this bit is cleared when the inversion is completed. (Page 72, 292)

Item 4: The description of the FAS1INV bit (b0, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one FAS bit and this bit is cleared when the inversion is completed. (Page 292)

Item 3: The output of the REFA_OUT pin and the REFB_OUT pin is changed in case of LOS. The output will be MCLK or high level, as selected by the REFH_LOS bit (b0, T1/J1-03EH,... / b0, E1-03EH,...). (Page 7)

Item 2: Reference Clock Output Control register is added to address 03EH, 13EH, 23EH, 33EH for T1/J1 and E1 modes. (Page 101, 107, 140, 256)

Item 1: The description of the RO1[1:0] bits (b1~0, T1/J1-007H / b1~0, E1-007H) and the RO2[1:0] bits (b4~3, T1/J1-007H / b4~3, E1-007H) is changed. (Page 117, 232)

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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