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Power-grid analysis on SOC-graphics-chip design

YOU CAN SUCCESSFULLY RUN POWER-GRID ANALYSIS ON A 65-nm MIXED-SIGNAL SOC DESIGN.

Accurate power-grid analysis of 65-nm and smaller chips is becoming increasingly important to ensure reliable operation of devices in the field. Re-spins due to on-chip power-distribution issues are expensive and time-consuming and can lead to lost business opportunities. However, power-grid analysis of complex deep-submicron SOCs (systems on chips) with digital, analog, and third-party IP (intellectual-property) blocks can be a difficult task. The task becomes even more daunting when you couple it with looking at variations over multiple corners, as well as between static and dynamic analyses. This article explores a power-grid-analysis flow on a high-performance, 65-nm SOC-graphics-chip design and compares the results of different analysis types and corners.

The design is a 65-nm SOC with multiple IP blocks and memories from different vendors and a main clock frequency of 200 MHz. It has more than 4 million instances and multiple clock domains. Ensuring the reliability of the power-distribution network in this design is critical due to the mass-market nature of the product. This analysis addresses several challenges, including meeting an aggressive tape-out deadline, validating technology information, preparing data, handling analog and mixed-signal IP, resolving import and export issues among tools, examining IR (current/resistance) drop, performing EM (electromigration) analysis using static and dynamic methods, and identifying and repairing any issues the analysis uncovers. This analysis uses a typical flow (**Figure 1**).

INPUT-DATA PREPARATION

In the first step, you characterize power for standard cells and macros. This step generates power-characterized libraries by extracting the netlist and parasitic data from the cell's or macro's physical layout. You can do this characterization at different levels of detail, which, in turn, affect runtime and accuracy. You can obtain the power views for your IP in several ways. If your foundry officially supports your IP and power-analysis tool, there is a good chance that the IP creator has generated power views for your tool. If not, the vendor may be able to generate them for you. However, this process can take some time.

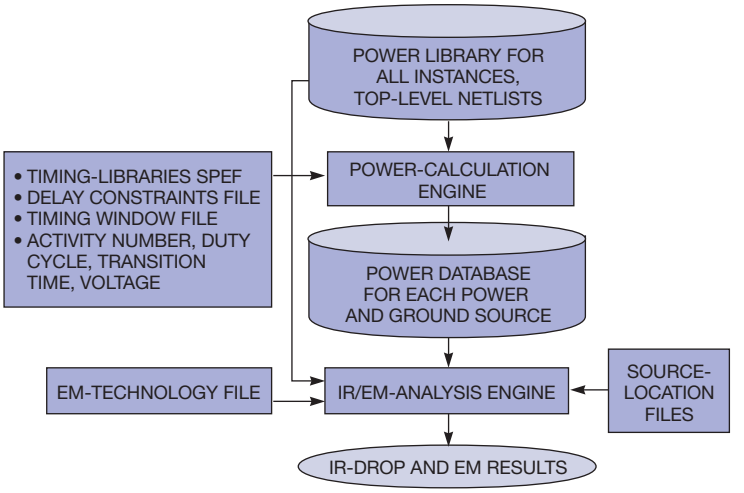

Figure 1 This design uses a typical power-analysis flow.

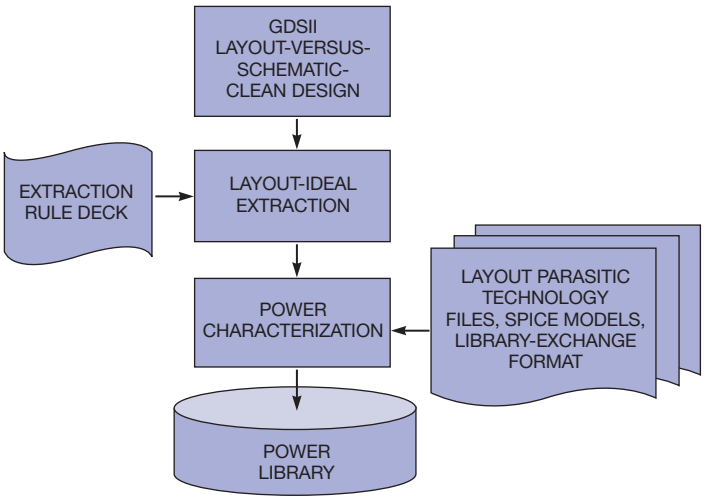

Figure 2 Generating custom power views can be nontrivial.

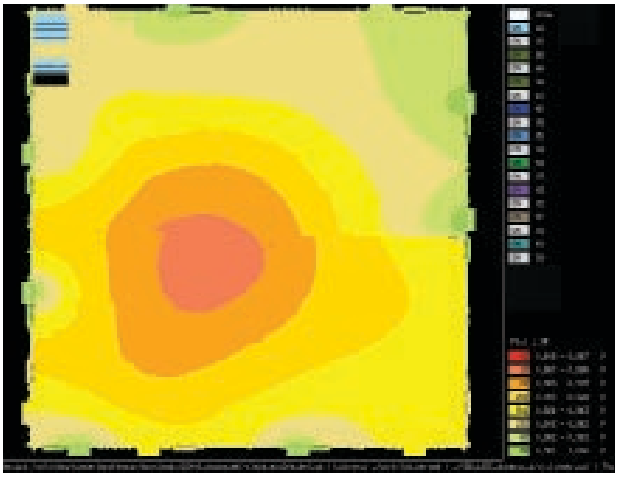

Figure 3 A display of the dynamic drain-to-drain-voltage analysis suggests an IR-drop issue.

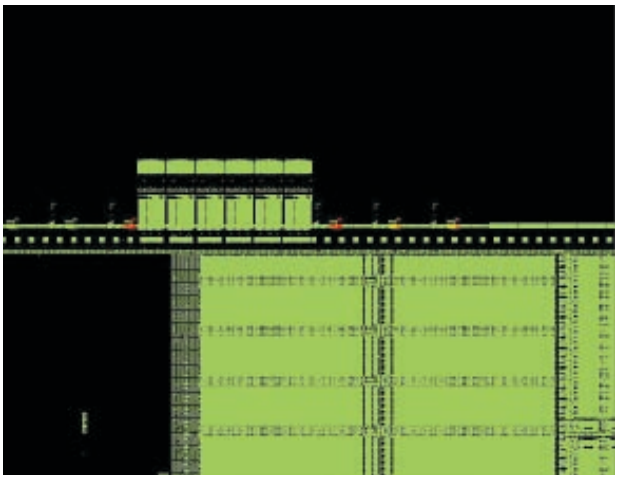

Figure 4 Zooming in on the data from Figure 3 pinpoints the problem.

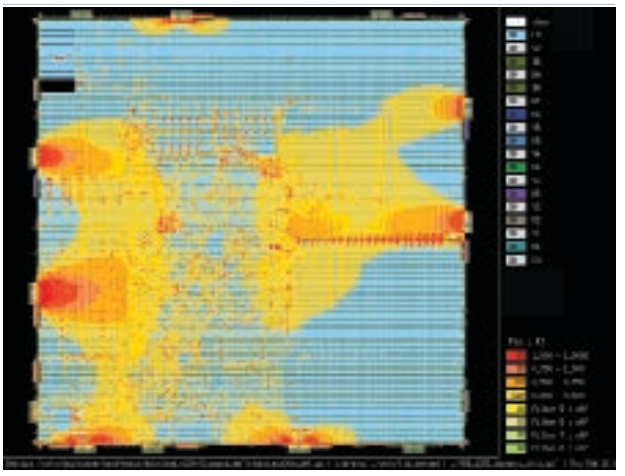

Figure 5 A current-density plot suggests the existence of some "hot" spots.

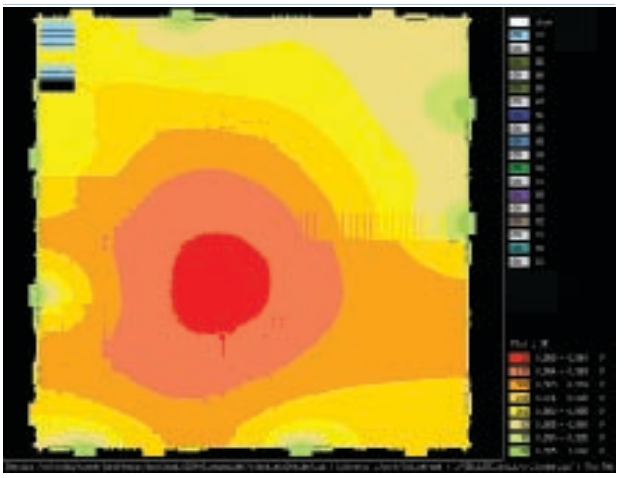

Figure 6 The static-IR-drop analysis does not suggest that problems occurred.

TABLE 1 POWER-CONSUMPTION VARIATION OVER DIFFERENT CORNERS (NORMALIZED TO 1W)

Corner	Internal power	External switching power	Leakage power	Total power
Fast	0.630	0.334	0.036	1
Typical	0.593	0.334	0.038	0.965
Slow	0.556	0.334	0.052	0.943

TABLE 2 IR AND EM RESULTS AT DIFFERENT ACTIVITY FACTORS

	V_{DD} IR drop (V)	V_{DD} EM	V_{SS} IR drop (mV)	V_{SS} EM
8%	0.984	20.448	14.496	25.267
10%	0.983	21.768	15.431	26.898
15%	0.981	25.08	17.767	30.984
20%	0.978	28.407	20.102	35.098

For the cases in which power views don't exist, including internally generated IP blocks, you must go through the custom power-analysis flow and generate the compatible views in that way (**Figure 2**). This task can be fairly complicated because you need to extract the layout, ensure that the LVS (layout versus schematic) is clean, and then run the power-characterization tool to analyze the block. Generating the correct technology files can be a difficult and time-consuming process, but you should again check with your vendors to see whether they have published the files. In this case, the foundry and the tool vendor generated all the technology files for the 65-nm process.

A number of other elements go into the power analysis, including the timing library, activity factors, power-source locations, physical netlist, extraction netlist, timing-window-constraint file, and SDC (standard-delay-constraint) file, all of which you must find or create. The timing library usually contains a power-look-up table that lists the gate's internal power. The power table is a function of input transition time and output net capacitance. The power-analysis tool uses

these entries to calculate overall power consumption within the cells. The activity factor—usually defined globally at the block level—represents how often nodes toggle in the design. It is also possible to have the activity factor propagate through the design logic and to set the factor explicitly on flip-flops to achieve a more realistic result. The most accurate method is to use a gate-level VCD (value-change-dump) file to determine exactly how the nodes toggle, but the onus is then on the user to find a VCD that represents the worst case for IR drop. Also, VCD-based analysis typically takes more runtime.

The power-source-location file specifies the exact X and Y locations for each power and ground source on the chip. This information enables the designer to justify whether the chosen positions will generate a balanced power distribution. At the chip level, these locations are usually on the power and ground pads.

The physical DEF (netlist-definition) file contains cell-placement, routing, and connectivity information for the SOC design. Although DEF is supposed to be a standard format, multiple issues can arise from some place-and-route tools during the generation of a complete DEF. Ultimately, you may have to write scripts to generate a complete DEF from multiple incomplete DEFs and use the new file to drive the power-analysis tools.

The extraction-netlist SPEF (standard-parasitic-exchange-format) file and the TWF (timing-window file) come from the normal process of design analysis. The wire parasitic data for resistance and capacitance are in the SPEF file, which the extraction tools generate. An STA (static-timing-analysis) tool generates the TWF. It contains information about switching windows and transition times, both of which have a large impact on dynamic power.

The SDC file contains clock-domain information, clock periods, and timing constraints. If the SDC file does not specify the default clock frequency, you can explicitly define it in the power-analysis tool's command file.

INSTANCE-BASED POWER CALCULATION

With all of the input files ready, you can begin the analysis, starting with instance-based power calculation. For each instance in the design, the power-analysis engine computes the power for each cell and reports it as an internal, an external, or a leakage type. Internal power is the power in the charging and discharging activities of a cell's internal capacitance, as well as the crowbar current. It is a function of load capacitance within the cell, voltage, frequency, and activity factors. In contrast, external switching power is essentially the power that is necessary for charging the wire capacitances that connect to the cell, which the input SPEF file determines. This power figure includes factors such as load capacitance, voltage, frequency, and activity factors. Leakage power is simply the static leakage power, independent of any cell activity.

Table 1 shows the design's power-calculation results at different corners. This analysis assumes propagated activity factors with maximum power normalized to 1W. As you would expect, you can see that a fast corner consumes the most power. Now, compare the results you obtain by using different values of parameters in the analysis command files.

TABLE 3 DYNAMIC AND STATIC ANALYSIS RESULTS OF USING GLOBAL AND PRIMARY INPUT ACTIVITIES

	Dynamic V_{DD} IR drop (V)	Dynamic V_{SS} IR drop (mV)	Static V_{DD} EM	Static V_{SS} EM	Total chip power (normalized)
Global activity (15%)	0.951	37.926	25.08	30.984	1W
Primary input activity	0.977	19.305	12.545	15.715	503 mW

Varying the global activity factor yields the results in **Table 2**. You can see when the global activity increased and that the IR drop and EM results are worse for drain-to-drain and source-to-source voltages. This expected change is not linear. After comparing the results at different global activities, you can also see what the difference would be between specifying global and propagated input activity factors. Setting the global activity factor to 15% and applying different activity factors for each pin yields the results in **Table 3**. Propagated activity factors show considerably reduced power consumption, IR drop, and EM violations.

Running static and vectorless dynamic analyses and using the most pessimistic results from each type to highlight issues in the design yields the results in **figures 3** through **6**. The worst IR drops occur while using dynamic analysis, and the worst EM violations occur in static analysis. Using fairly pessimistic operating conditions, including high-temperature and high-activity factors, accentuates errors. **Figures 3** through **6** highlight the dynamic drain-to-drain-voltage analysis and some weaknesses in the power grid at the top left of the die. These issues are not obvious in the static analysis. The resistor-current plot in **Figure 5** illustrates the current-density distribution in the design; the red areas are "hotter." After seeing these results, the physical-design team modifies the layout. After reanalysis, the design is ready for verification. Note that a similar analysis of source-to-source voltage is also necessary.

You can successfully run power-grid analysis on a 65-nm mixed analog and digital SOC design using industry tools and assistance from your foundry and the tool vendor. It is worthwhile to run static and vectorless dynamic analyses to find issues that one type of analysis may not highlight, particularly if you can obtain the input activity data from verification. EDN

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