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H8/300H Tiny Series

WKP Interrupt

Introduction

By turning on a switch input connected to the $\overline{\text{WKP}}$ pin, a WKP interrupt is generated, and counting-up of a 16-bit counter which is set in a two-byte variable (counter_sub) starts.

Target Device

H8/3664

Contents

1. Specifications

1. By turning on a switch input connected to the $\overline{\text{WKP}}$ pin, a WKP interrupt is generated, and counting-up of a 16-bit counter which is set in a two-byte variable (counter_sub) starts.
2. The WKP interrupt is requested by detection of the falling edge of the input to the $\overline{\text{WKP}}$ pin.
3. During WKP interrupt handling, counting-up of the 16-bit counter value set in counter_sub starts.
4. Each time the 16-bit counter set in counter_sub overflows, an LED is lit or extinguished.
5. The LED is assumed to be connected to the P74 output pin of port 7.
6. Figure 1.1 shows an example of connection of a switch to the $\overline{\text{WKP}}$ input pin.

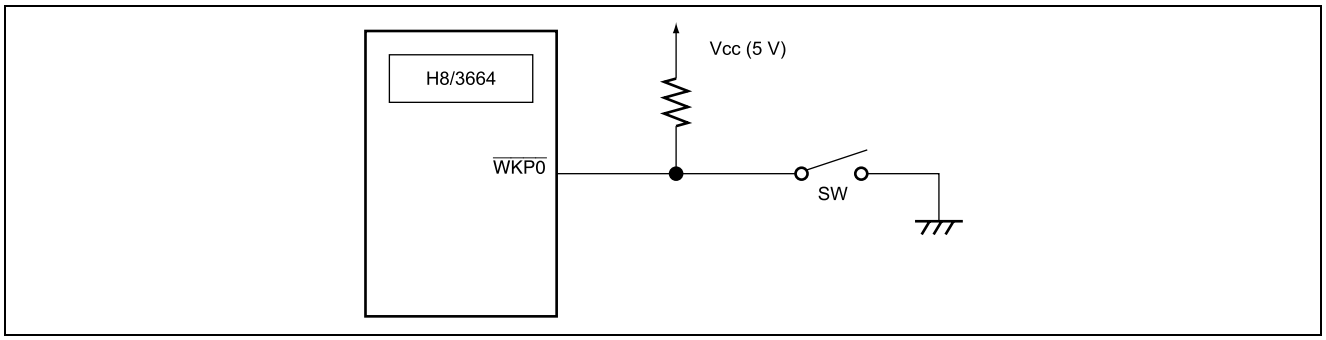


Figure 1.1 LED lighting/extinction operation

2. Description of Functions

1. In this task example, the counter is started by a WKP interrupt.
   Below, the WKP interrupt is explained.
   - The WKP interrupt is requested by an input signal to pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$. Rising or falling edge sensing for the WKP interrupt can be specified using the interrupt edge select register 2 (IEGR2) bits WPEG5 to WPEG0.
   - Pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ are also used for port 5. When using these pins as $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ input pins, the WKP5 to WKP0 bits of the port mode register 5 (PMR5) are set to 1.
   - When, with the pin functions for pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$ selected using the port mode register 5 (PMR5), the specified edge is input, the corresponding bits IWPF5 to IWPF0 of the wakeup interrupt flag register (IWPR) are set to "1", and an interrupt request is generated.
   - Acceptance of an interrupt request can be prohibited by clearing IENWP in the interrupt enable register 1 (IENR1) to "0".
   - By setting the I bit of the condition code register (CCR) to 1, all interrupts can be prohibited.
   - Interrupt operation is described below.
     a. With the corresponding bits of the interrupt enable register set to 1, when an interrupt request occurs, an interrupt request signal is sent to the interrupt controller.
     b. When the interrupt request signal is sent to the interrupt controller, the interrupt request flag is set.
     c. Among interrupts for which the interrupt request flag is set to 1, the highest-priority interrupt request is selected according to the order of priority, and the others are held.
     d. The CCR I bit is referenced, and if the I bit is cleared to 0 then interrupt requests are accepted, but if the I bit is set to 1 then interrupt requests are held.
     e. When an interrupt is accepted, after the instruction being executed at that time ends, the program counter (PC) and CCR are saved to the stack area. The PC saved on the stack indicates the start address for execution on return.
     f. The CCR I bit is set to 1. As a result, all interrupts are masked.
     g. A vector address is generated for the accepted interrupt, and execution of the interrupt processing routine is begun from the address indicated by the contents of the vector address. When interrupts are disabled by clearing the interrupt enable register 1, or when the interrupt flag register 1 is cleared, interrupts should always be masked (I=1). If such operations are performed while I=0, if there is contention between execution of the operation instruction and the occurrence of the interrupt, exception handling for the interrupt which has occurred is executed at the end of execution of the operation instruction.

2. Table 2.1 indicates function allocations in this task example.
   The function allocations are indicated in Table 1, and operations to light and extinguish the LED connected to the I/O port are performed.

Table 2.1 Function Allocation

Function	Function allocation
WPEG0	Sets detection edge direction for $\overline{\text{WKP}}$ pin input
PCR7	Sets P74 output pin function
PDR7	Stores data of P74 output pin
P74	Output pin for LED output

3. Description of Operations

Figure 3.1 explains the operation. Through the hardware and software processing shown in the figure, after a WKP interrupt is generated, the LED connected to the I/O port is lit and extinguished.

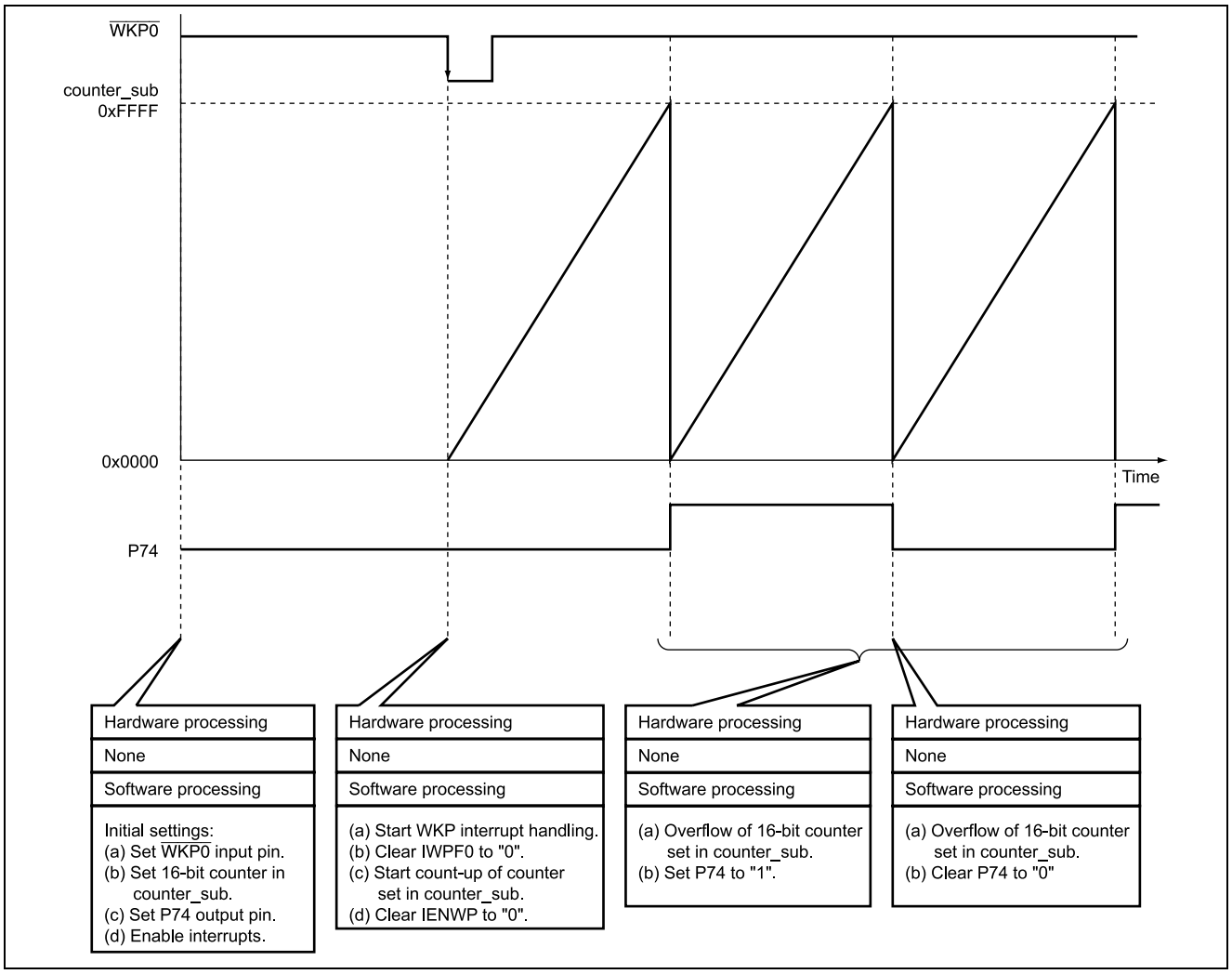


Figure 3.1 Explanation of operation to light and extinguish LED connected to the I/O port

4. Description of software

4.1 Description of Modules

Table 4.1 explains the modules in this task example.

Table 4.1 Description of Modules

Module name	Label name	Function
Main routine	main	Sets direction of input edge for WKP interrupt, sets LED output pin, increments 16-bit counter, and performs LED output
Switch on	WKP	In the WKP interrupt routine, sets SWO NF to 1

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

Register	Name	Function	Address	Setting
PDR7	P74	Port data register 7 (port data register 74) P74 = 0: The pin P74 output level is low P74 = 1: The pin P74 output level is high	H'FFDA Bit 4	0
PCR7	PCR74	Port control register 7 (port control register 74) PCR74 = 1: The I/O pin P74 functions as an output pin	H'FFEA Bit 4	1
IEGR2	WPEG0	Interrupt edge select register 2 (WKP0 edge select) WPEG0 = 0: Detects the falling edge of the $\overline{\text{WKP0}}$ pin input	H'FFF3 Bit 0	0
IENR1	IENWP	Interrupt enable register 1 (WKP0 interrupt enable) IENWP = 1: Enables $\overline{\text{WKP0}}$ pin input interrupt requests	H'FFF4 Bit 5	1
IWPR	IWPF0	Interrupt flag register (WKP0 interrupt request flag) IWPF0 = 0: A WKP0 interrupt is requested IWPF0 = 1: A WKP0 interrupt is not requested	H'FFF8 Bit 0	0
PMR5	WKP0	Selects general I/O port/WKP0 pin function WKP0 = 0: Selects general I/O output port WKP0 = 1: selects $\overline{\text{WKP0}}$ input pin	H'FFE1 Bit 0	1

4.4 Description of RAM Used

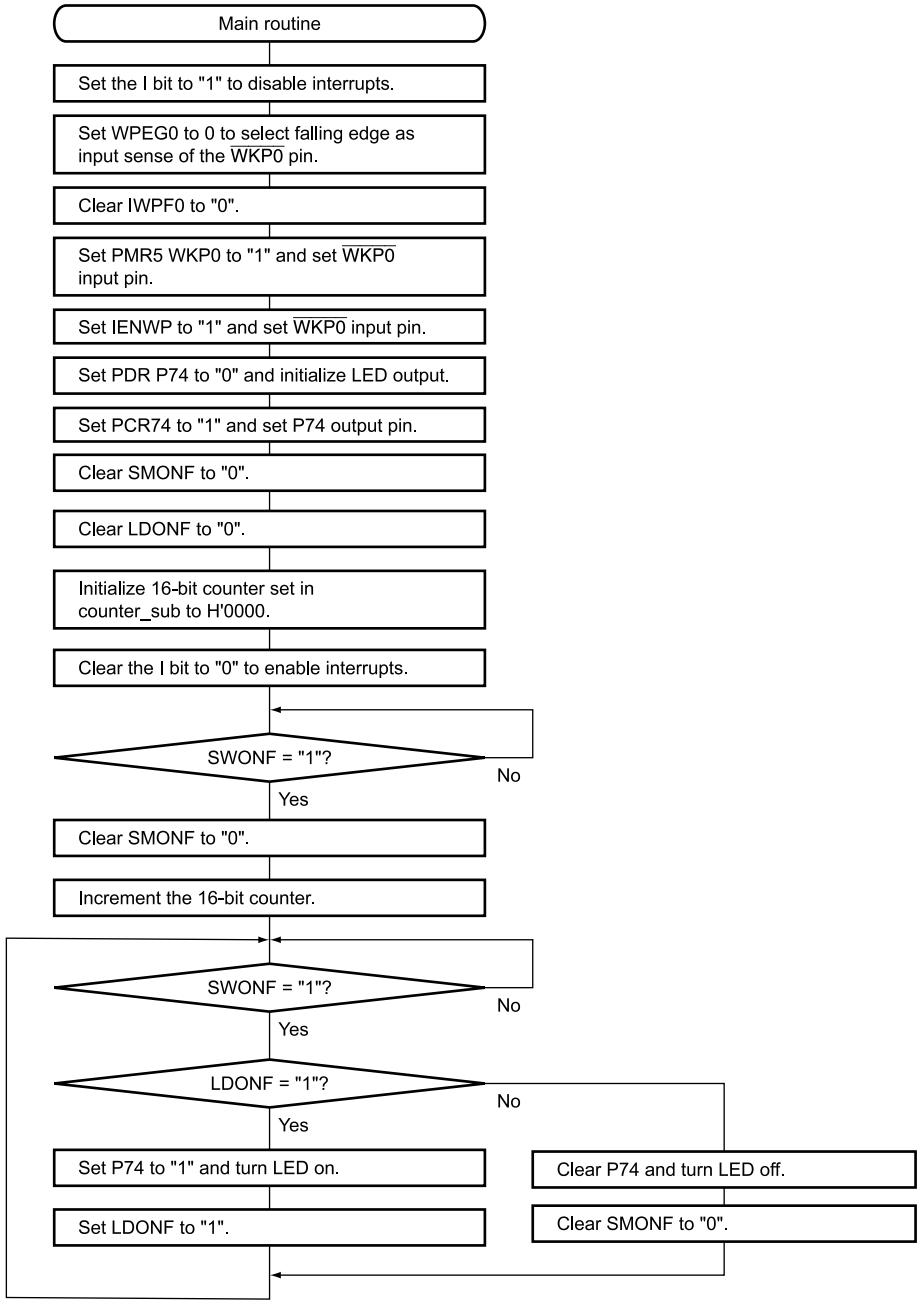
Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name		Function	Address	Used in
Counter_sub		16-bit up-counter which lights and extinguishes the LED each time overflow occurs	H'FB80	Main routine
USRF	SWONF	Flag to judge whether switch input is on or off	H'FB82 Bit 0	Main routine Switch on
	LDONF	Flag to judge whether LED is on or off	H'FB82 Bit 1	Main routine

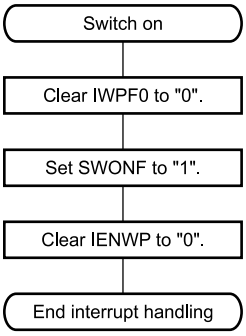
5. Flowcharts

1. Main routine



Note: * In this example, the stack pointer is set using INIT.SRC (assembly language).

2. WKP0 interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT   _INIT
      .IMPORT   _main
 ;
      .SECTION  P,CODE
 _INIT:
      MOV.W     #H'FF80,R7
      LDC.B     #B'10000000,CCR
      JMP       @_main
 ;
      .END
```

```
/************************************************************************************************************************************************/
/*                                                                                                                                              */
/*   H8/300H Tiny Series -H8/3664-                                                                                                              */
/*   Application Note                                                                                                                           */
/*                                                                                                                                              */
/*   'Wake Up Interrupt function                                                                                                                */
/*                                                                                                                                              */
/      Function                                                                                                                                  */
/*   : Wake Up                                                                                                                                  */
/*                                                                                                                                              */
/*   External Clock : 16MHz                                                                                                                     */
/*   Internal Clock : 16MHz                                                                                                                     */
/*   Sub Clock      : 32.768kHz                                                                                                                 */
/*                                                                                                                                              */
/************************************************************************************************************************************************/

#include    <C:\ch38\include\machine.h>

/************************************************************************************************************************************************/
/*   Symbol Defnition                                                                                                                           */
/************************************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;    /* bit7 */
     unsigned char   b6:1;    /* bit6 */
     unsigned char   b5:1;    /* bit5 */
     unsigned char   b4:1;    /* bit4 */
     unsigned char   b3:1;    /* bit3 */
     unsigned char   b2:1;    /* bit2 */
     unsigned char   b1:1;    /* bit1 */
     unsigned char   b0:1;    /* bit0 */
};

#define   IEGR2          *(volatile unsigned char *)0xFFF3                    /* Interrupt Select Edge Register 2         */
#define   IEGR2_BIT           (*(struct BIT *)0xFFF3)                         /* Interrupt Select Edge Register 2         */
#define   WPEG0               IEGR2_BIT.b0                                    /* Wake Up 0 Edge Select                    */
#define   INER1               *(volatile unsigned char *)0xFFF4               /* Interrupt Enable Register 1              */
#define   INER1_BIT      (*(struct BIT *)0xFFF4)                              /* Interrupt Enable Register 1              */
#define   IENWP               INER1_BIT.b5                                    /* Wake Up Interrupt Enbable                */
#define   IWPR           *(volatile unsigned char *)0xFFF8                    /* Interrupt Flag Register                  */
#define   IWPR_BIT       (*(struct BIT *)0xFFF8)                              /* Interrupt Flag Register                  */
#define   IWPF0               IWPR_BIT.b0                                     /* Wake Up0 Interuput Request Flag          */
#define   PMR5           *(volatile unsigned char *)0xFFE1                    /* Port Mode Register 5                     */
#define   PMR5_BIT       (*(struct BIT *)0xFFE1)                              /* Port Mode Register 5                     */
#define   WKP0           PMR5_BIT.b0                                          /* WKP0 Function Select Bit                 */
```

```
#define   PCR7          *(volatile unsigned char *)0xFFEA                    /* Port Control Register 7                */
#define   PCR7_BIT      (*(struct BIT *)0xFFEA)                              /* Port Control Register 7                */
#define   PCR74              PCR7_BIT.b4                                     /* Port Control Register Bit 4            */
#define   PDR7          *(volatile unsigned char *)0xFFDA                    /* Port Data Register 7                   */
#define   PDR7_BIT      (*(struct BIT *)0xFFDA)                              /* Port Data Register 7                   */
#define   P74           PDR7_BIT.b4                                          /* Port Data Register Bit 4               */

#pragma       interrupt    (WKP_0)
/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
unsigned int        counter_sub;                                            /* 16 Bit Up Counter                      */
unsigned char       USRF;                                                   /* User Flag Erea                         */
#define             USRF_BIT    (*(struct BIT *)&USRF)
#define             SWONF         USRF_BIT.b0                               /* Swich ON/OFF Judgment Flag             */
#define             LDONF         USRF_BIT.b1                               /* LED ON/OFF Judgment Flag               */

extern void _INITSCT();
/************************************************************************************************************************/
/*   Function definition                                                                                                */
/************************************************************************************************************************/
extern  void   INIT( void );                                                /* SP Set                                 */
extern  void   WKP_0( void );                                               /* Wake Up 0 Interrupt Routine            */
void    main   ( void );
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                      /* VECTOR SECTOIN SET                     */
void (*const VEC_TBL1[])(void) = {                                          /* 0x00 - 0x0f                            */
     INIT                                                                   /* 00 Reset                               */
};

#pragma section     V2                                                      /* VECTOR SECTOIN SET                     */
void (*const VEC_TBL2[])(void) = {                                          /* 0x24 - 0x25                            */
     WKP_0                                                                  /* 18 WKP0                                */
};

#pragma section                                                             /* P                                      */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     _INITSCT();

     set_imask_ccr(1);                                                      /* Interrupt Disable                      */

     WPEG0 = 0;                                                             /* WKP0 Falling Edge Interrupt Select     */

     WKP0 = 1;                                                              /* WKP0 Input Pin Select                  */

     IENWP = 1;                                                             /* WKP0 Interrupt Enable                  */

     P74 = 0;                                                               /* Port74 "0" Output                      */

     PCR7 = 0x10;                                                           /* Port74 Output                          */
     SWONF = 0;                                                             /* Swich ON/OFF Judgment Flag Clear       */

     LDONF = 0;                                                             /* LED ON/OFF Judgment Flag Clear         */
```

```
    counter_sub = 0x0000;                                   /* 16 Bit Counter Clear                 */

    set_imask_ccr(0);                                       /* Interrupt Enable                     */

    while(SWONF != 1){                                      /* SWONF = 1 ?                          */
        ;
    }

    SWONF = 0;                                              /* Clear SWONF                          */

    while(1){
        do{
            counter_sub++;                                  /* Increment 16bit Counter              */
        }while(counter_sub != 0x0000);                      /* 16bit Counter = H'0000 ?             */

        if(LDONF == 1){                                     /* LDONF = 1 ?                          */
            P74 = 0;                                        /* Turn Off LED                         */
            LDONF = 0;                                      /* Clear LDONF                          */
        }
            else{
                P74 = 1;                                    /* Turn On LED                          */
                LDONF = 1;                                  /* Set LDONF                            */
            }
        }
}

/*****************************************************************************************************************************************/
/*   Wake Up Interrupt                                                                                                                   */
/*****************************************************************************************************************************************/
void WKP_0( void )
{
    IWPF0 = 0;                                              /* Clear IWPF0 to 0                     */

    SWONF = 1;                                              /* Set SWONF to 1                       */

    IENWP = 0;                                              /* Clear IENWP to 0                     */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0016
P	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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