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Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Sample Programs for Standby Function

V850E/IF3: μ PD70F3451 μ PD70F3452 V850E/IG3: μ PD70F3453 μ PD70F3454

Document No. U18735EJ1V0AN00 (1st edition) Date Published September 2007 N

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[MEMO]

NOTES FOR CMOS DEVICES —

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M5 02.11-1

INTRODUCTION

- Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.
 - 2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).
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 - 4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

Startup routine: ig3_start.sLink directive file: ig3_link.dir

Target Readers This Application Note is intended for users who understand the functions of the

V850E/IF3 (μ PD70F3451, 70F3452), and V850E/IG3 (μ PD70F3453, 70F3454), and

who design application systems that use these microcontrollers.

Purpose This manual is intended to give users an understanding of the basic functions of the

V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual It is assumed that the reader of this Application Note has general knowledge in the

fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the V850E/IF3, V850E/IG3 Hardware User's Manual.

For details of instruction functions

→ See the V850E1 Architecture User's Manual.

Conventions Data significance: Higher digits on the left and lower digits on the right

Active low representation: \overline{xxx} (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on

the bottom

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information Numeric representation: Binary ... xxxx or xxxxB

Decimal ... xxxx

Hexadecimal ... xxxxH

Prefix indicating the power

of 2 (address space,

memory capacity): K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

The function lists are structured as follows.

Theme

[Function] Function description [Function name] Name of sample function [Argument(s)] Type and overview of argument(s) [Processing content] Processing content of sample function [Starting method] Conditions for calling a function [SFR(s) used] Register name and setting content [call function(s)] Name and function of call function(s) Type, name, and overview of variable(s) used in sample function [Variable(s)] [Interrupt(s)] Name of function Name [Interrupt source(s)] [File name] Name of corresponding sample program file Caution(s) upon function usage [Caution(s)]

Interrupt function

 [Function name]
 Name of interrupt function

 [Servicing content]
 Servicing content of interrupt function

 [SFR(s) used]
 Name of interrupt and conditions for occurrence

 [call function(s)]
 None

 [Variable(s)]
 Name of variable, function

 [File name]
 Name of corresponding sample program file

 [Caution(s)]
 None

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I ² C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

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CHAPTER 1 HALT MODE

[Function] Sets standby function (HALT mode).

[Function name] halt_main

[Argument] None

[Processing content] Shifts from normal operation mode to HALT mode. The HALT mode is released by an

external interrupt request signal.

[Starting method] None

[SFR used] None

[call functions] halt_init, halt_mode

[Variable] None

[Interrupt] external_int

[Interrupt source] INTP07

[File name] halt.c

[Caution] Interrupts not to be used must be masked before setting to HALT mode.

[Function name] halt_init

[Processing content] Sets an external interrupt request signal (INTP07) for releasing HALT mode.

[SFRs used] PFC0: 0x00 (Sets INTP07 to input.)

PMC0: 0x80 (Sets INTP07 to input.)

INTR0: 0x80 (Sets valid edge to rising edge.)
INTF0: 0x00 (Sets valid edge to rising edge.)
PIC07.PIF07: 0 (Clears INTP07 interrupt request flag.)
IMR5: 0xFFFF (Specifies interrupt mask.)
IMR4: 0xFFFF (Specifies interrupt mask.)
IMR3: 0xFFFF (Specifies interrupt mask.)

IMR2: 0xFFFF (Specifies interrupt mask.)

IMR1: 0xFFFF (Specifies interrupt mask.)

IMR0: 0xFFFF (Specifies interrupt mask.)

PICOZ RMKOZ: 0 (Epobles INTROZ interrupt contining.)

PIC07.PMK07: 0 (Enables INTP07 interrupt servicing.)

[call function]None[Variable]None[File name]halt.c

[Caution]

[Function name] halt_mode

[Processing content] Executes HALT instruction.

None

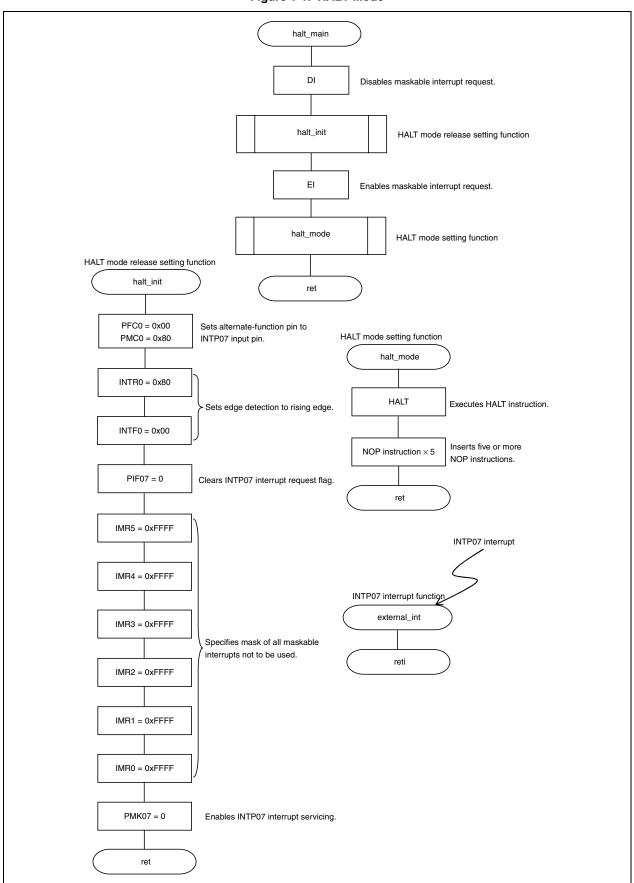
[SFR used] None
[call function] None
[Variable] None
[File name] halt.c

[Caution] Insert five or more NOP instructions after the HALT instruction.

Interrupt function

[Function name]	external_int
[Servicing content]	There is no particular servicing, because this is used for confirmation of external interrupt occurrence.
[SFR used]	None
[call function]	None
[Variable]	None
[File name]	halt.c
[Caution]	None

Figure 1-1. HALT Mode



CHAPTER 2 IDLE MODE

[Function] Sets standby function (IDLE mode).

[Function name] idle_main

[Argument] None

[Processing content] Shifts from normal operation mode to IDLE mode. The IDLE mode is released by an

external interrupt request signal.

[Starting method] None

[SFR used] None

[call functions] idle_init, idle_mode

[Variable] None

[Interrupt] external_int

[Interrupt source] INTP07

[File name] idle.c

[Caution] Interrupts not to be used must be masked before setting to IDLE mode.

[Function name] idle_init

[Processing content] Sets an external interrupt request signal (INTP07) for releasing IDLE mode.

[SFRs used] PFC0: 0x00 (Sets INTP07 to input.)

PMC0: 0x80 (Sets INTP07 to input.)

INTR0: 0x80 (Sets valid edge to rising edge.)
INTF0: 0x00 (Sets valid edge to rising edge.)
PIC07.PIF07: 0 (Clears INTP07 interrupt request flag.)
IMR5: 0xFFFF (Specifies interrupt mask.)

IMR5: 0xFFFF (Specifies interrupt mask.)

IMR4: 0xFFFF (Specifies interrupt mask.)

IMR3: 0xFFFF (Specifies interrupt mask.)

IMR2: 0xFFFF (Specifies interrupt mask.)

IMR1: 0xFFFF (Specifies interrupt mask.)

IMR0: 0xFFFF (Specifies interrupt mask.)

PIC07.PMK07: 0 (Enables INTP07 interrupt servicing.)

[call function]None[Variable]None[File name]idle.c

[Caution]

None

[Function name] idle_mode

[Processing content] Executes IDLE mode by forcibly terminating all DMA transfers.

[SFRs used] DCHC0.TC0 DMA0 transfer status bit

DCHC0.E00: 1 (Enables DMA0 transfer.)

DCHC0.INIT0: 1 (Forcibly terminates DMA0 transfer.)

DCHC1.TC1 DMA1 transfer status bit DCHC1.E11: 1 (Enables DMA1 transfer.)

DCHC1.INIT1: 1 (Forcibly terminates DMA1 transfer.)

DCHC2.TC2 DMA2 transfer status bit DCHC2.E22: 1 (Enables DMA2 transfer.)

DCHC2.INIT2: 1 (Forcibly terminates DMA2 transfer.)

DCHC3.TC3 DMA3 transfer status bit DCHC3.E33: 1 (Enables DMA3 transfer.)

DCHC3.INIT3: 1 (Forcibly terminates DMA3 transfer.)
PRCMD: 0x03 (Writes to command register

(used when writing to a special register).)

PCC: 0x03 (Selects clock as fxx/8.)
PSMR: 0x00 (Sets to IDLE mode.)

PRCMD: 0x02 (Writes to command register

(used when writing to a special register).)

PSC: 0x02 (Enables standby mode release by maskable interrupt request and

sets to standby mode.)

[call function] None

[Variable] None

[File name] idle.c

[Cautions] • DMA transfer is forcibly terminated in this sample program, because all DMA transfers

must be terminated before performing data setting to the special register.

When DMA is not used, the terminate processing of DMA is not needed.

PCC and PSC registers are special registers and can therefore only be written in

combination of specific sequences.

• When setting to IDLE mode, set in the order of, the PCC register (set to 03H), the

PSMR.PSM0 bit, and the PSC.STB bit.

Interrupt function

[Function name]	external_int
[Servicing content]	There is no particular servicing because this is used for confirmation of external interrupt occurrence.
[SFR used]	None
[call function]	None
[Variable]	None
[File name]	idle.c
[Caution]	None

Figure 2-1. IDLE Mode (1/3)

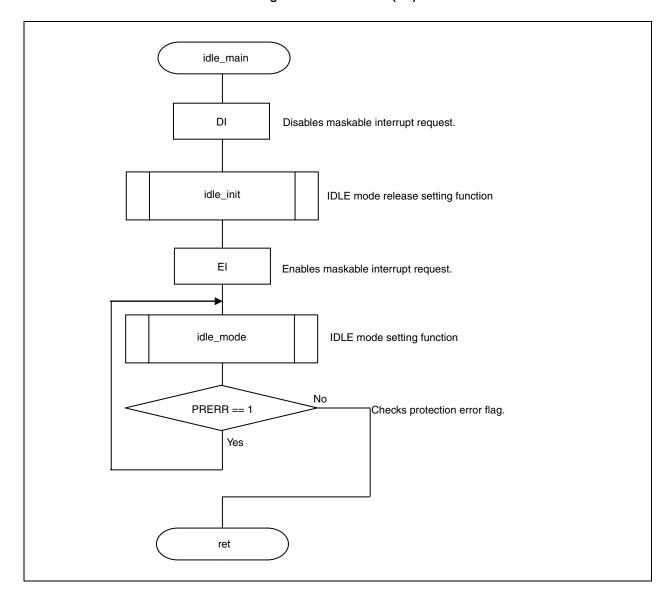
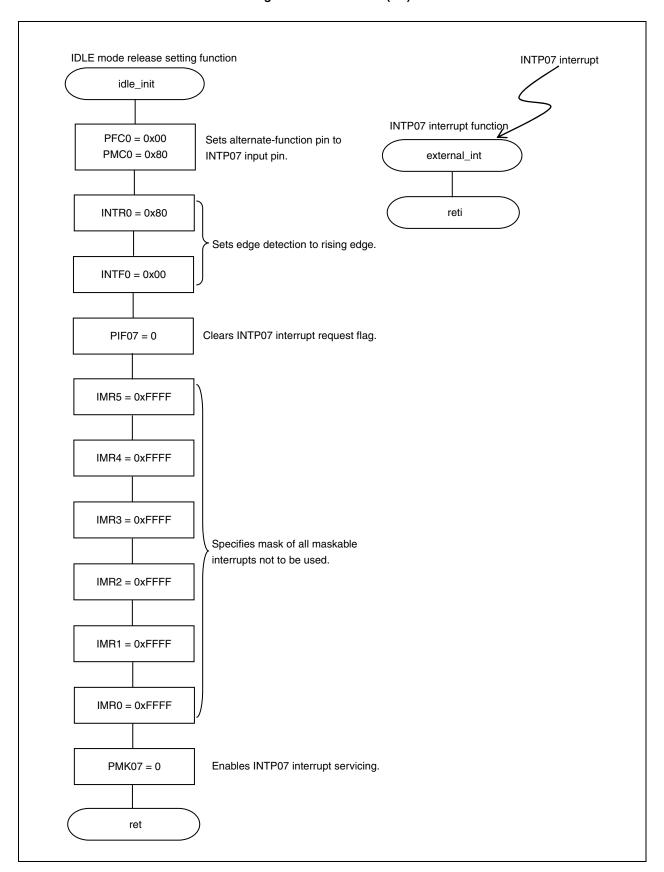


Figure 2-1. IDLE Mode (2/3)



IDLE mode setting function idle_mode PRCMD = 0x03Writes to command register. No TC0 == 0 && E00 == 1 Checks DMA0 transfer. Yes PCC = 0x03Selects clock as fxx/8. Forcibly INIT0 = 1 terminates DMA0. NOP instruction × 5 Inserts five or more NOP instructions. No TC1 == 0 && E11 == 1 Checks DMA1 transfer. Yes PSMR = 0x00Specifies standby mode operation as IDLE mode. INIT1 = 1 Forcibly terminates DMA1. Unnecessary when PRCMD = 0x02Writes to command register. DMA is not used. TC2 == 0 && E22 == 1 Checks DMA2 Enables release of standby control via transfer. PSC = 0x02 maskable interrupt request. Yes Specifies operation mode as standby mode. Forcibly INIT2 = 1terminates DMA2. NOP instruction \times 5 Inserts five or more NOP instructions. No Checks DMA3 TC3 == 0 && E33 == 1 ret transfer. Yes Forcibly terminates INIT3 = 1 DMA3.

Figure 2-1. IDLE Mode (3/3)

CHAPTER 3 STOP MODE

[Function] Sets standby function (STOP mode).

[Function name] stop_main

[Argument] None

[Processing content] Shifts from normal operation mode to STOP mode. The STOP mode is released by an

external interrupt request signal.

[Starting method] None

[SFR used] None

[call functions] stop_init, stop_mode

[Variable] None

[Interrupt] external_int

[Interrupt source] INTP07

[File name] stop.c

[Cautions] • Interrupts not to be used must be masked before setting to STOP mode.

• The INTP07 interrupt request signal is kept set after releasing STOP mode.

CHAPTER 3 STOP MODE

[Function name] stop_init [Processing content] Sets an external interrupt request signal (INTP07) for releasing STOP mode. [SFRs used] OSTS: 0x07 (Sets oscillation stabilization time to 16.4 ms) PFC0: 0x00 (Sets INTP07 to input.) PMC0: 0x80 (Sets INTP07 to input.) 0x80 (Sets valid edge to rising edge.) INTR0: INTF0: 0x00 (Sets valid edge to rising edge.) PIC07.PIF07: 0 (Clears INTP07 interrupt request flag.) IMR5: 0xFFFF (Specifies interrupt mask.) IMR4: 0xFFFF (Specifies interrupt mask.) IMR3: 0xFFFF (Specifies interrupt mask.) IMR2: 0xFFFF (Specifies interrupt mask.) IMR1: 0xFFFF (Specifies interrupt mask.) IMR0: 0xFFFF (Specifies interrupt mask.) PIC07.PMK07: 0 (Enables INTP07 interrupt servicing.)

[call function]None[Variable]None[File name]stop.c[Caution]None

[Function name] stop_mode [Processing content] Executes STOP mode by forcibly terminating all DMA transfers. [SFRs used] DCHC0.TC0 DMA0 transfer status bit DCHC0.E00: 1 (Enables DMA0 transfer.) DCHC0.INIT0: 1 (Forcibly terminates DMA0 transfer.) DCHC1.TC1 DMA1 transfer status bit DCHC1.E11: 1 (Enables DMA1 transfer.) DCHC1.INIT1: 1 (Forcibly terminates DMA1 transfer.) DCHC2.TC2 DMA2 transfer status bit DCHC2.E22: 1 (Enables DMA2 transfer.) DCHC2.INIT2: 1 (Forcibly terminates DMA2 transfer.) DCHC3.TC3 DMA3 transfer status bit DCHC3.E33: 1 (Enables DMA3 transfer.) DCHC3.INIT3: 1 (Forcibly terminates DMA3 transfer.) PRCMD: 0x03 (Writes to command register (used when writing to a special register).) PCC: 0x03 (Selects clock as fxx/8.) PSMR: 0x01 (Sets to STOP mode.) PRCMD: 0x02 (Writes to command register (used when writing to a special register).) PSC: 0x02 (Enables standby mode release by maskable interrupt request and sets to standby mode.) [call function] None [Variable] None [File name] stop.c [Cautions] DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register. When DMA is not used, the terminate processing of DMA is not needed. · PCC and PSC registers are special registers and can therefore only be written in combination of specific sequences. • When setting to STOP mode, set in the order of, the PCC register (set to 03H), the

PSMR.PSM0 bit, and the PSC.STB bit.

Interrupt function

[Function name]	external_int
[Servicing content]	There is no particular servicing because this is used for confirmation of external interrupt occurrence.
[SFR used]	None
[call function]	None
[Variable]	None
[File name]	stop.c
[Caution]	None

Figure 3-1. STOP Mode (1/3)

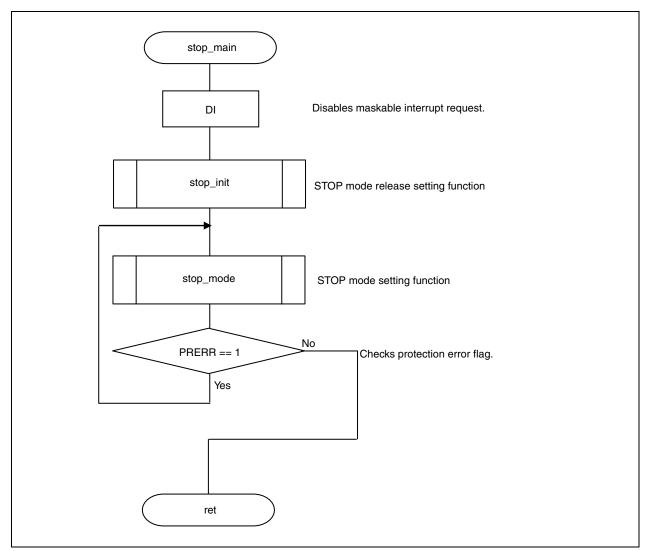
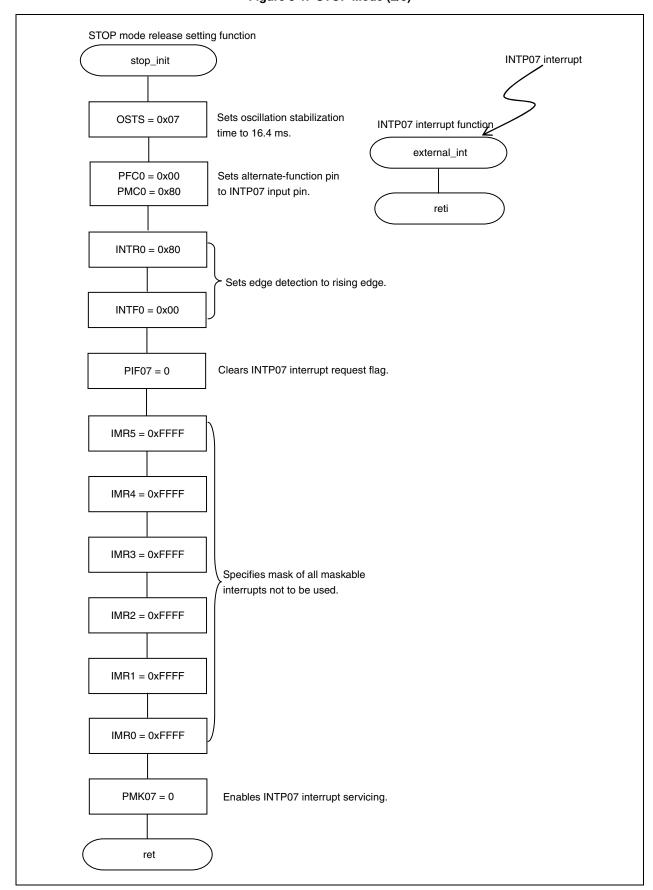


Figure 3-1. STOP Mode (2/3)



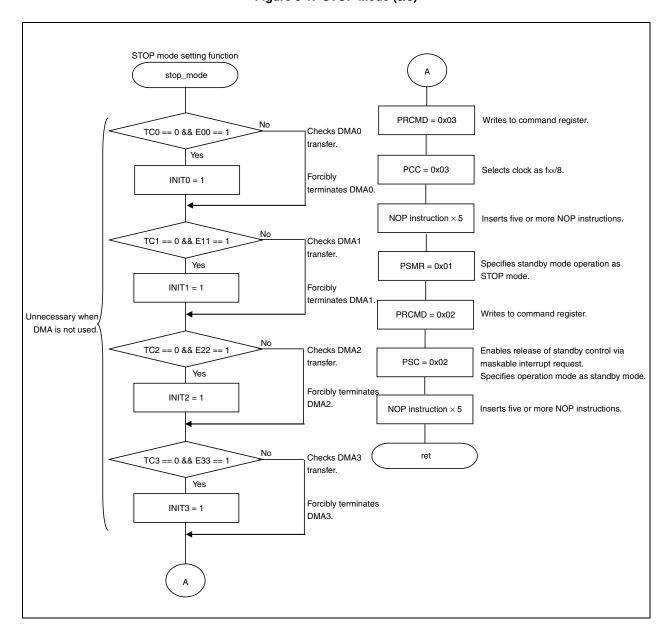


Figure 3-1. STOP Mode (3/3)

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