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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Sample Programs for DMA Function

V850E/IF3:
- μPD70F3451
- μPD70F3452

V850E/IG3:
- μPD70F3453
- μPD70F3454

Document No. U18727EJ1V0AN00 (1st edition)
Date Published August 2007 N

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M5 02. 11-1

INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.

2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).

3. This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

- **Startup routine: ig3_start.s**
- **Link directive file: ig3_link.dir**

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IF3 (μPD70F3451, 70F3452), and V850E/IG3 (μPD70F3453, 70F3454), and who design application systems that use these microcontrollers.

Purpose

This manual is intended to give users an understanding of the basic functions of the V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the **V850E/IF3, V850E/IG3 Hardware User's Manual**.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$

The function lists are structured as follows.

Hardware name (symbol)

[Function]	Function description
[Function name]	Name of sample function
[Argument(s)]	Type and overview of argument(s)
[Processing content]	Processing content of sample function
[Starting method]	Conditions for calling a function
[SFR(s) used]	Register name and setting content
[call function(s)]	Name and function of call function(s)
[Variable(s)]	Type, name, and overview of variable(s) used in sample function
[Interrupt(s)]	Name of function
[Interrupt source(s)]	Name
[File name]	Name of corresponding sample program file
[Caution(s)]	Caution(s) upon function usage

Interrupt function

[Function name]	Name of interrupt function
[Servicing content]	Servicing content of interrupt function
[SFR(s) used]	Name of interrupt and conditions for occurrence
[call function(s)]	None
[Variable(s)]	Name of variable, function
[File name]	Name of corresponding sample program file
[Caution(s)]	None

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I^2C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

CONTENTS

CHAPTER 1 SINGLE TRANSFER MODE

1.1 Software Sources

[Function]	Starts DMA transfer by software trigger.
[Function name]	dma1_main
[Argument]	None
[Processing content]	Performs DMA transfer between on-chip peripheral I/O (A/D2 conversion result register) and on-chip peripheral I/O (UARTA0 transmit data register). Generates a DMA transfer end interrupt (INTDMA0) upon completion of DMA transfer. Sets transfer data size to 8 bits, transfer count to 1, and sets to single transfer mode.
[Starting method]	None
[SFR used]	DMAIC0: 0x07 (Clears DMA0 transfer end interrupt request signal (INTDMA0), releases mask, sets to priority level 7.)
[call functions]	dma_forward, dma_count_add_control, dma_start
[Variable]	None
[Interrupt]	dma_int
[Interrupt source]	INTDMA0
[File name]	dma1.c
[Caution]	None

[Function name]	dma_forward
[Processing content]	Specifies DMA transfer source/destination addresses.
[SFRs used]	DSA0H: 0x0FFF (Sets DMA transfer source to on-chip peripheral I/O and sets DMA transfer source address.) DSA0L: 0xFB90 (Sets DMA transfer source address.) DDA0H: 0x0FFF (Sets DMA transfer destination to on-chip peripheral I/O and sets DMA transfer destination address.) DDA0L: 0xFA07 (Sets DMA transfer destination address.)
[call function]	None
[Variable]	None
[File name]	dma1.c
[Caution]	None

[Function name]	dma_count_add_control
[Processing content]	Specifies DMA transfer counts and DMA transfer mode.
[SFRs used]	DBC0: 0x0000 (Sets one transfer.) DADC0: 0x00A0 (Sets transfer data size to 8 bits, fixes count direction of transfer source/destination addresses, and sets to single transfer mode.)
[call function]	None
[Variable]	None
[File name]	dma1.c
[Caution]	None

[Function name]	dma_start
[Processing content]	Enables and starts DMA transfer.
[SFRs used]	DCHC0: 0x01 (Enables DMA transfer.) DCHC0.STG0: 1 (Starts DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma1.c
[Caution]	None

Interrupt function

[Function name]	dma_int
[Servicing content]	Disables DMA transfer after completion of DMA transfer.
[SFR used]	DCHC0.E00: 0 (Disables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma1.c
[Caution]	None

Figure 1-1. Software Sources (1/2)

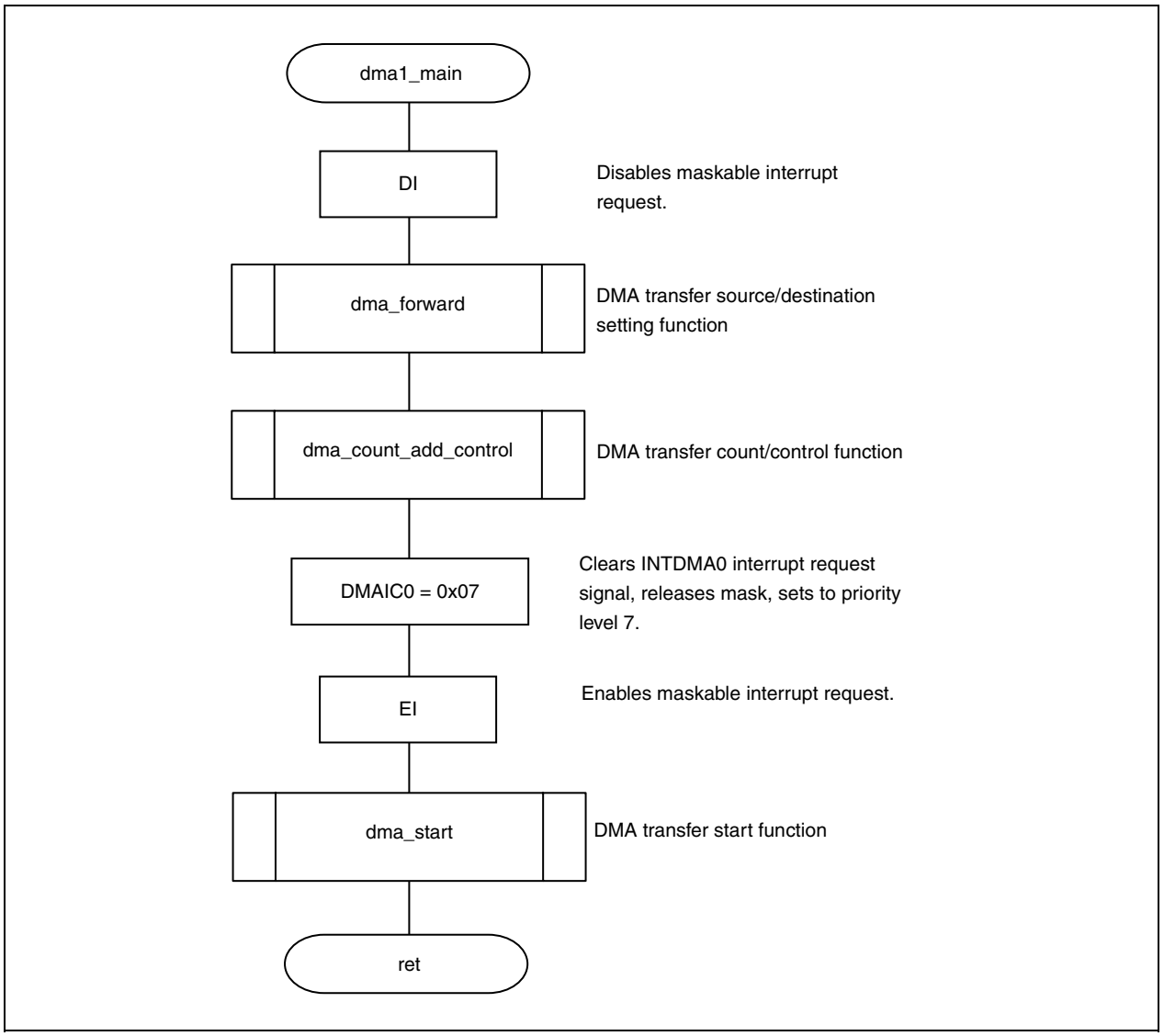
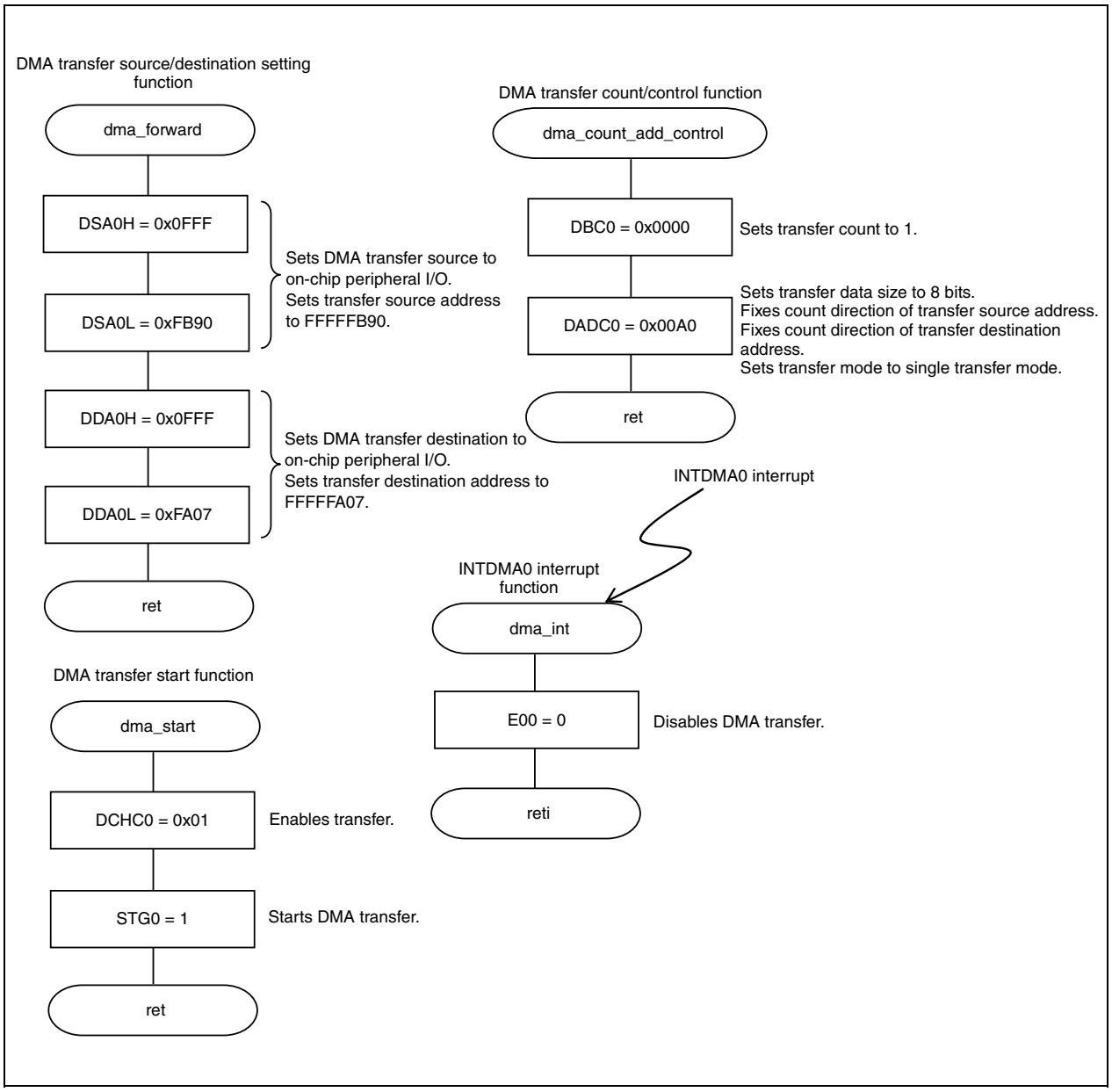


Figure 1-1. Software Sources (2/2)



1.2 Source of Interrupt from On-Chip Peripheral I/O

[Function]	Starts DMA transfer when an interrupt request from on-chip peripheral I/O that is set by the DTFR0 register occurs.
[Function name]	dma2_main
[Argument]	None
[Processing content]	Performs transfer between on-chip peripheral I/O (UARTA0 receive data register) and internal RAM (buf_rx[]). The DMA start factor is a UARTA0 reception end interrupt request signal. Generates INTDMA0 after 10 DMA transfers and completes the DMA transfer.
[Starting method]	None
[SFRs used]	UA0REIC: 0x07 (Clears UARTA0 reception error interrupt request signal (INTUA0RE), releases mask and sets to priority level 7.) UA0RIC: 0x07 (Clears UARTA0 reception end interrupt request signal (INTUA0R), releases mask and sets to priority level 7.) DMAIC0: 0x07 (Clears DMA0 transfer end interrupt request signal (INTDMA0), releases mask, and sets to priority level 7.)
[call functions]	dma_forward, dma_count_add_control, dma_start, uarta_port, uarta_set, uarta_start
[Variables]	unsigned char buf_rx[]: Receive data storing buffer volatile unsigned char count_rx: Reception count variable
[Interrupts]	dma_int, uarta_int_receive, uarta_error
[Interrupt sources]	INTDMA0, INTUA0R, INTUA0RE
[File name]	dma2.c
[Caution]	None

[Function name]	dma_forward
[Processing content]	Specifies DMA transfer source/destination addresses.
[SFRs used]	DSA0H: 0x0FFF (Sets DMA transfer source to on-chip peripheral I/O and sets DMA transfer source address.)
	DSA0L: 0xFA06 (Sets DMA transfer source address.)
	DDA0H: 0x8FFF (Sets DMA transfer destination to internal RAM and sets DMA transfer destination address.)
	DDA0L: 0xE30C (Sets DMA transfer destination address.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	dma_count_add_control
[Processing content]	Specifies DMA transfer counts and DMA transfer mode.
[SFRs used]	DBC0: 0x0009 (Sets 10 transfers.)
	DADC0: 0x0080 (Sets transfer data size to 8 bits, fixes count direction of transfer source addresses, increments count direction of transfer destination address, and sets to single transfer mode.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	dma_start
[Processing content]	Enables DMA transfer.
[SFRs used]	DTFR0: 0x2A (Sets DMA start factor to UARTA0 reception end interrupt request (INTUA0R).)
	DCHC0: 0x01 (Enables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	uarta_port
[Processing content]	Sets to alternate-function pin.
[SFRs used]	PFC4: 0x03 (Sets TXDA0 output, RXDA0 input.)
	PFCE4: 0x00 (Sets TXDA0 output, RXDA0 input.)
	PMC4: 0x03 (Sets TXDA0 output, RXDA0 input.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	uarta_set
[Processing content]	Sets UARTA0 control register. Sets baud rate to 9,600 (bps).
[SFRs used]	UA0CTL1: 0x03 (Sets baud rate to 9,600 (bps).)
	UA0CTL2: 0xD0 (Sets baud rate to 9,600 (bps).)
	UA0OPT0: 0x14 (Sets to normal output/input of transfer data.)
	UA0CTL0: 0x8A (Enables UARTA0 operation, sets to MSB first, and sets odd parity to output, data character length to 8 bits, and stop bit length to 1 bit.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	uarta_start
[Processing content]	Enables UARTA0 reception operation.
[SFR used]	UA0CTL0.UA0RXE: 1 (Enables reception operation.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

Interrupt functions

[Function name]	dma_int
[Servicing content]	Disables DMA transfer after completion of DMA transfer.
[SFR used]	DCHC0.E00: 0 (Disables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

[Function name]	uarta_int_receive
[Servicing content]	Counts number of receptions and disables UARTA0 operation and reception operation.
[SFRs used]	UA0CTL0.UA0RXE: 0 (Disables reception operation.)
	UA0CTL0.UA0PWR: 0 (Disables UARTA0 operation.)
[call function]	None
[Variables]	unsigned char buf_rx[]: Receive data storing buffer
	volatile unsigned char count_rx: Reception count variable
[File name]	dma2.c
[Caution]	None

[Function name]	uarta_error
[Servicing content]	Clears error flag when a reception error occurs.
[SFRs used]	UA0STR.UA0PE: 0 (Clears parity error flag.)
	UA0STR.UA0FE: 0 (Clears framing error flag.)
	UA0STR.UA0OVE: 0 (Clears overrun error flag.)
[call function]	None
[Variable]	None
[File name]	dma2.c
[Caution]	None

Figure 1-2. Source of Interrupt from On-Chip Peripheral I/O (1/3)

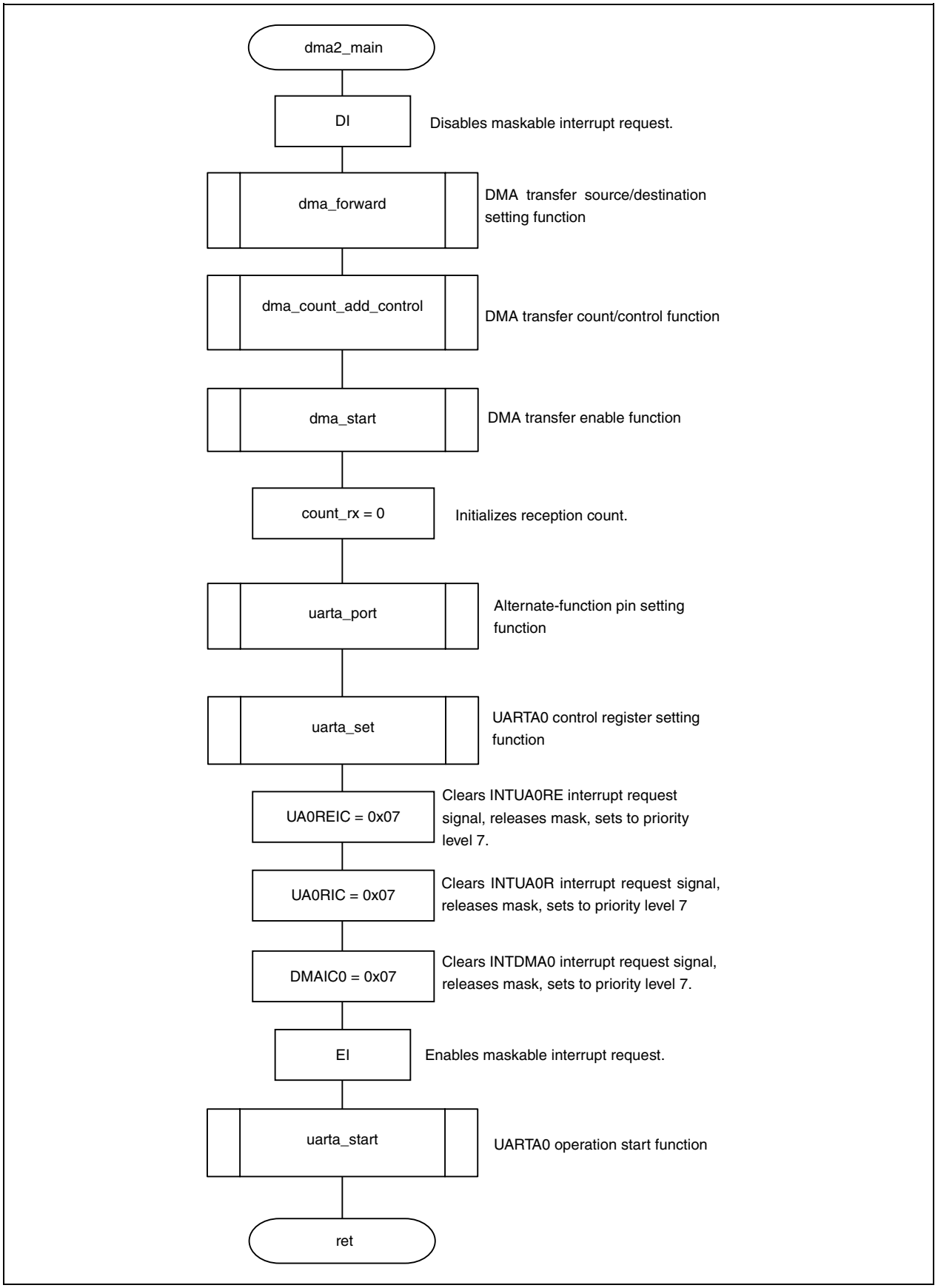


Figure 1-2. Source of Interrupt from On-Chip Peripheral I/O (2/3)

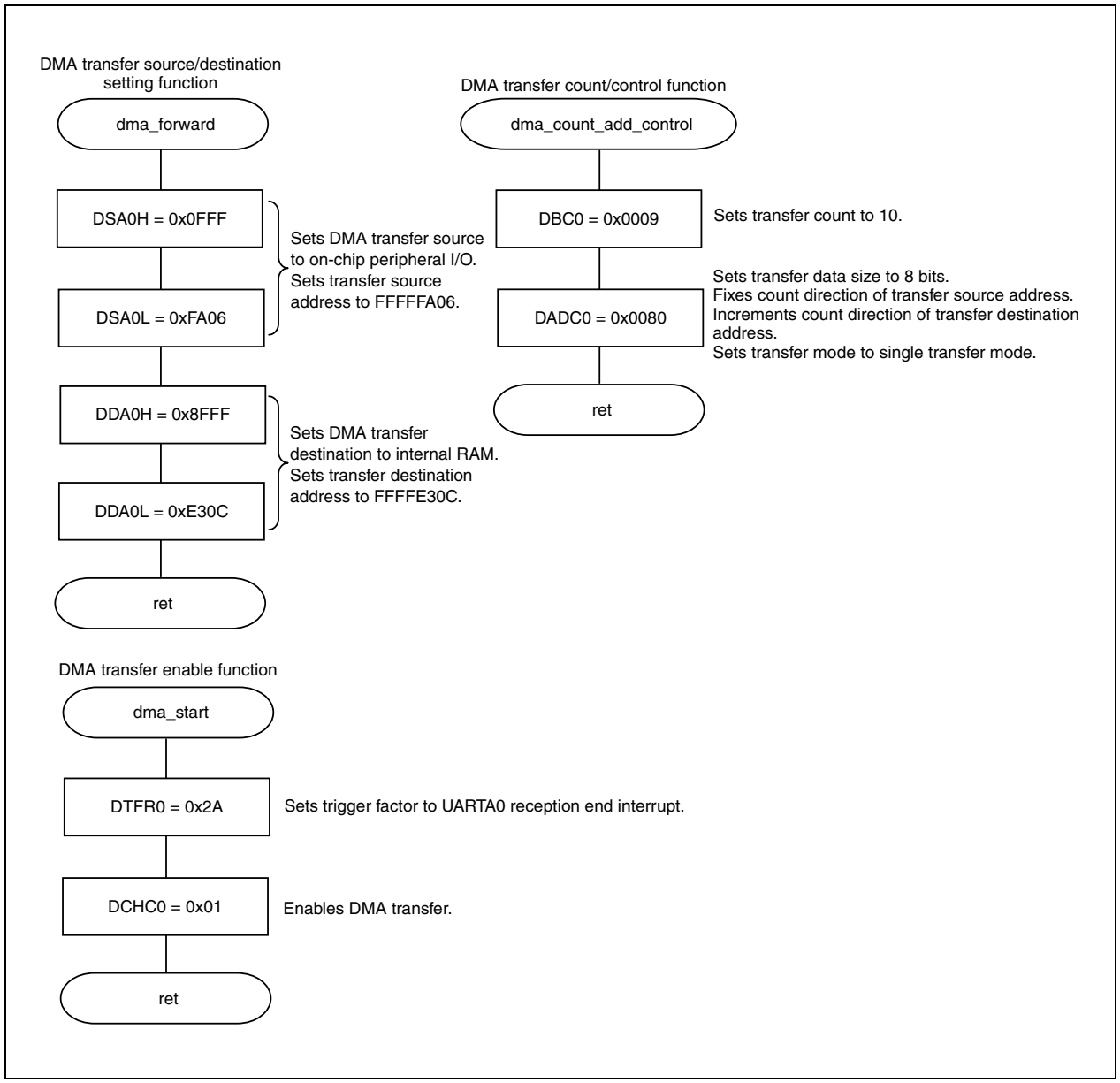
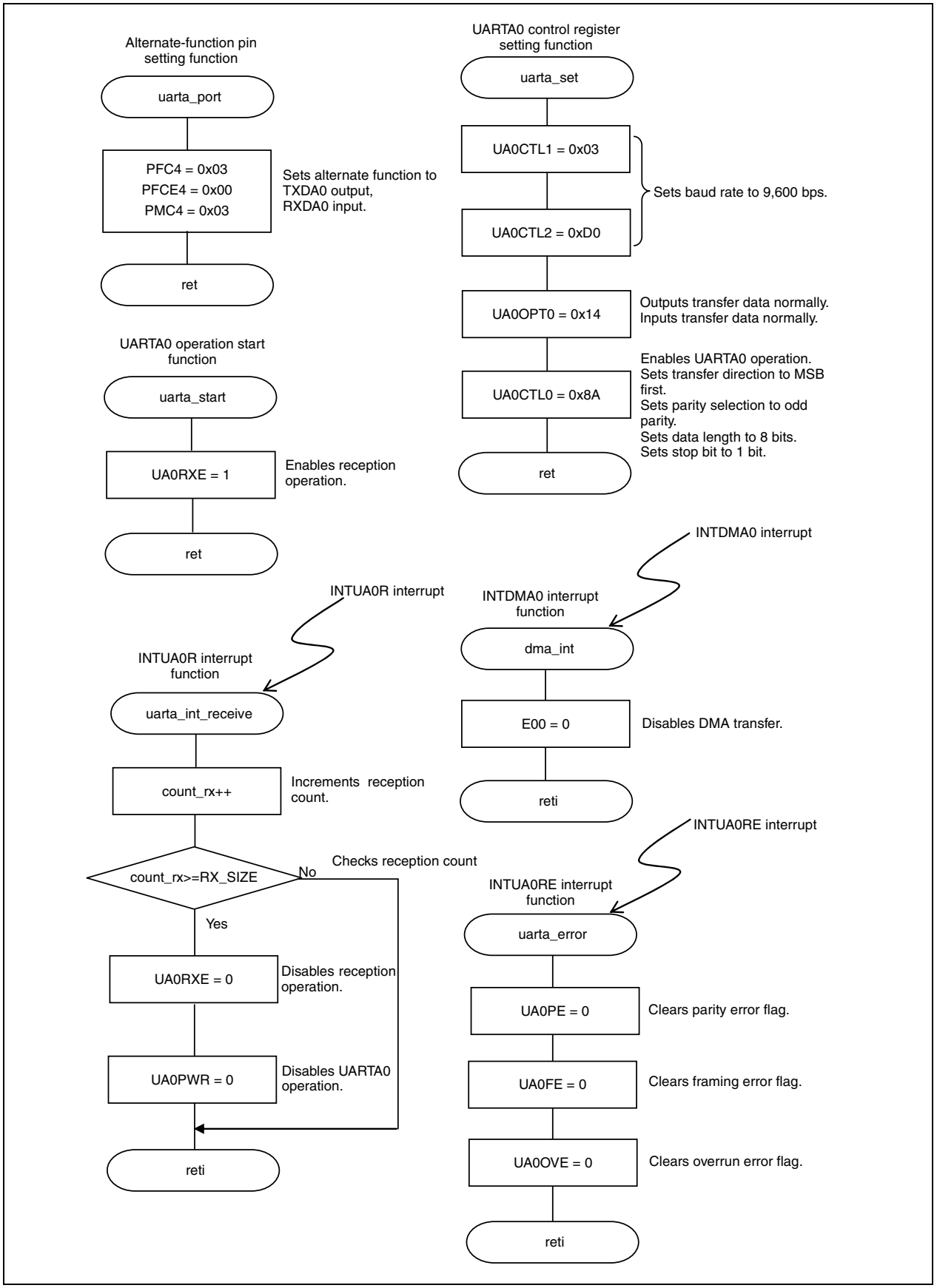


Figure 1-2. Source of Interrupt from On-Chip Peripheral I/O (3/3)



1.3 Forcible Termination of DMA

[Function]	Forcibly terminates DMA transfer.
[Function name]	dma3_main
[Argument]	None
[Processing content]	Performs transfer between on-chip peripheral I/O (UARTA0 receive data register) and internal RAM (buf_rx[]). The DMA start factor is a UARTA0 reception end interrupt request signal (INTUA0R). Forcibly terminates DMA transfer when 4 bytes of data are transferred.
[Starting method]	None
[SFRs used]	UA0REIC: 0x07 (Clears UARTA0 reception error interrupt request signal (INTUA0RE), releases mask and sets to priority level 7.) UA0RIC: 0x07 (Clears UARTA0 reception end interrupt request signal (INTUA0R), releases mask and sets to priority level 7.)
[call functions]	dma_forward, dma_count_add_control, dma_start, uarta_port, uarta_set, uarta_start
[Variables]	unsigned char buf_rx[]: Receive data storing buffer volatile unsigned char count_rx: Reception count variable
[Interrupts]	uarta_int_receive, uarta_error
[Interrupt sources]	INTUA0R, INTUA0RE
[File name]	dma3.c
[Caution]	None

[Function name]	dma_forward
[Processing content]	Specifies DMA transfer source/destination addresses.
[SFRs used]	DSA0H: 0x0FFF (Sets DMA transfer source to on-chip peripheral I/O and sets DMA source address.) DSA0L: 0xFA06 (Sets DMA transfer source address.) DDA0H: 0x8FFF (Sets DMA transfer destination to internal RAM and sets DMA transfer destination address.) DDA0L: 0xE30C (Sets DMA transfer destination address.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

[Function name]	dma_count_add_control
[Processing content]	Specifies DMA transfer counts and DMA transfer mode.
[SFRs used]	DBC0: 0x0009 (Sets 10 transfers.)
	DADC0: 0x0080 (Sets transfer data size to 8 bits, fixes count direction of transfer source addresses, increments count direction of transfer destination address, and sets to single transfer mode.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

[Function name]	dma_start
[Processing content]	Enables and starts DMA transfer.
[SFRs used]	DTFR0: 0x2A (Sets DMA start factor to UARTA0 reception end interrupt request (INTUA0R).)
	DCHC0: 0x01 (Enables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

[Function name]	uarta_port
[Processing content]	Sets to alternate-function pin.
[SFR used]	PFC4: 0x03 (Sets TXDA0 output, RXDA0 input.)
	PFCE4: 0x00 (Sets TXDA0 output, RXDA0 input.)
	PMC4: 0x03 (Sets TXDA0 output, RXDA0 input.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

[Function name]	uarta_set
[Processing content]	Sets UARTA0 control register. Sets baud rate to 9,600 (bps).
[SFRs used]	UA0CTL1: 0x03 (Sets baud rate to 9,600 (bps).)
	UA0CTL2: 0xD0 (Sets baud rate to 9,600 (bps).)
	UA0OPT0: 0x14 (Sets to normal output/input of transfer data.)
	UA0CTL0: 0x8A (Enables UARTA0 operation, sets to MSB first, and sets odd parity to output, data character length to 8 bits, and stop bit length to 1 bit.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

[Function name]	uarta_start
[Processing content]	Enables UARTA0 reception operation.
[SFR used]	UA0CTL0.UA0RXE: 1 (Enables reception operation.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

Interrupt functions

[Function name]	uarta_int_receive
[Servicing content]	Forcibly terminates operation when 4 bytes of receive data are acquired.
[SFRs used]	DCHC0.INIT0: 1 (Forcibly terminates DMA transfer.)
	DCHC0.E00: 0 (Disables DMA transfer.)
[call function]	None
[Variable]	volatile unsigned char count_rx: Reception count variable
[File name]	dma3.c
[Caution]	None

[Function name]	uarta_error
[Servicing content]	Clears error flag when a reception error occurs.
[SFRs used]	UA0STR.UA0PE: 0 (Clears parity error flag.)
	UA0STR.UA0FE: 0 (Clears framing error flag.)
	UA0STR.UA0OVE: 0 (Clears overrun error flag.)
[call function]	None
[Variable]	None
[File name]	dma3.c
[Caution]	None

Figure 1-3. Forcible Termination of DMA (1/3)

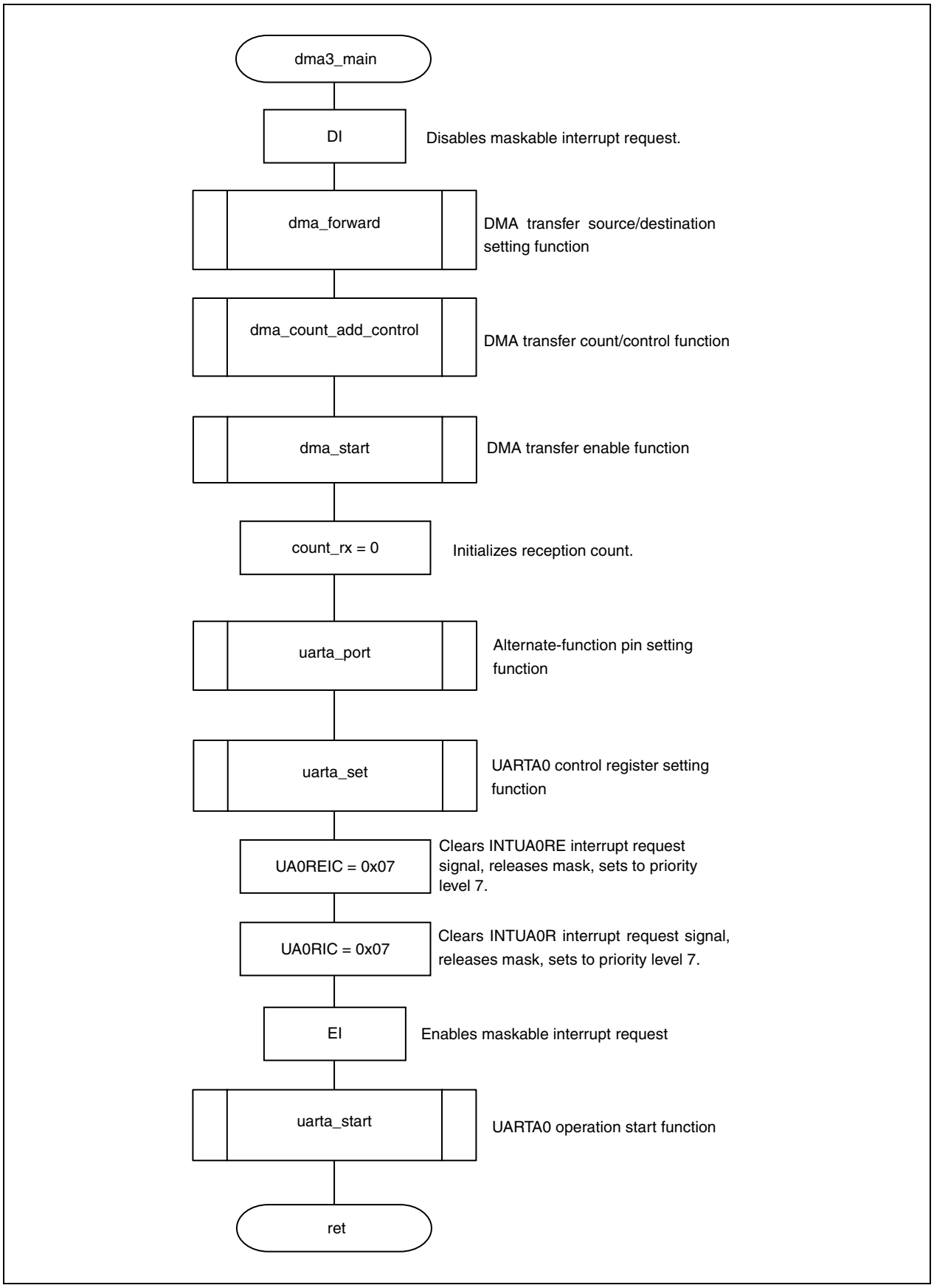


Figure 1-3. Forcible Termination of DMA (2/3)

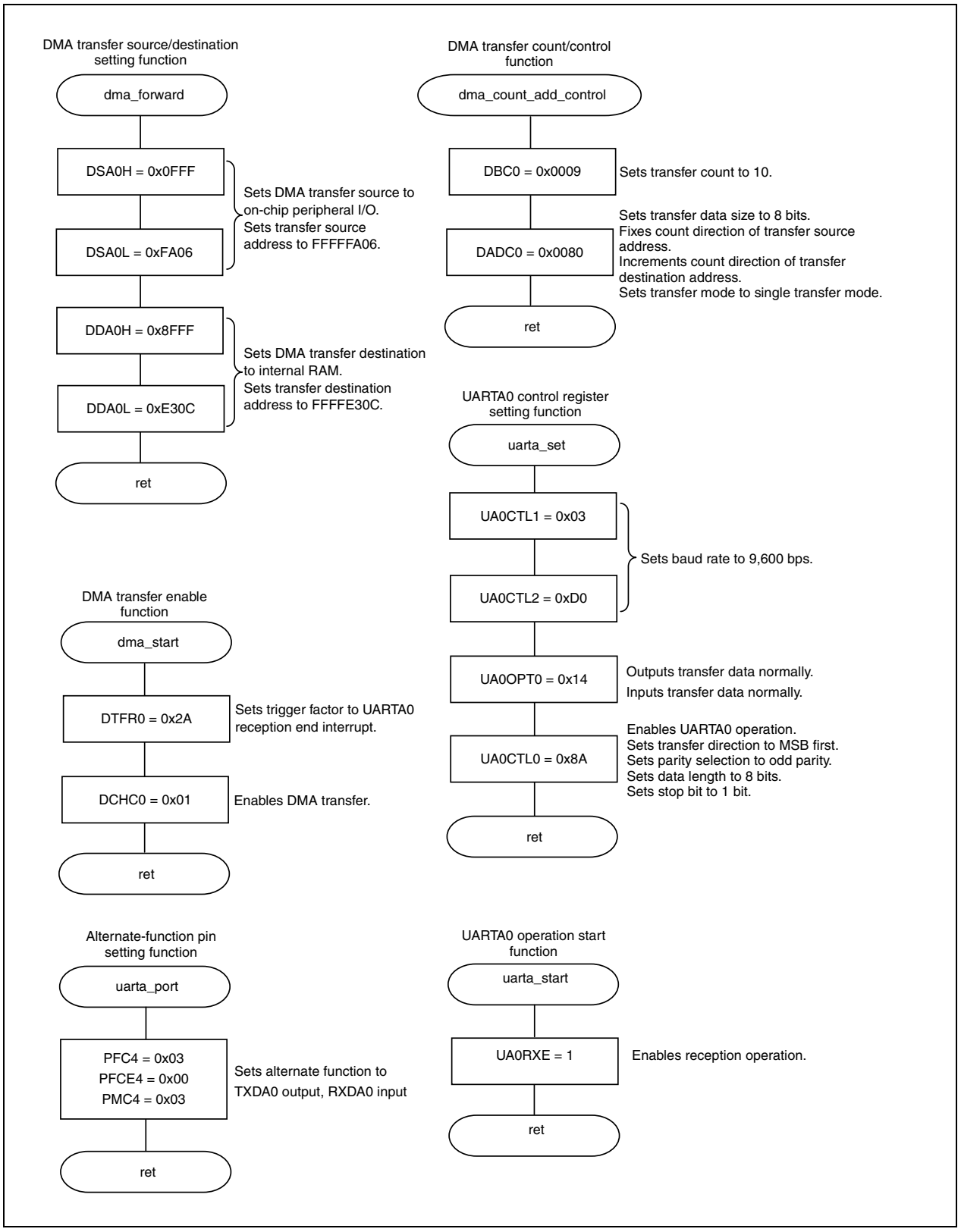
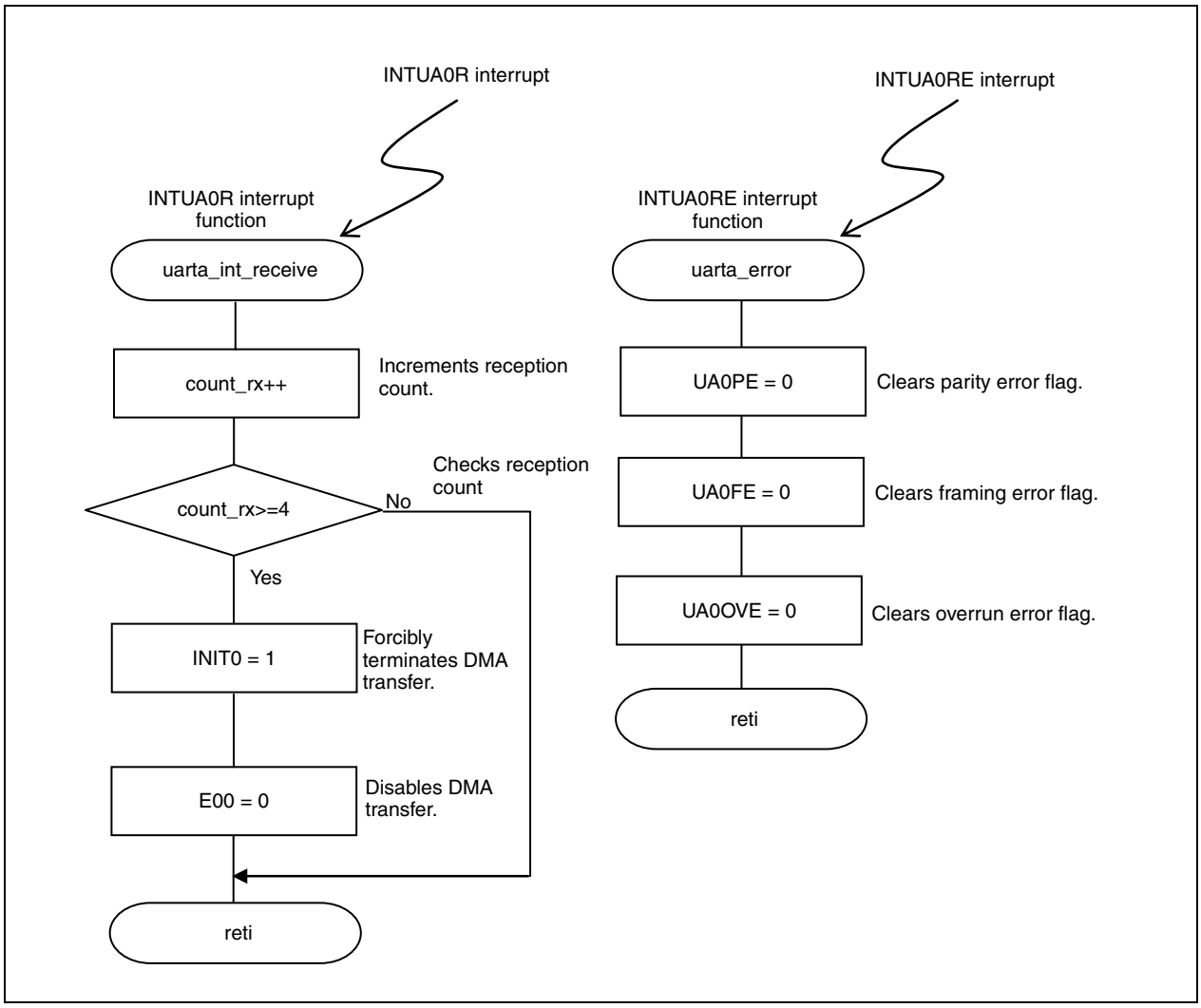


Figure 1-3. Forcible Termination of DMA (3/3)



CHAPTER 2 SINGLE-STEP TRANSFER MODE

2.1 Source of Interrupt from On-Chip Peripheral I/O

[Function]	Starts DMA transfer when an interrupt request from on-chip peripheral I/O that is set by the DTFR0 register occurs.
[Function name]	dma4_main
[Argument]	None
[Processing content]	Performs DMA transfer between on-chip peripheral I/O (UARTA0 receive data register) and internal RAM (buf_rx[]). The DMA start factor is a UARTA0 reception end interrupt request signal (INTUA0R). Generates INTDMA0 after 10 DMA transfers and completes transfer.
[Starting method]	None
[SFRs used]	UA0REIC: 0x07 (Clears UARTA0 reception error interrupt request signal (INTUA0RE), releases mask and sets to priority level 7.) UA0RIC: 0x07 (Clears UARTA0 reception end interrupt request signal (INTUA0R), releases mask and sets to priority level 7.) DMAIC0: 0x07 (Clears DMA0 transfer end interrupt request signal (INTDMA0), releases mask and sets to priority level 7.)
[call functions]	dma_forward, dma_count_add_control, dma_start, uarta_port, uarta_set, uarta_start
[Variables]	unsigned char buf_rx[]: Receive data storing buffer volatile unsigned char count_rx: Reception count variable
[Interrupts]	dma_int, uarta_int_erceive, uarta_error
[Interrupt sources]	INTDMA0, INTUA0R, INTUA0RE
[File name]	dma4.c
[Caution]	None

[Function name]	dma_forward
[Processing content]	Specifies DMA transfer source/destination addresses.
[SFRs used]	DSA0H: 0x0FFF (Sets DMA transfer source to on-chip peripheral I/O and sets DMA source address.)
	DSA0L: 0xFA06 (Sets DMA transfer source address.)
	DDA0H: 0x8FFF (Sets DMA transfer destination to internal RAM and sets DMA transfer destination address.)
	DDA0L: 0xE30C (Sets DMA transfer destination address.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	dma_count_add_control
[Processing content]	Specifies DMA transfer count/mode.
[SFRs used]	DBC0: 0x0009 (Sets 10 transfers.)
	DADC0: 0x0084 (Sets transfer data size to 8 bits, fixes count direction of transfer source addresses, increments count direction of transfer destination address, and sets to single-step transfer mode.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	dma_start
[Processing content]	Enables and starts DMA transfer.
[SFRs used]	DTFR0: 0x2A (Sets DMA start factor to UARTA0 reception end interrupt request (INTUA0R).)
	DCHC0: 0x01 (Enables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	uarta_port
[Processing content]	Sets to alternate-function pin.
[SFRs used]	PFC4: 0x03 (Sets to TXDA0 output, RXDA0 input.)
	PFCE4: 0x00 (Sets to TXDA0 output, RXDA0 input.)
	PMC4: 0x03 (Sets to TXDA0 output, RXDA0 input.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	uarta_set
[Processing content]	Sets UARTA0 control register. Sets baud rate to 9,600 (bps).
[SFRs used]	UA0CTL1: 0x03 (Sets baud rate to 9,600 (bps).)
	UA0CTL2: 0xD0 (Sets baud rate to 9,600 (bps).)
	UA0OPT0: 0x14 (Sets to normal output/input of transfer data.)
	UA0CTL0: 0x8A (Enables UARTA0 operation, sets to MSB first, and sets odd parity to output, data character length to 8 bits, and stop bit length to 1 bit.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	uarta_start
[Processing content]	Enables UARTA0 reception operation.
[SFR used]	UA0CTL0.UA0RXE: 1 (Enables reception operation.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

Interrupt functions

[Function name]	dma_int
[Processing content]	Disables DMA transfer after completion of DMA transfer.
[SFR used]	DCHC0.E00: 0 (Disables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

[Function name]	uarta_int_receive	
[Processing content]	Counts number of receptions and disables UARTA0 operation and reception operation.	
[SFRs used]	UA0CTL0.UA0RXE: 0 (Disables reception operation.)	
	UA0CTL0.UA0PWR: 0 (Disables UARTA0 operation.)	
[call function]	None	
[Variables]	unsigned char buf_rx[]:	Receive data storing buffer
	volatile unsigned char count_rx:	Reception count variable
[File name]	dma4.c	
[Caution]	None	

[Function name]	uarta_error
[Processing content]	Clears error flag when a reception error occurs.
[SFRs used]	UA0STR.UA0PE: 0 (Clears parity error flag.)
	UA0STR.UA0FE: 0 (Clears framing error flag.)
	UA0STR.UA0OVE: 0 (Clears overrun error flag.)
[call function]	None
[Variable]	None
[File name]	dma4.c
[Caution]	None

Figure 2-1. Source of Interrupt from On-Chip Peripheral I/O (1/3)

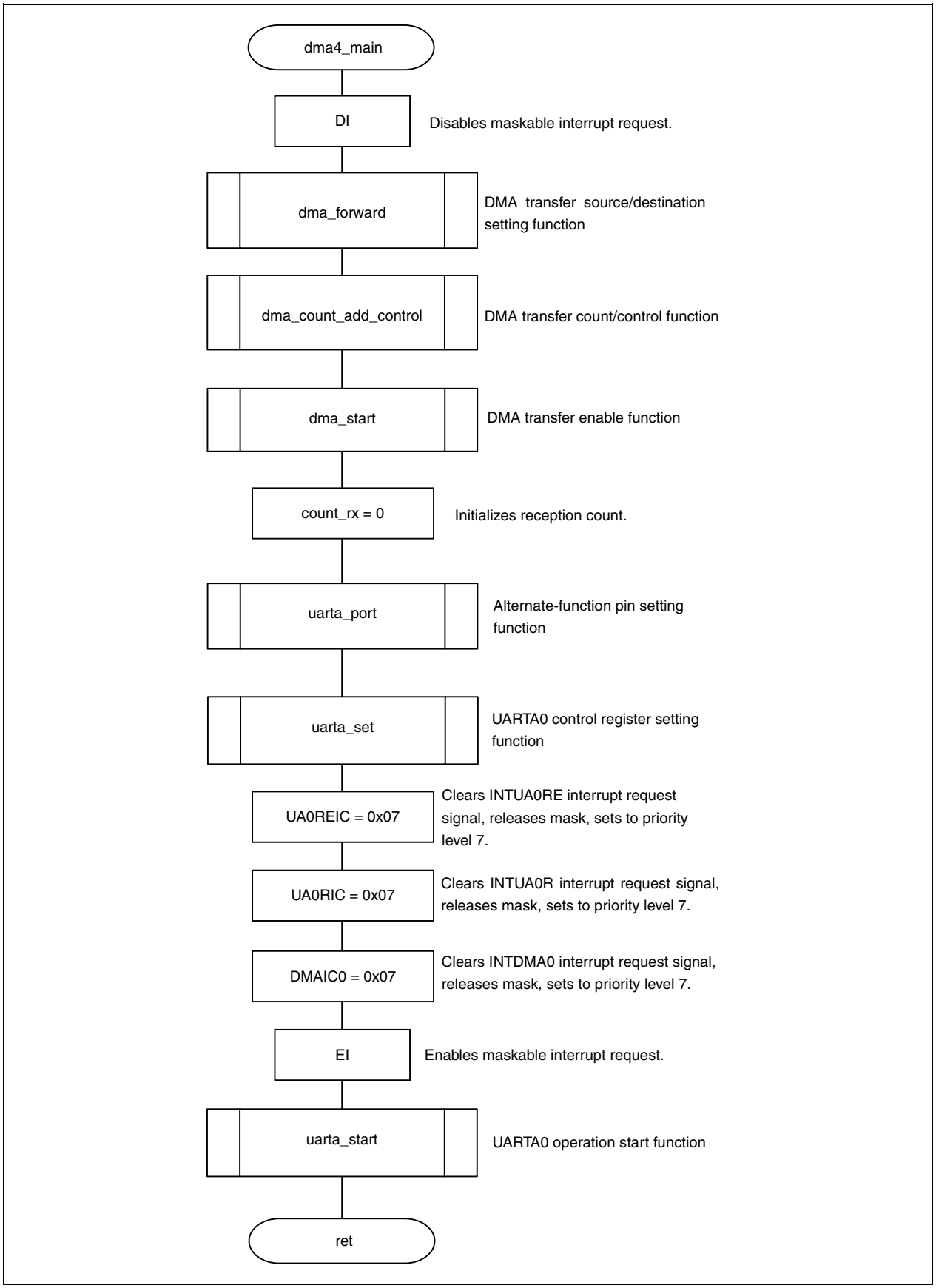


Figure 2-1. Source of Interrupt from On-Chip Peripheral I/O (2/3)

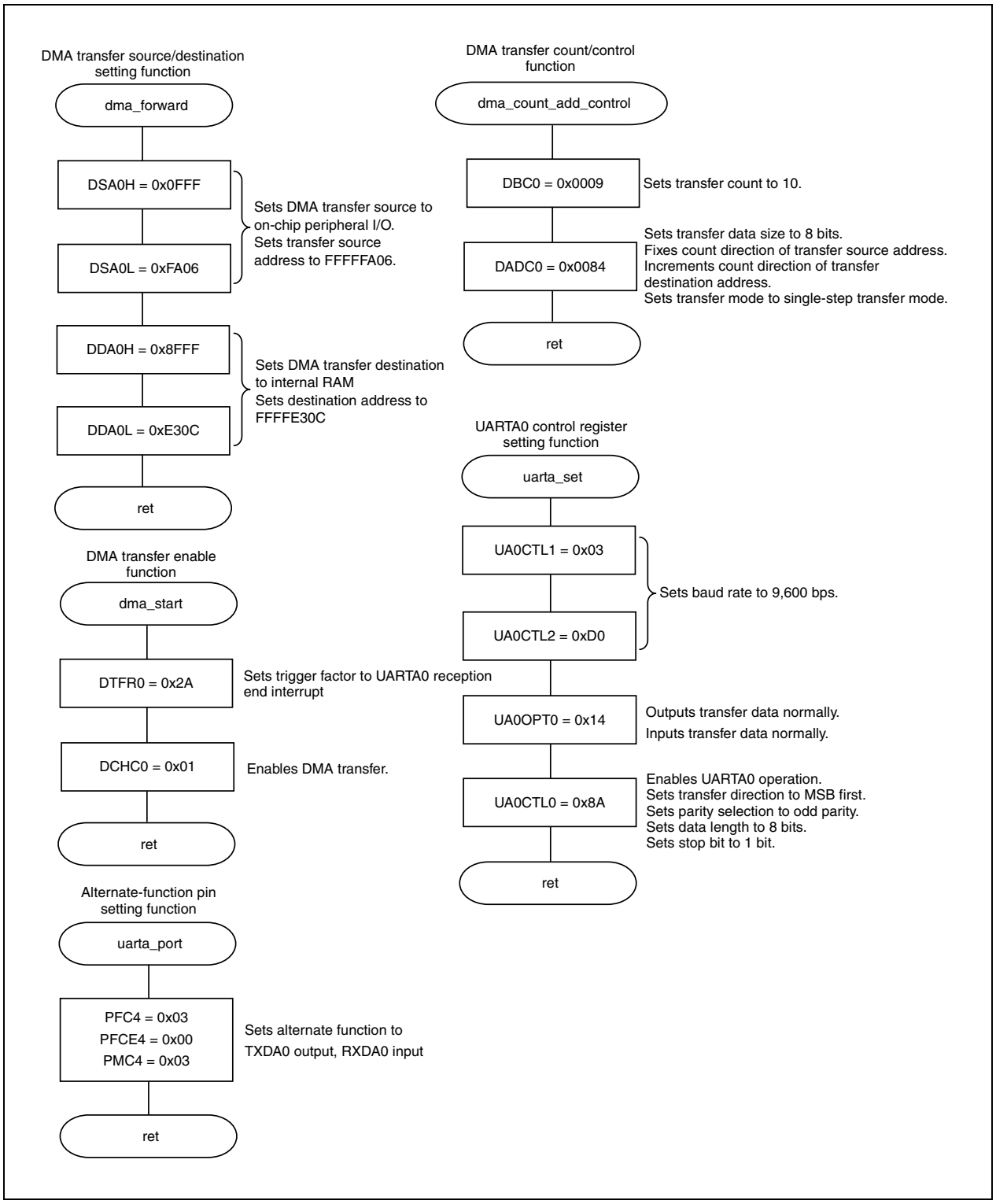
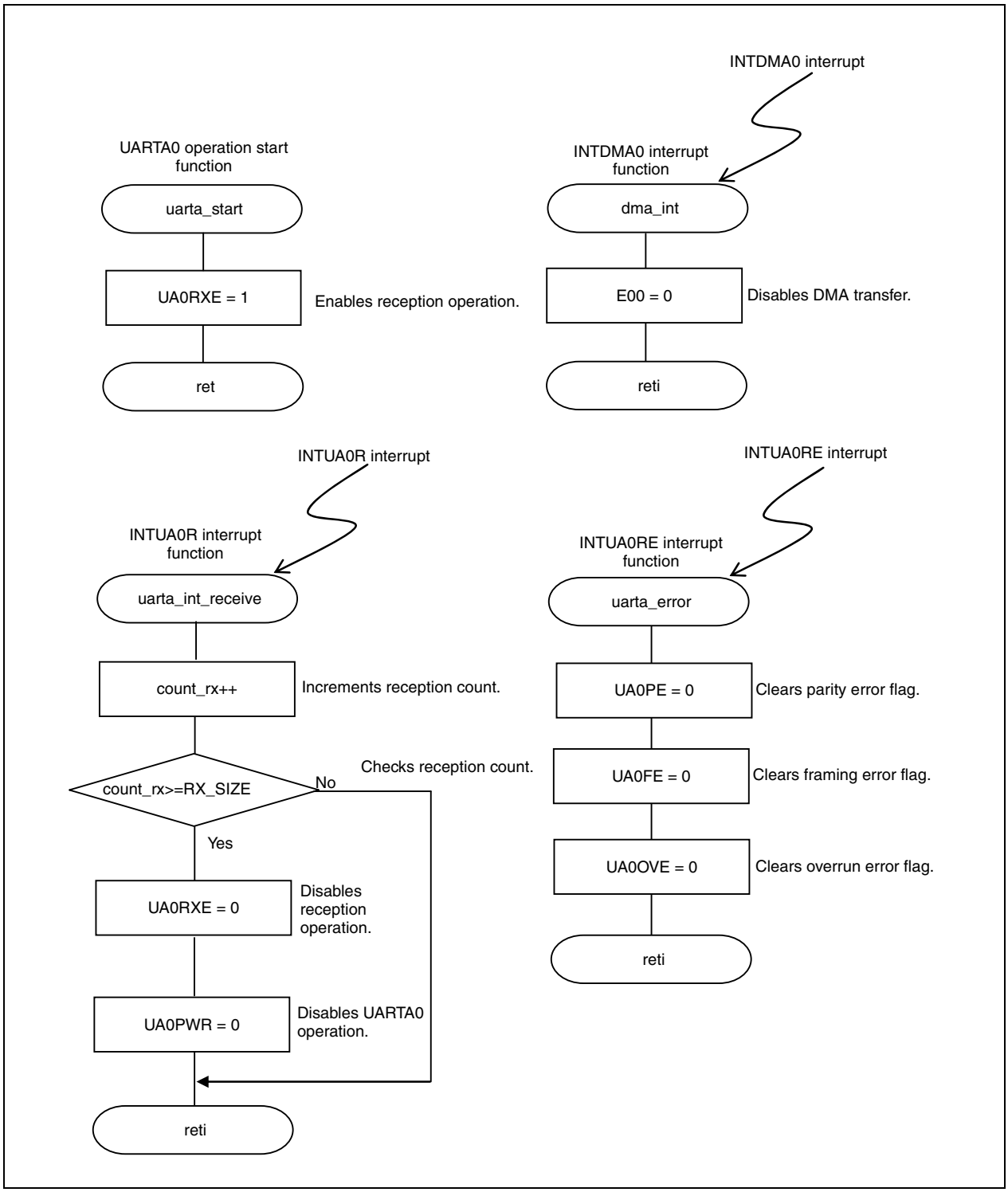


Figure 2-1. Source of Interrupt from On-Chip Peripheral I/O (3/3)



CHAPTER 3 BLOCK TRANSFER MODE

3.1 Source of Interrupt from On-Chip Peripheral I/O

[Function]	Starts DMA transfer when an interrupt request from on-chip peripheral I/O that is set by the DTFR0 register occurs.
[Function name]	dma5_main
[Argument]	None
[Processing content]	Performs DMA transfer between on-chip peripheral I/O (UARTA0 receive data register) and internal RAM (buf_rx[]). The DMA start factor is a UARTA0 reception end interrupt request signal (INTUA0R). Generates INTDMA0 after 10 DMA transfers and completes transfer.
[Starting method]	None
[SFRs used]	UA0REIC: 0x07 (Clears UARTA0 reception error interrupt request signal (INTUA0RE), releases mask, and sets to priority level 7.) UA0RIC: 0x07 (Clears UARTA0 reception end interrupt request signal (INTUA0R), releases mask, and sets to priority level 7.) DMAIC0: 0x07 (Clears DMA0 transfer end interrupt request signal (INTDMA0), releases mask, and sets to priority level 7.)
[call functions]	dma_forward, dma_count_add_control, dma_start, uarta_port, uarta_set, uarta_start
[Variables]	unsigned char buf_rx[]: Receive data storing buffer volatile unsigned char count_rx: Reception count variable
[Interrupts]	dma_int, uarta_int_receive, uarta_error
[Interrupt sources]	INTDMA0, INTUA0R, INTUA0RE
[File name]	dma5.c
[Caution]	None

[Function name]	dma_forward
[Processing content]	Specifies DMA transfer source/destination addresses.
[SFRs used]	DSA0H: 0x0FFF (Sets DMA transfer source to on-chip peripheral I/O and sets DMA transfer source address.) DSA0L: 0xFA06 (Sets DMA transfer source address.) DDA0H: 0x8FFF (Sets DMA transfer destination to internal RAM and sets DMA transfer destination address.) DDA0L: 0xE30C (Sets DMA transfer destination address.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	dma_count_add_control
[Processing content]	Specifies DMA transfer count/mode.
[SFRs used]	DBC0: 0x0009 (Sets 10 transfers.) DADC0: 0x008C (Sets transfer data size to 8 bits, fixes count direction of transfer source addresses, increments count direction of transfer destination address, and sets to block transfer mode.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	dma_start
[Processing content]	Enables and starts DMA transfer.
[SFRs used]	DTFR0: 0x2A (Sets DMA start factor to UARTA0 reception end interrupt request (INTUA0R).) DCHC0: 0x01 (Enables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	uarta_port
[Processing content]	Sets to alternate-function pin.
[SFRs used]	PFC4: 0x03 (Sets to TXDA0 output, RXDA0 input.)
	PFCE4: 0x00 (Sets to TXDA0 output, RXDA0 input.)
	PMC4: 0x03 (Sets to TXDA0 output, RXDA0 input.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	uarta_set
[Processing content]	Sets UARTA0 control register. Sets baud rate to 9,600 (bps).
[SFRs used]	UA0CTL1: 0x03 (Sets baud rate to 9,600 (bps).)
	UA0CTL2: 0xD0 (Sets baud rate to 9,600 (bps).)
	UA0OPT0: 0x14 (Sets to normal output/input of transfer data.)
	UA0CTL0: 0x8A (Enables UARTA0 operation, sets to MSB first, and sets odd parity to output, data character length to 8 bits, and stop bit length to 1 bit.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	uarta_start
[Processing content]	Enables UARTA0 reception operation.
[SFR used]	UA0CTL0.UA0RXE: 1 (Enables reception operation.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

Interrupt functions

[Function name]	dma_int
[Servicing content]	Disables DMA transfer after completion of DMA transfer.
[SFR used]	DCHC0.E00: 0 (Disables DMA transfer.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

[Function name]	uarta_int_receive
[Servicing content]	Counts number of receptions and disables UARTA0 operation and reception operation.
[SFRs used]	UA0CTL0.UA0RXE: 0 (Disables reception operation.)
	UA0CTL0.UA0PWR: 0 (Disables UARTA0 operation.)
[call function]	None
[Variables]	unsigned char buf_rx[]: Receive data storing buffer
	volatile unsigned char count_rx: Reception count variable
[File name]	dma5.c
[Caution]	None

[Function name]	uarta_error
[Servicing content]	Clears error flag when a reception error occurs.
[SFRs used]	UA0STR.UA0PE: 0 (Clears parity error flag.)
	UA0STR.UA0FE: 0 (Clears framing error flag.)
	UA0STR.UA0OVE: 0 (Clears overrun error flag.)
[call function]	None
[Variable]	None
[File name]	dma5.c
[Caution]	None

Figure 3-1. Source of Interrupt from On-Chip Peripheral I/O (1/3)

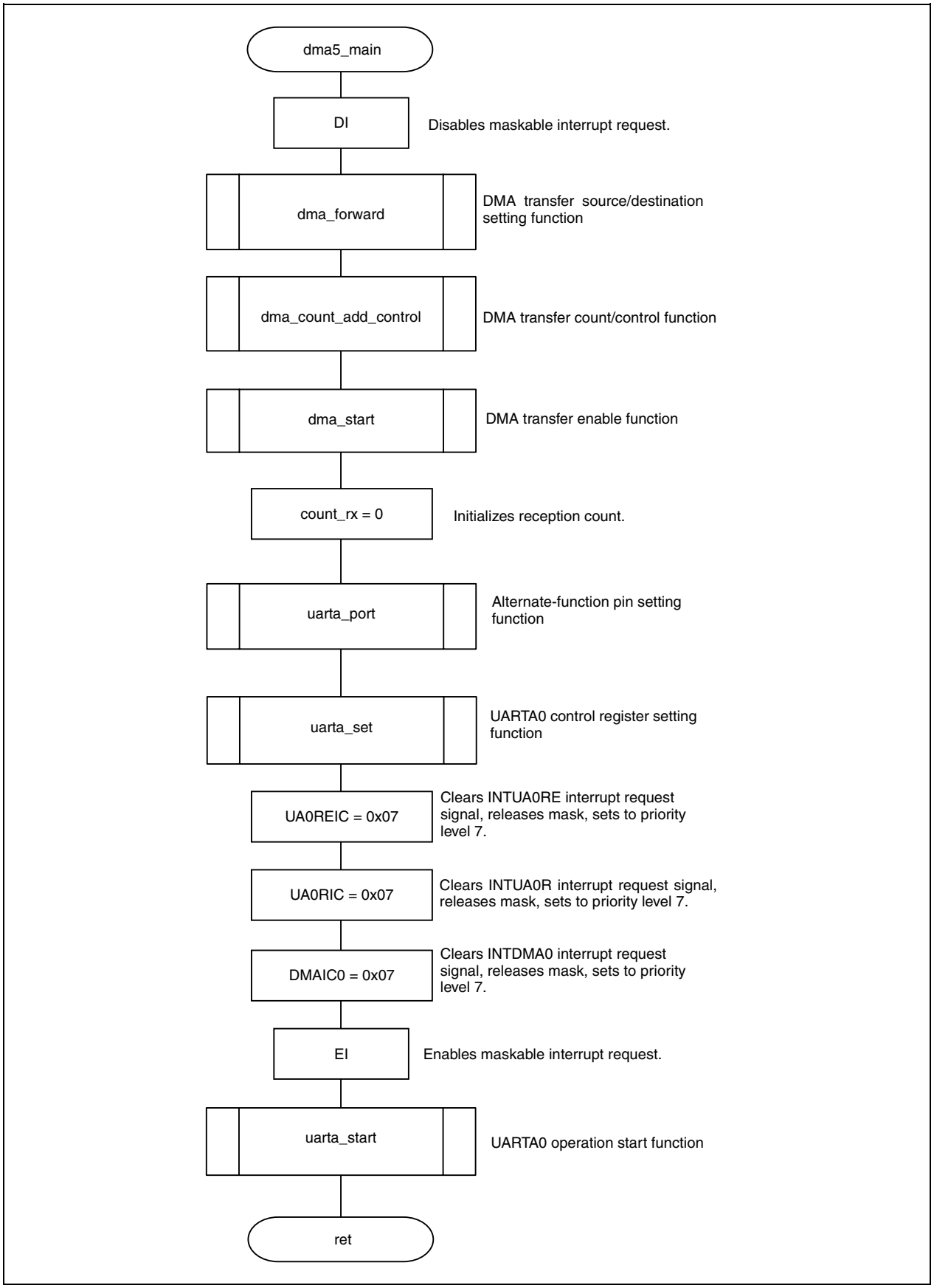


Figure 3-1. Source of Interrupt from On-Chip Peripheral I/O (2/3)

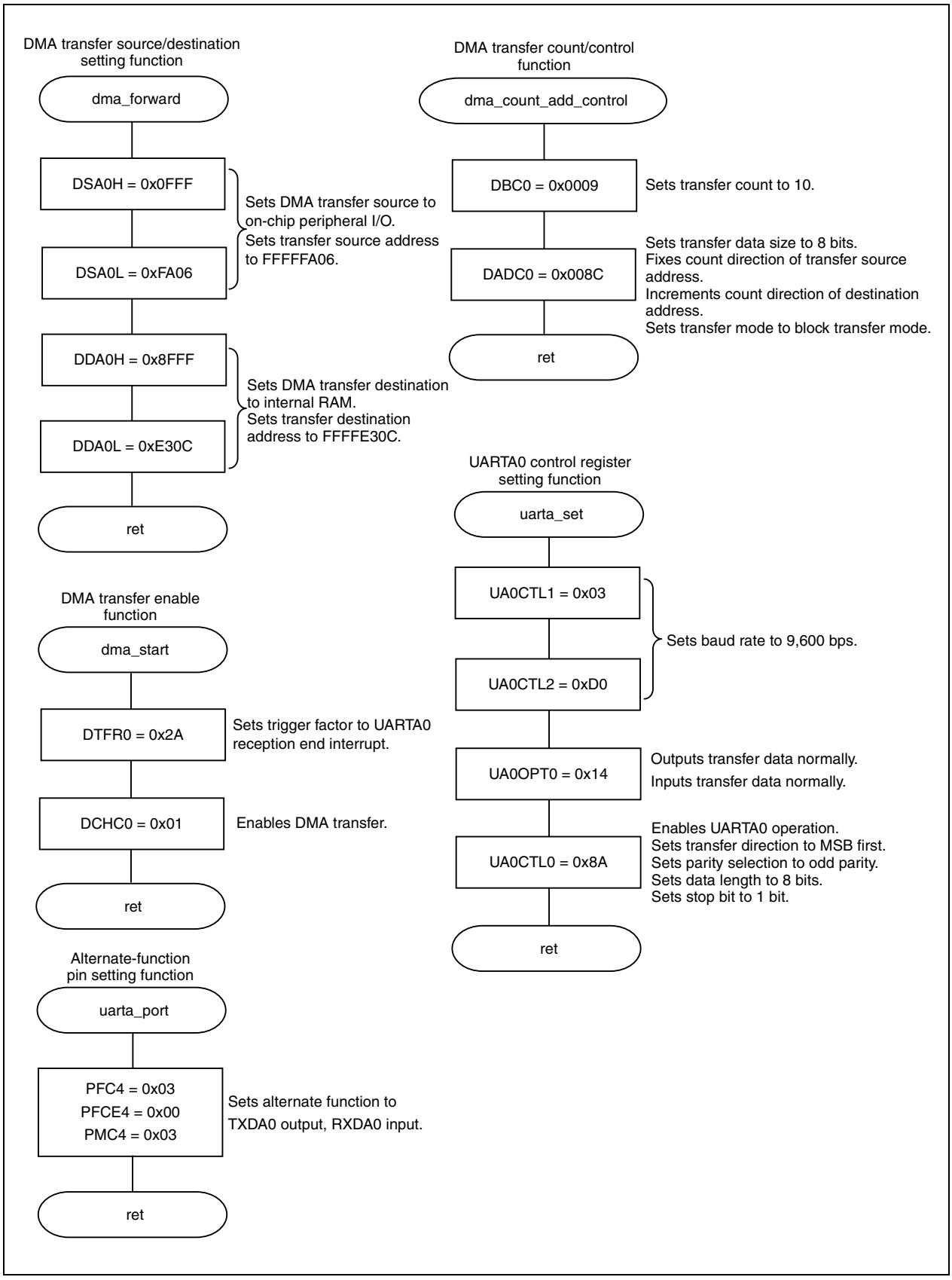
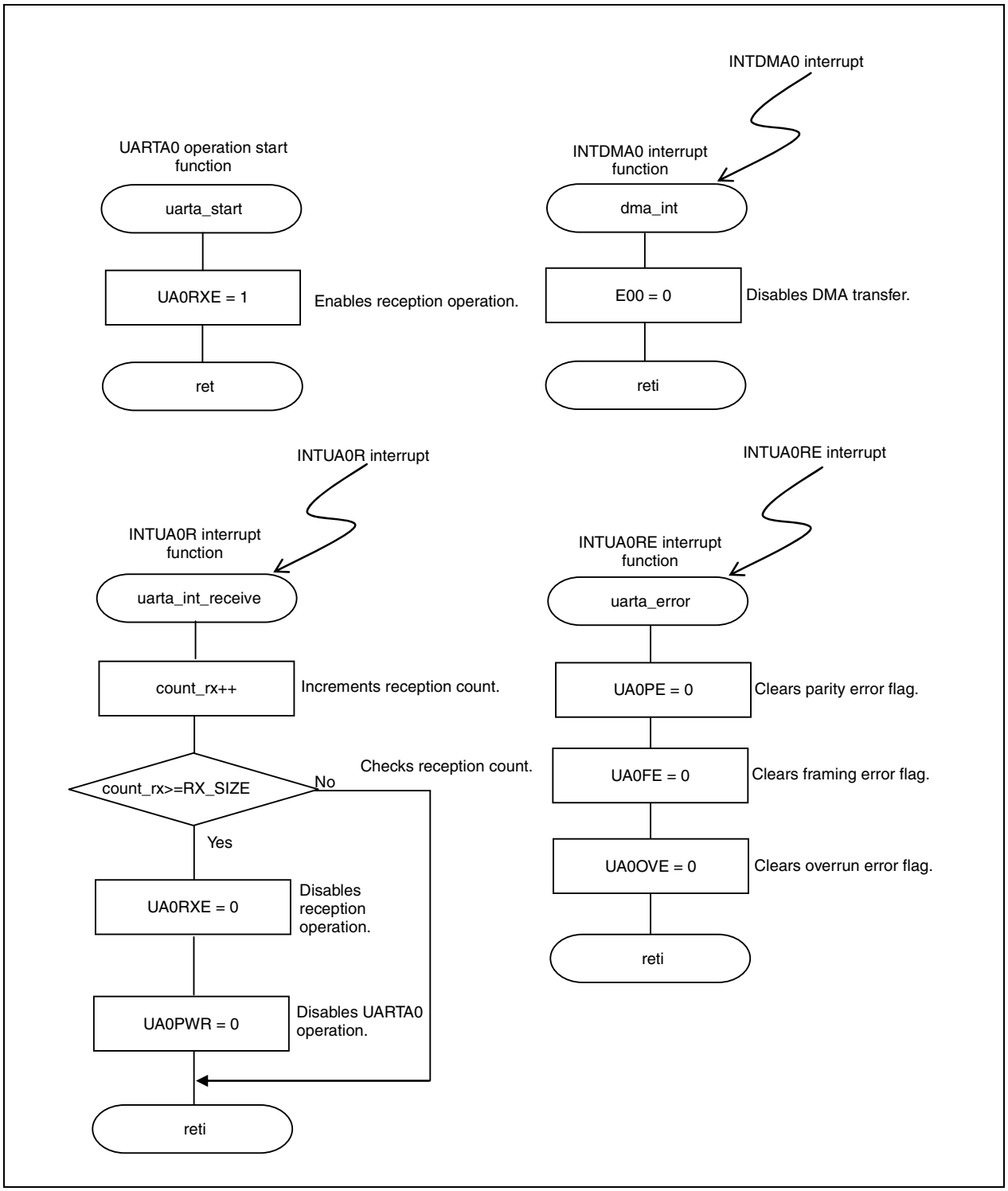


Figure 3-1. Source of Interrupt from On-Chip Peripheral I/O (3/3)



For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

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