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H8/300H Tiny Series

Using Timer V 8-Bit Event Counter Function to Measure Input Pulses

Introduction

Timer V's 8-bit event counter function is used to count the number of rising edges of the pulses input from the timer V event input pin (TMCIV).

Target Device

H8/3664

Contents

1. Specifications

1. Timer V's 8-bit event counter function is used to count the number of rising edges of the pulses input from the timer V event input pin (TMCIV).
2. The timer counter V (TCNTV) is specified to be incremented on the rising edge of the external clock and to continue counting up until the TCNTV value becomes H'0xF0.
3. When the TCNTV counter value reaches H'0xF0, the external clock input to the TCNTV is stopped and the processing ends.

2. Description of Functions Used

1. In this sample task, the 8-bit event counter function is used to count the number of pulses input from the TMCIV input pin. Figure 2.1 is a block diagram of the 8-bit event counter function of timer V. The elements in the block diagram are described below.

- Timer control register V0 (TCRV0) selects the TCNTV input clock and the condition for clearing of TCNTV, and enables or disables various interrupt requests. In this sample task, the TCNTV's input clock is specified as a rising edge of the external clock, the TCNTV is specified not to be cleared, and compare-match A interrupt requests are enabled.
- Timer control/status register V (TCSRV) is an 8-bit register that sets the compare-match flag, sets timer overflow flag, and controls the compare-match output. In this sample task, output on the TMOV pin is disabled.
- Time constant register A (TCORA) is always compared with TCNTV. If TCORA matches TCNTV, a compare-match A interrupt occurs.
- Timer counter V (TCNTV) is an 8-bit readable/writable up-counter that is incremented by internal or external clock input. The input clock can be selected from six clocks generated by dividing ϕ or three external clocks.
- Timer control register V1 (TCRV1), in combination with TCRV0, selects the input clock of TCNTV.
- The value of TCNTV is always compared with that of TCORA. If TCNTV matches TCORA, the compare-match flag A (CMFA) is set to 1. In this case, if the compare-match interrupt enable A (CMIEA) bit of TCRV0 is set to 1, a compare-match A interrupt is requested to the CPU.

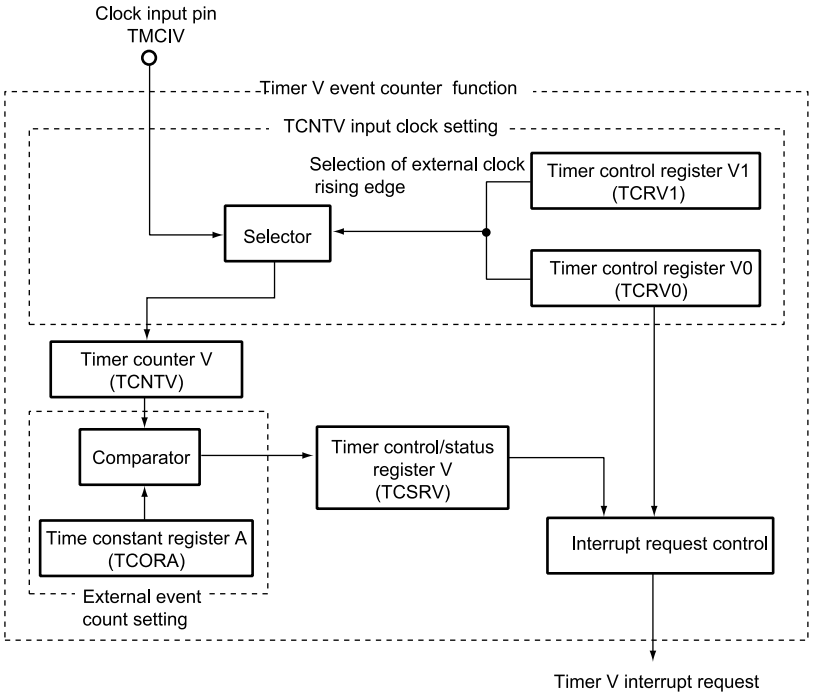


Figure 2.1 Block Diagram of Timer V

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that the number of input pulses can be counted by the 8-bit event counter function of the timer V.

Table 2.1 Function Allocation

Function	Description
TCRV0	Sets up the compare-match A interrupt function.
TCSRV	Sets the timer V compare-match interrupt flag.
TCRV1	Specifies the TCNTV to count the number of rising edges of an external clock.
TCORA	Compared with the timer V counter (TCNTV).
TCNTV	Timer V counter
TMCIV pin	External clock input pin

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in this figure applies the 8-bit event counter function of timer V to count the number of input pulses.

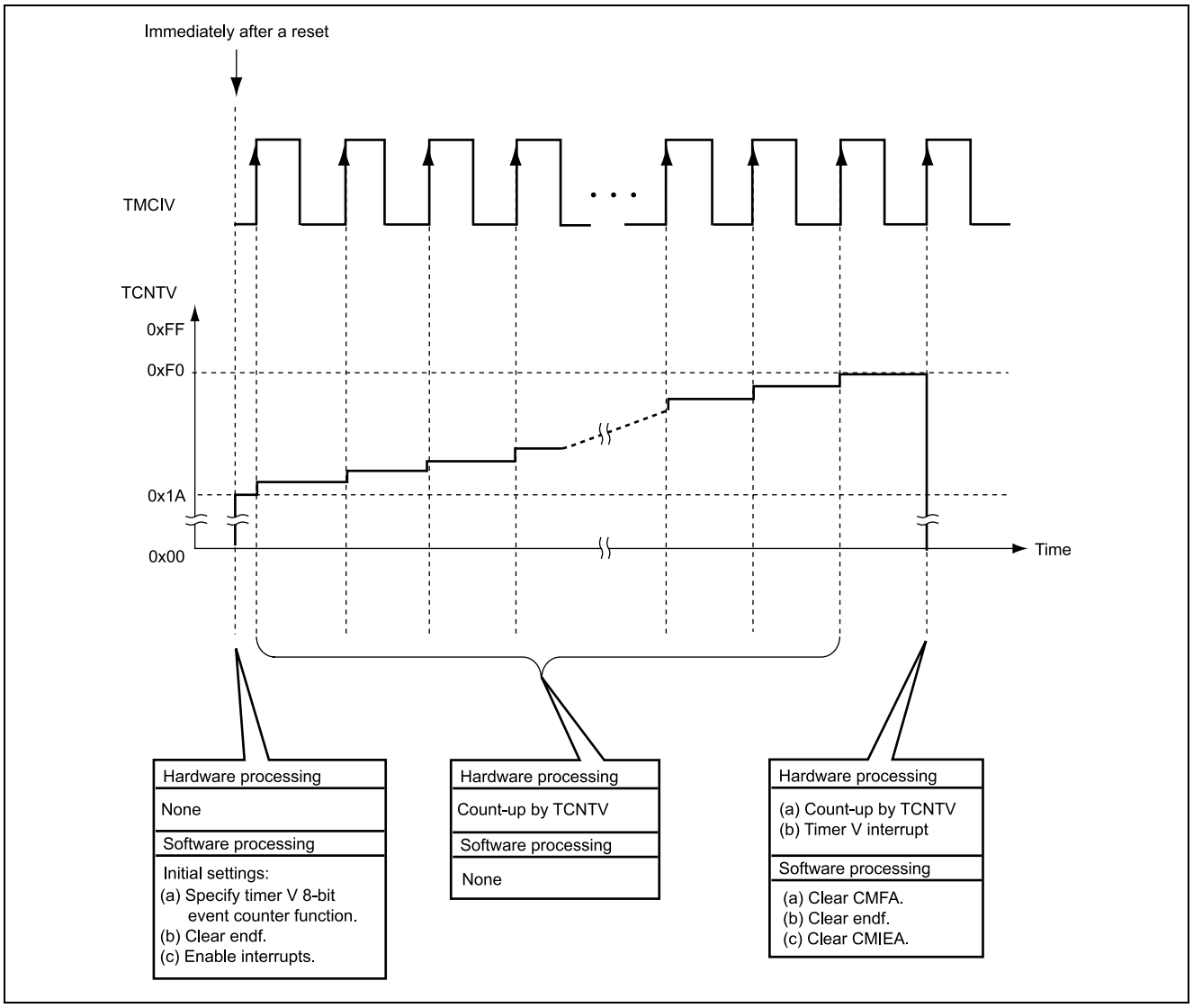


Figure 3.1 Operation Principle

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Specifies compare-match A, initializes TCNTV, and provide setting for the TMCIV clock input pin.
Timer V interrupt	tvint	This module is the timer V compare-match A interrupt handling routine that clears the CMFA and CMIEA flags and sets the endf flag.

4.2 Description of Arguments

This sample task uses no arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TCRV0 Timer control register V0 Address: 0xFFA0

Bit	Bit Name	Setting	Function
6	CMIEA	1	Compare match interrupt enable A CMIEA = 0: Disables interrupt-generation according to the value of the compare-match flag A (CMFA). CMIEA = 1: Enables interrupt-generation according to the value of the compare-match flag A (CMFA).
2	CKS2	CKS2 = 1	Clock select
1	CKS1	CKS1 = 0	CKS2 = 1, CKS1 = 0, CKS0 = 1:
0	CKS0	CKS0 = 1	TCNTV is incremented on the rising edge of an external clock.

- TCSRV Timer control/status register V Address: 0xFFA1

Bit	Bit Name	Setting	Function
6	CMFA	0	Compare match flag A CMFA = 0: Indicates that no compare-match has occurred. CMFA = 1: Indicates that a compare-match has occurred.

- TCORA Time constant register A Address: 0xFFA2
  Function: f the TCNTV counter value matches the TCORA, a compare-match A occurs.
  Setting: xF0

- TCNTV Timer counter V Address: 0xFFA4
  Function: n 8-bit up-counter that is incremented by the rising edge of an external clock.
  Setting: x00

- TCRV1 Timer control register V1 Address: 0xFFF5

Bit	Bit Name	Setting	Function
4	TVEG1	TVEG1 = 0	TVEG1 = 0, TVEG0 = 0: Disables trigger input on the TRGV pin.
3	TVEG0	TVEG0 = 0	
2	TRGE	0	TRGE = 0: Disables starting of TCNTV counting by the input on the TRGV pin and halting of TCNTV counting when TCNTV is cleared upon a compare-match. TRGE = 1: Enables starting of TCNTV counting by the input on the TRGV pin and halting of TCNTV counting when TCNTV is cleared upon a compare-match.

4.4 Description of RAM

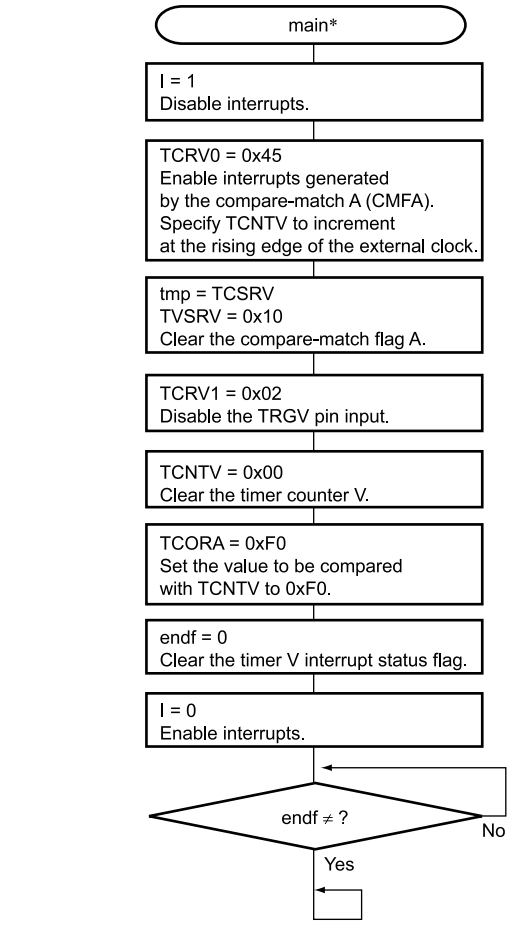
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
endf	A flag that indicates whether rising edges of the input pulses have been detected 0xF0 times. endf = 0: Rising edges have not been detected 0xF0 times. endf = 1: Rising edges have been detected 0xF0 times.	1 byte	Main routine Timer V interrupt

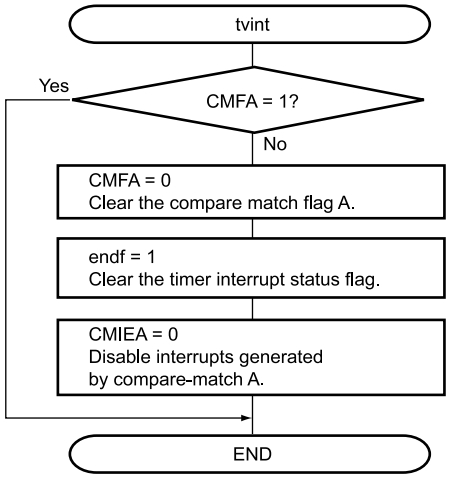
5. Flowchart

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Count up



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3664-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Measurement of Input Pulses by 8-bit                                                                              */
/*   Event Counter Function'                                                                                            */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer V 8bit Event Counter                                                                                       */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/
#include    <machine.h>
/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCRV0          *(volatile unsigned char *)0xFFA0                  /* Timer Control Register V0               */
#define        TCRV0_BIT      (*(struct BIT *)0xFFA0)                            /* Timer Control Register V0               */
#define        CMIEB          TCRV0_BIT.b7                                       /* Compare Match Interrupt Enable B        */
#define        CMIEA          TCRV0_BIT.b6                                       /* Compare Match Interrupt Enable A        */
#define        OVIE           TCRV0_BIT.b5                                       /* Timer Overflow Interrupt Enable         */
#define        CCLR1          TCRV0_BIT.b4                                       /* Counter Clear 1                         */
#define        CCLR0          TCRV0_BIT.b3                                       /* Counter Clear 0                         */
#define        CKS2           TCRV0_BIT.b2                                       /* Clock Select 2                          */
#define        CKS1           TCRV0_BIT.b1                                       /* Clock Select 1                          */
#define        CKS0           TCRV0_BIT.b0                                       /* Clock Select 0                          */
#define        TCSRV          *(volatile unsigned char *)0xFFA1                  /* Timer Control/Status Register V         */
#define        TCSRV_BIT      (*(struct BIT *)0xFFA1)                            /* Timer Control/Status Register V         */
#define        CMFB           TCSRV_BIT.b7                                       /* Compare Match Flag B                    */
#define        CMFA           TCSRV_BIT.b6                                       /* Compare Match Flag A                    */
#define        OVF            TCSRV_BIT.b5                                       /* Timer Overflow Flag                     */
#define        OS3            TCSRV_BIT.b3                                       /* Output Select 3                         */
#define        OS2            TCSRV_BIT.b2                                       /* Output Select 2                         */
#define        OS1            TCSRV_BIT.b1                                       /* Output Select 1                         */
#define        OS0            TCSRV_BIT.b0                                       /* Output Select 0                         */
#define        TCORA          *(volatile unsigned char *)0xFFA2                  /* Time constant register A                */
#define        TCORB          *(volatile unsigned char *)0xFFA3                  /* Time constant register B                */
#define        TCNTV          *(volatile unsigned char *)0xFFA4                  /* Timer counter V                         */
#define        TCRV1          *(volatile unsigned char *)0xFFA5                  /* Timer control register V1               */
```

```
#define        TCRV1_BIT      (*(struct BIT *)0xFFA5)                    /* Timer control register V1              */
#define        TVEG1          TCRV1_BIT.b4                               /* TRGV Input Edge Select 1               */
#define        TVEG0          TCRV1_BIT.b3                               /* TRGV Input Edge Select 0               */
#define        TRGE           TCRV1_BIT.b2                               /* TCNTV starts counting up               */
#define        ICKS0          TCRV1_BIT.b0                               /* Internal Clock Select 0                */

#pragma interrupt   (tvint)

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                               /* SP Set                                 */
void main ( void );
void tvint ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  endf;                                            /* End Flag                               */

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section                                                                                                          /*
VECTOR SECTOIN SET  */
void (*const VEC_TBL1[])(void) = {                                       /* 0x00 - 0x0f                            */
     INIT                                                                /* 00 Reset                               */
};
#pragma section     V2                                                   /* VECTOR SECTOIN SET                     */
void (*const VEC_TBL2[])(void) = {
     tvint                                                               /* 2C Timer V Interrupt                   */
};

#pragma section                                                          /* P                                      */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                                   /* Interrupt Disable                      */

     TCRV0 = 0x45;                                                       /* Set Outside Clock Count                */
                                                                         /* CMFA Interrupt Enable                  */
     tmp = TCSRV;
     TCSRV = 0x10;                                                       /* Clear CMFA                             */
     TCRV1 = 0x02;                                                       /* Not use TRGV                           */
     TCNTV = 0x00;                                                       /* Timer Counter V Clear                  */
     TCORA = 0xF0;                                                       /* Set Max Value                          */

     endf = 0;                                                           /* Initialize endf                        */
     set_imask_ccr(0);                                                   /* Interrupt Enable                       */

     while(endf != 1);                                                   /* ENDF = 1 ?                             */

     while(1);
}
```

```
/************************************************************************************************************************/
/*   Timer V Interrupt                                                                                                  */
/************************************************************************************************************************/
void tvint ( void )
{
     if(CMFA == 1){
          CMFA = 0;                                          /* Clear CMFA                          */
          endf = 1;                                          /* Set endf                            */
          CMIEA = 0;                                         /* CMFA Interrupt Disable              */
     }
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x002C
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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