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H8/300L SLP Series

Using Interval Timing to Increment an 8-Bit "Counter" in RAM

Introduction

Using an interval function of Timer A, the 8-bit counter set in RAM is counted up. The counter starts from the initial value of H'00. After count value reaches H'FF, the counter is initialized to H'00 and resumes counting up.

Target Device

H8/38024

Contents

1. Specifications 2
2. Description of Functions 2
3. Principle of Operation 4
4. Description of Software 5
5. Flowchart 6
6. Program Listing 7

1. Specifications

1. Using an interval function of Timer A, the 8-bit counter set in RAM is counted up.
2. A Timer A interrupt is generated by overflow of Timer Counter A (TCA). The counter set in RAM is counted up or initialized during Timer A interrupt handling.
3. The counter to be set in RAM is an 8-bit counter. The counter starts from the initial value of H'00. After count value reaches H'FF, the counter is initialized to H'00 and resumes counting up.
4. Set Timer A to generate interrupts every 104.858 ms.

2. Description of Functions

1. Using the Timer A interval function, the 8-bit counter is counted up in this task example. Figure 1.1 shows the block diagram of the Timer A interval function. The block diagram of the Timer A interval function is described below.
   - The system clock (ϕ) is a 5 MHz clock and is a reference clock to operate the CPU and its peripheral functions.
   - PSS is a 13-bit counter using ϕ as its input clock. This is counted up for every cycle.
   - Timer Mode Register A (TMA) is an 8-bit read/write register and selects the prescaler and input clock. In this task example, PSS is selected for the prescaler and ϕ/2048 is selected for the prescaler divider ratio.
   - Timer Counter A (TCA) is an 8-bit read-only up counter and is counted up by an internal clock input. When TCA overflows, the Timer A overflow interrupt request flag (IRRTA) in Interrupt Request Register 1 (IRR1) is set to 1.
   - Overflowing of TCA will set the Timer A overflow interrupt request flag (IRRTA) to 1. A Timer A interrupt is accepted and Timer A interrupt handling starts if IRRTA is set to 1, Timer A interrupt enable (IENTA) in Interrupt Enable Register 1 (IENR1) is 1 and the I bit in the condition code register (CCR) is cleared to 0.
   - The method to calculate the TCA overflow period in this task example is shown below.

$$\text{TCA overflow period} = \frac{1}{\text{System clock}/2048} \times 256$$
$$= 104.858 \text{ ms}$$

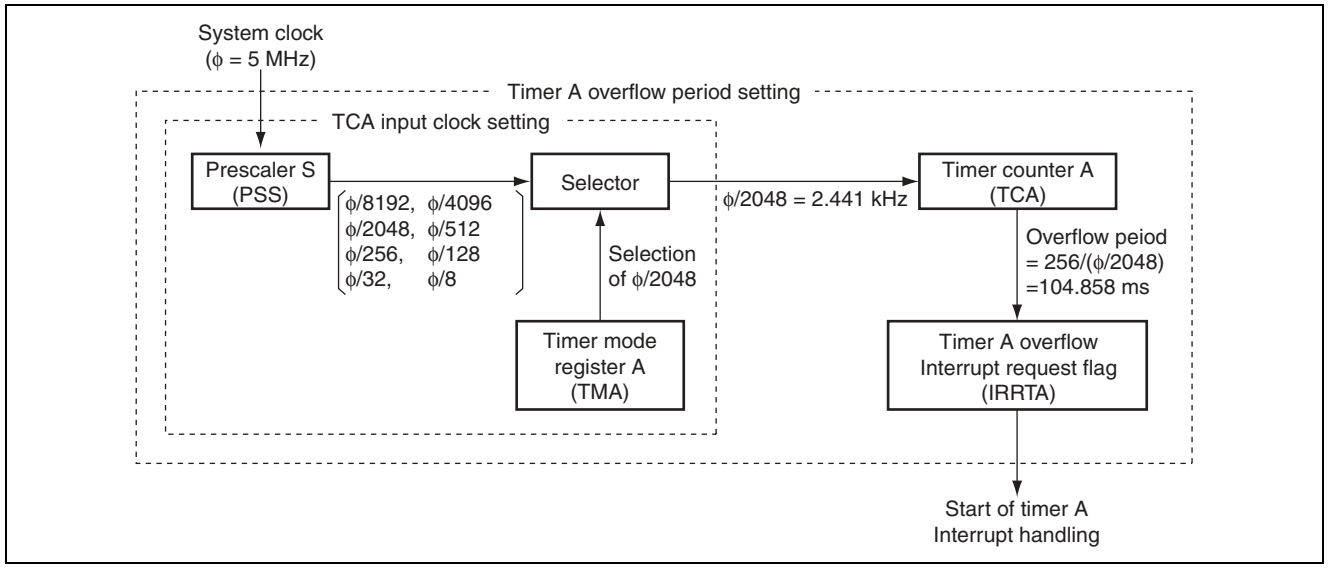


Figure 2.1 Block Diagram of Timer A Interval Function

2. Table 2.1 shows function assignment in this task example. The functions are assigned as shown in table 2.1 and the 8-bit counter is counted up by the Timer A interval function.

Table 2.1 Assignment of Functions

Function	Assignment
PSS	A 13-bit up counter using the system clock (5 MHz) as an input signal.
IENTA	Enables Timer A interrupt request.
IRRTA	Indicates whether or not a Timer A interrupt request is issued.
TMA	Selects PSS and sets prescaler divider ratio.
TCA	An 8-bit up counter using a clock input of system clock/2048.

3. Principle of Operation

1. Figure 3.1 illustrates the principle of operation of this sample task. As shown in figure 3.1, the 8-bit counter is counted up by the Timer A interval function by means of hardware processing and software processing.

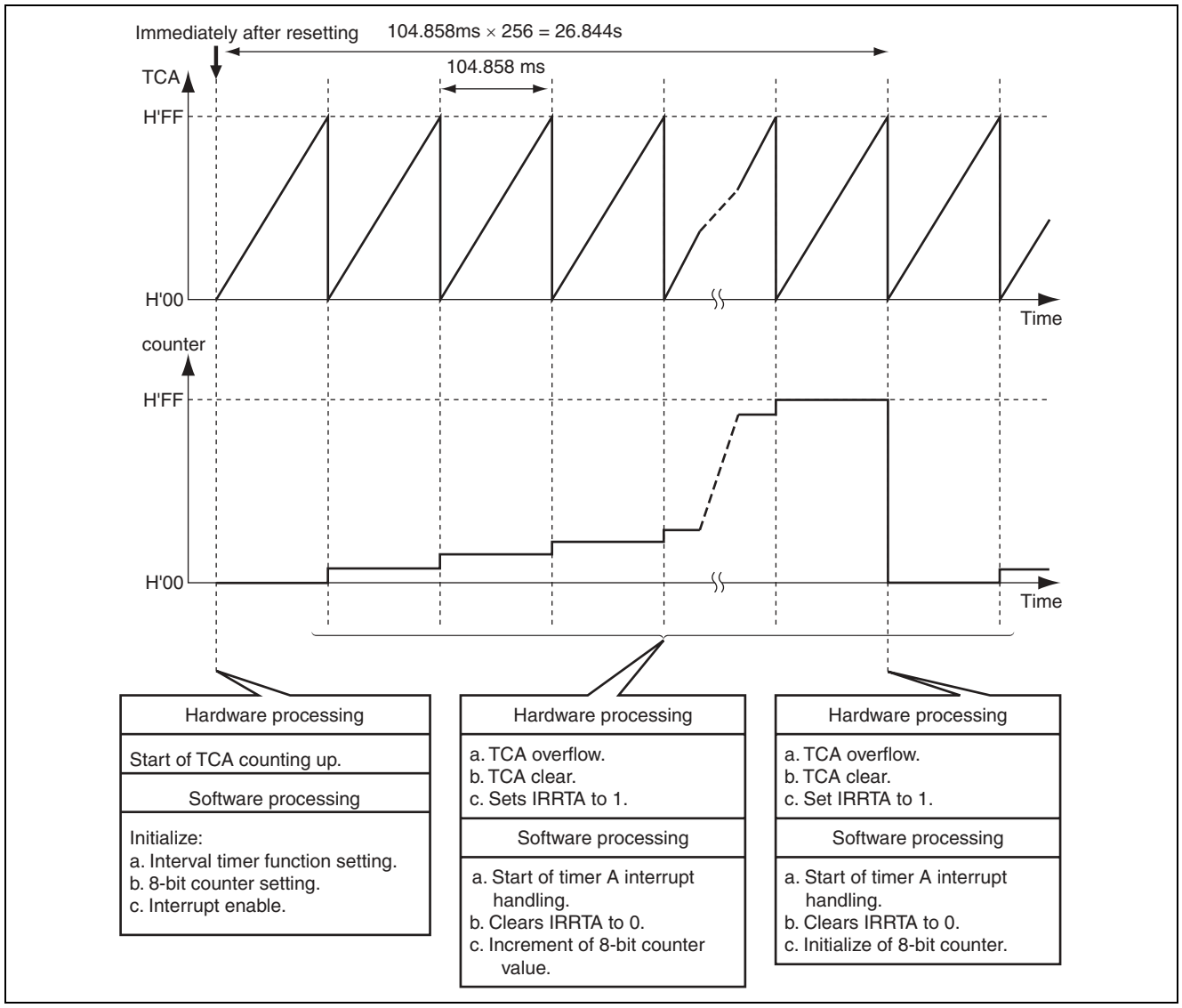


Figure 3.1 Operation Principle of Counting up the 8-bit Counter by the Timer A Interval Function

4. Description of Software

4.1 Modules

Table 4.1 describes the modules in this task example.

Table 4.1 Description of Modules

Module	Label	Function
Main Routine	main	Sets the interval timer, sets the 8-bit counter and enables interrupts.
Count Up	taint	Increments or initializes the 8-bit counter (counter) during the Timer A interrupt handling routine.

4.2 Arguments

Arguments are not used in this task example.

4.3 Internal registers

Table 4.2 describes the internal registers in this task example.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
IENR1	IENTA	Interrupt Enable Register 1 (Timer A interrupt enable) If IENTA = 0, Timer A interrupt request is disabled. If IENTA = 1, Timer A interrupt request is enabled.	H'FFF3 Bit 7	1
IRR1	IRRTA	Interrupt Request Register 1 (Timer A interrupt request flag) If IRRTA = 0, Timer A interrupt is not requested. If IRRTA = 1, Timer A interrupt is requested.	H'FFF6 Bit 7	0
TMA		Timer Mode Register A If TMA = H'12, the the timer A function is set to the interval function, TCA input clock source is set to PSS, and the prescaler divider ratio is set to 2048.	H'FFB0	H'12
TCA		Timer Counter A An 8-bit up counter using a clock input of system clock/2048.	H'FFB1	H'00

4.4 Description of RAM

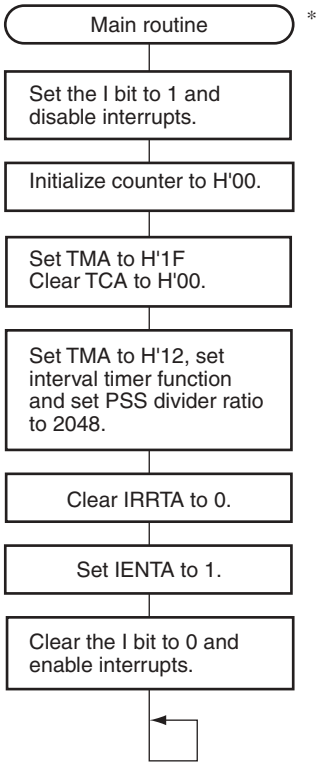
Table 4.3 shows the RAM used in this task example.

Table 4.3 Description of RAM

Label	Function	Address	Used in
counter	8-bit counter	H'FB80	Main Routine Count up

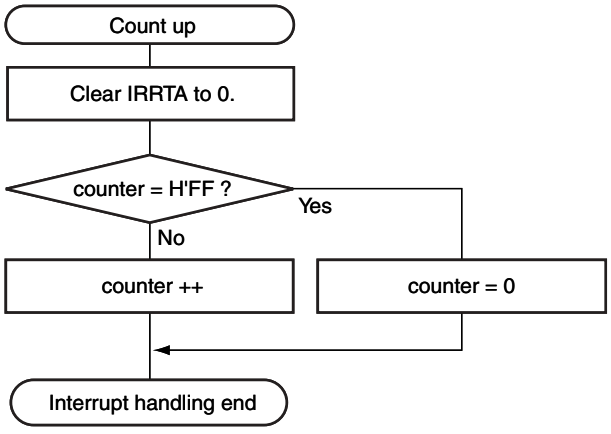
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

2. Timer A interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  '8-bit Counter Count-Up by Interval Function'                                                                       */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  :Timer A Interval Timer                                                                                             */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0         /* Timer Mode Register A                  */
#define     TCA         *(volatile unsigned char *)0xFFB1         /* Timer Counter A                        */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)                   /* Interrupt Enable Register 1            */
#define     IENTA       ENR1_BIT.b7                               /* Timer A Interrupt Enable               */
#define     IRR1_BIT    ((struct BIT *)0xFFF6)                    /* Interrupt Request Register 1           */
#define     IRRTA       IR1_BIT.b7                                /* Timer A Interrupt Request Flag         */
```

```
#pragma interrupt   (taint)
/************************************************************************************************************************/
/*  Function define                                                                                                     */
/************************************************************************************************************************/
extern void INIT ( void );                                      /* SP Set                                               */
void        main ( void );
void        taint ( void );

/************************************************************************************************************************/
/*  RAM define                                                                                                          */
/************************************************************************************************************************/
unsigned char counter;                                           /* 8bit Counter                                        */

/************************************************************************************************************************/
/*  Vector Address                                                                                                      */
/************************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                                   */
void (*const VEC_TBL1[])(void) = {                              /* 0x0000 - 0x000F                                      */
    INIT                                                        /* 0x0000 Reset Vector                                  */
};
#pragma section     V2                                          /* Vector Section Set                                   */
void (*const VEC_TBL2[])(void) = {
    taint                                                       /* 0x0016 Timer A Interrupt Vector                      */
};

#pragma section                                                 /* P                                                    */
/************************************************************************************************************************/
/*  Main Program                                                                                                        */
/************************************************************************************************************************/
void main ( void )
{

    set_imask_ccr(1);                                           /* Interrupt Disable                                    */

    counter = 0;                                                /* Initialize 8 bit  Counter                            */

    TMA = 0x1F;                                                 /* Initialize Timer Counter A                           */
    TMA = 0x12;                                                 /* Initialize Timer A Function &                        */
                                                                /*                   TCA input clock period             */

    IRRTA = 0;                                                  /* Clear IRRTA                                          */
    IENTA = 1;                                                  /* Timer A Interrupt Enable                             */

    set_imask_ccr(0);                                           /* Interrupt Enable                                     */

    while(1){
        ;
    }
}
```

```
/*****************************************************************************************************************/
/*  Timer A Interrupt                                                                                            */
/*****************************************************************************************************************/
void taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA                          */

    if(counter == 0xff){                                /* 8bit Counter = 0xff?                 */
        counter = 0;                                    /* Clear 8bit Counter                   */
    }
    else{
        counter++;                                      /* Increment 8bit Counter               */
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0016
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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