

Renesas Synergy[™] Platform

Using IAR C-STAT Static Code Analysis with R20AN0436EU0101 Rev.1.01 Selected IoT Checks from MISRA C:2012

Introduction

This application note describes how to enable and execute code analysis with the integrated IAR C-STAT solution in IAR Embedded Workbench[®] for Renesas SynergyTM.

Required Resources

A PC running Microsoft[®] Windows[®] 7 or later, with the following Renesas Synergy software installed:

- Synergy Software Platform (SSP) v1.4.0 or later
- IAR EW for Synergy[™] v8.21.1
- Synergy Standalone Configurator (SSC) v6.2.0.

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1. Creating the Blinky Project

1. Create a new workspace with IAR EW for Synergy. Select **File** > **New Workspace**.

New File	Ctrl+N
New Workspace	
Open File	Ctrl+O
Open Workspace	
Open Header/Source File	Ctrl+Shift+H
Close	Ctrl+F4
Save Workspace	
Save Workspace As	
Close Workspace	
D Save	Ctrl+S
Save As	
Save All	
b Page Setup	
Print	Ctrl+P
Recent Files	,
Recent Workspaces	
Exit	

Figure 1 Create Workspace

2. Select the **Renesas Synergy** tab and **> New Synergy Project.**

<u>File Edit View</u>	Project	<u>Renesas Synergy</u> <u>T</u> ools <u>W</u> indow	Help
D 🖻 🖬 🕼 🖉	∰ X	Configurator	
Workspace		Settings	
		New Synergy Project	
Files	22		-

Figure 2 Create a New Synergy Project



3. Set up a folder for your new **Workspace Project**. Create a **Workspace File**. Name the file .eww and save it. Example shown below, **Blinky_DKS7G2.eww**.

Organize 👻 New folder		=== -
★ Favorites Name Name Desktop Downloads Recent Places Libraries Documents Music Pictures Videos	Date modified No items match your search.	Туре
File <u>n</u> ame: Blinky_DKS7G2	m	
Save as type: Workspace Files (*.eww)		

Figure 3 Create a Workspace File, name and save it

4. Select the location in the **Renesas Synergy Settings** where the **License file** is installed and click **OK**.



Renesas Synergy Settings	×
Location where Renesas Synergy SSC/SSP is installed:	
C:\Renesas\Synergy\SSC_v6_2_0_R20180102\eclipse) 🗸 📖
License file:	
$\label{eq:c:Renesas} Synergy \\ \label{eq:c:Renesas} Synergy $	ε 🕶 📖
License information:	
Could not retrieve Renesas Synergy license information.	~
Replace encrypted files with decrypted files	
ОК	Cancel

Figure 4 Select Renesas Synergy SSC/SSP and License root directory

5. Create a **Project File**, name the Project file with .ewp and save it. Example, **Blinky_DKS7G2.ewp**.

Organize 🔻 New folder		• ==	?
★ Favorites Name Desktop Downloads Recent Places Documents Music Pictures Videos	A Date modified No items match your search.	Туре	
File <u>n</u> ame: Blinky_DKS7G2 Save as <u>type</u> : Workspace Files (*.eww)	III Save	Can	cel

Figure 5 Create project file, name and save it



6. After you save it, IAR EW for Synergy will automatically use the SSC (Synergy Standalone Configurator) to create your new project. You must select the **SSP version**, **Board** and **Device**. Click **Next** when you are done with selection.

A package view is not available for the active editor.	Help		- 8	Package	- 8
Synergy Standalone Configurator Select the board support that you require. Device Selection SSP version: 1.4.0 Board: \$STG2 DK					
Select the board support that you require.		Synergy Standalone Configurator	-		
SSP version: 1.4.0 V Board: S7G2 DK V					
		SSP version: 1.4.0 Board: [\$7G2 DK]			

Figure 6 Select SSP, Board and Device

7. The **Synergy Standalone Configurator** window pops up. Scroll down and select **Blinky with ThreadX**[®] and click the **Finish** button.

Synergy Standalone Configurator		$ \rightarrow $	
Select the type of project you wish to create.			
Project Template Selection			
O Blinky		^	
Blinky project.			
Renesas.Synergy.1.4.0			
Image: Blinky with ThreadX			
Threaded version of Blinky project.			
Renesas.Synergy.1.4.0		~	
< Back Next > Finish	_	Cancel	_

Figure 7 Select Blinky with ThreadX



8. Double check your configuration (**SSP**, **Board and Device**) from the **BSP** tab, then click the **Generate Project Content** button on the upper right side of the window.

靀 [Synergy Pr	oject] Synergy Configura	ation 🛛		- 8	Package
Board Sup	port Package Co	nfiguration		Generate Project Content	1 2 A 9302 F
Device Selec	tion				8 P109 P108 F
SSP version:	1.4.0	~			C P111 P110
Board:	S7G2 DK	~			D VCC VSS
Device:	R7FS7G27H2A01CBD				E P610 P611 F
					F P614 P612 F
					G P813 PA15 F
					H VCL1 VSS
					³ PA07 PA06 F
					K P605 P604 F
					L P602 P601 F
					M VSS VCC
					N P102 P103 F
					P P101 P800 F
					R P100 P801 F
Summary BSP	Clocks Pins Threads	Messaging Component	nts		<
Properties	Problems			Pin Conflicts	
S7G2 DK				0 items	
			^	Description	

Figure 8 Double check the setting and Generate Project Content

9. Click the **Select All** button and click **OK** if the following window pops up.



Renesas Synergy[™] Platform Using IAR C-STAT Static Code Analysis with Selected IoT Checks from MISRA C:2012

Deselected Files - Synergy Project Confirm files for deletion:		
✓ src/blinky_thread_entry.c ✓ src/hal_entry.c ✓ src/synergy_gen/blinky_thread.c ✓ src/synergy_gen/blinky_thread.h		
 src/synergy_gen/hal_data.c src/synergy_gen/hal_data.h src/synergy_gen/main.c 		
<u>S</u> elect All	Deselect All	
	ОК	

Figure 9 Confirm files for deletion

10. After Generate Project Content and configuration, you must save your configuration with your changes. Click the **Yes** button.

[Synergy Project]] Synergy Configuration' has been modified. Save changes?	
	Yes <u>No</u> Cancel	

Figure 10 Saving your configuration



11. Build your project by selecting the **Project** tab and scroll down and choose **Make F7** to build your project. You should have 0 error and 0 warning after the build, shown in the following figure.

Blinky_DKS7G2 -1	IAR Embedded Workbench IDE - ARM 7.71.2		Blinky_DKS7G2 - IAR Embedded Workbench IDE - ARM 7.71.2
File Edit View	Project Renesas Synergy J-Link Tools Window	Help	Eile Edit View Project Benesas Synergy J-Link Iools Window Help
0 📽 🖬 🕼	Add Files	- + + + H D D P P	D 📽 🖬 🚳 🕹 🖄 🖄 🖄 🖉 🖉 🖉
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Debug	Import File List		Debug
Files	Add Project Connection		Files 2: 10
Blinky_D	Edit Configurations		Blinky_DKS7 V
- El Synergy - El Cutput	Remove		Ha @Synergy La C Output
	Create New Project		
_	Add Existing Project		
	Options Alt+F7		
_			
	Version Control System		
	Make F7		
-	Compile Ctrl+F7		
	Rebuild All		
	Clean		
	Batch build F8		
	C-STAT Static Analysis		
	Stop Build Ctrl+Break		
Blinky_DKS7G2	Download and Debug Ctrl+D		Birky_DK\$762
Log	Debug without Downloading		× Messages
Mon Jun 21	Attach to Running Target	emproc.dll)	r_mic
100000000000000000000000000000000000000	Make & Restart Debugger Ctrl+R		r_ioport.c
	Restart Debugger Ctrl+Shift+R		startup_S7G2.c system_S7G2.c
	Download +		Linking
	SFR Setup		Total number of errors: 0
	Open Device Description File		Total number of warnings: 0
	Save List of Registers		DebugLog Build
	ect (build files as needed)		Ready

Figure 11 Building your project



2. Analyzing the Project with IAR C-STAT

- Right click on the project name and select Project > Options > Static Analysis. In the new version of IAR v8.21.1 or above, the cstat IoT setting will be applied when the new project is created or when you click on the Factor Setting button as shown in the following figure.
- From Category of Options for node Blinky_DKS7G2 scroll down and select Static Analysis. Click on Select C-STAT Checks and make sure that the MISRAC2012 check box is enabled with the selected IoT checks. Confirm with OK.

File Edit View Pr	R Embedded Workbench IDE - AR oject Renesas Synergy J-Link		Options for node "Blinky_D	KS7G2"		×		
C 😂 🖬 🚭 Vorkspace Debug	Add Files Add Group Import File List							
Files Binky_DI	Add Project Connection Edit Configurations		Category: General Options	1	Facto	ory Settings		
La Output	Remove Create New Project Add Existing Project		Static Analysis Runtime Checking C/C++ Compiler Assembler	C-STAT Static Analysis Extra Options				
	Options	Alt+F7	Output Converter	Select C-STAT Checks	C-STAT checks Search:		· · · · · · · · · · · · · · · · · · ·	
	Version Control System	,	Custom Build		Name			
	Make Compile Rebuild All Clean Batch build	F7 Ctrl+F7 F8	Build Actions Linker Debugger Simulator CMSIS DAP	Import Settings	STDCHECKS CERT SECURITY MISRAC2004	Severity Used None None None	Checks based on the C Checks based on the C Checks based on the N	
	C-STAT Static Analysis	,	I-jet/JTAGjet J-Link/J-Trace	Enable parallel analysis:	MISRAC2012 MISRAC++2008	90/22 None		
	Stop Build	Ctrl+Break		Enable module timeout:				
Binky_DKS762 Messages r_fmi.c r_ioport.c startup_S7 system_S1 Linking	Download and Debug Debug without Downloading Attach to Running Target Make & Restart Debugger Restart Debugger Download	Ctrl+D Ctrl+R Ctrl+Shift+R		 Enable false-positives analysis Limit messages per check and 	٠		OK Cancel	
Total num Total num Debug Log Buik t options for the sele	SFR Setup Open Device Description File Save List of Registers	۲			ОК	Cancel		

Figure 11 Selecting MISRA C:2012

3. Start the static code analysis over the complete project from **Project** > **C-STAT Static Analysis** > **Analyze Project** or use the shortcut key **Shift+F7** in the following figure.



Image: Section 2000 Add Files Add Group Image: File List Add Files Add Group Image: File List Add Files Add Files Add Files BillinkyD Edit Configurations Remove Create New Project Options Alt+F7 Version Control System > Make F7 Compile Curl-F7 Rebuild All Clean Bathy.DN3702 Step Build Curl-Break Messager Crist New Project Analyze Project Import File List F8 Make Curl-F7 Rebuild All Clean Bathy.DN3702 Step Build Curl-Break Devolge without Downloading Target Curl-Shift-F7 Add Ste Restart Debugger Curl-Shift-F8 Bilking Step Build Curl-Shift-R Totiol num SfR Setup Open Device Description File Totiol num SfR Setup Open Device Description File		R Embedded Workbench IDE - ARM 7.		ela.				
C-STAT Static Analysis Analyze Project Shift+F7 Binky_DKS762 Stop Build Ctrl+Break. Analyze File(s) Ctrl+Shift+F7 Messages Debug without Downloading Ctrl+D Generate HTML Summary Messages Attach to Running Target Generate HTML Report File Make & Restart Debugger Ctrl+R Restart Debugger Ctrl+R Make & Restart Debugger Ctrl+Shift+R Download File Total num SfR Setup Open Device Description File H	Crispace Debug Files Crispace Debug Files Crispace Debug Files Crispace	Add Files Add Group Import File List Add Project Connection Edit Configurations Remove Create New Project Add Existing Project Options Version Control System Make Compile Rebuild All	Alt+ F7 ,			Di 👫 💥 🔎 🌛 🕹	>	
Stop Build Ctrl+Break Analyze File(s) Ctrl+Shift+F7 Debug without Downloading Ctrl+D Generate HTML Summary Debug without Downloading Generate HTML Summary Make & Restart Debugger Ctrl+R Restart Debugger Ctrl+Shift+R Download Ctrl+Shift+R System_SS SfR Setup Total num SfR Setup Open Device Description File				Analyze Project	Shift+F7	1		
Total numi Open Device Description File	Messages r_fmi.c r_ioport.c startup_S7 system_S1 Linking	Stop Build Download and Debug Debug without Downloading Attach to Running Target Make & Restart Debugger Restart Debugger Download	Ctrl+D Ctrl+R Ctrl+Shift+R	Analyze File(s) Clear Analysis Results Generate HTML Summary			File	Line
Ebdg Log Dunk Save List of Registers		Open Device Description File Save List of Registers	,					

Figure 12 Analyzing project

4. Additionally, it is possible to analyze specific files or a group of files by right clicking on the file or group and using the option **C-STAT Static Analysis > Analyze File(s)**.

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orkspace	×			•
Debug	•			
Files	#a BB			
Blinky_DKS7G2 - Deb	oug 🗸			
🕫 🤀 Synergy				
	Open Renesas Synergy Configurator			
E synergy	Renesas Synergy Settings			
	Options			
Blinky_DKS7G2.	Make			
a _ onny_ororde.	Compile			
	Rebuild All			
	Clean			
	C-STAT Static Analysis	Analyze Project		
		Analyze File(s)		
	Stop Build	Clear Analysis Results		
	Add	Generate HTML Summary		
	Remove	Generate Full HTML Report		
	Rename	Generate Pull PTML Report		
Blinky_DKS7G2	Version Control System			
Messages			File	Line
r_fmi.c	Open Containing Folder			
r_ioport.c startup_S7G2.c	File Properties			
system_S7G2.c	Set as Active			
Linking				
Total number of errors: 0				
Total number of warnings				
Debug Log Build				





3. Using the Report

1. After 3-4 minutes, depending on the complexity of your project, you should have the static analysis completed and the warnings will be available in the C-STAT messages window. Notice the check names, file details and severity in the warnings.

	Window Help			
) 🖆 🖬 🕼 👗 🗞 🛍 💼 🗠 ભ	- < > > > > > > > > > > > > > > > > > >	🗈 🐨 🏠 🔯 💖 🗩	A A	
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100				
a <mark>Blinky_DKS7 ✓</mark> —⊞ ∰ Synergy				
-B Output				
Blinky_DK				
Blinky_DK				
linky DKS762				
Messages			File	Line
Analyzing startup_S7G2.c				
startup_S7G2.c: 28 messages				
system_S7G2.c:				
Analyzing system S7G2 c				
Analyzing system_S7G2.c system_S7G2.c: 37 messages				
system_S7G2.c: 37 messages				
system_S7G2.c: 37 messages Link analysis: 116 messages				
system_S7.32.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s)				
system_S7G2.c. 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s)				
system_S7G2.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s) DebugLog Build	Messages: 1765			
system_\$762.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s) Debug Log_Build Severity: All Fiter:	Messages: 1765 Check	Sevenity	File	Line
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system_\$7G2.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s) Debug Log_Buld Severity: All Filter: Message Heal D blinky_thread_c (88 messages) Heal D blinky_thread_entry.c: (84 messages)		Severity	blinky_thread.c blinky_thread_entry.c	Line
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system_\$7\$2.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s) Debug Log Buld Severity: All Fiter: Message Binky_thread_c (88 messages) Binky_thread_enty.c: (84 messages) Binky_thread_enty.c: (54 messages) Binky_thread_colocks.c: (55 messages) Binky_clocks.c: (55 messages)		Severity	blinky_thread.c blinky_thread_entry.c bsp_cache.c bsp_clocks.c	Line
system_\$762.c: 37 messages Link analysis: 116 messages Analysis completed. 1765 message(s) Debug tog Build Severity: All Fiter: Message B blinky_thread_c (88 messages) B blinky_thread_entry.c (84 messages) B blinky_thread_entry.c (84 messages) B bsp_cachec (35 messages) B bsp_clocks.c (50 messages) B bsp_common.c (27 messages)		Severity	blinky_thread.c blinky_thread_entry.c bsp_cache.c bsp_clocks.c bsp_common.c	Line
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Figure 14 C-STAT report

2. To get additional information about the checks that have been triggered and reference information on how to fix the issues, select the warning and press **F1**.



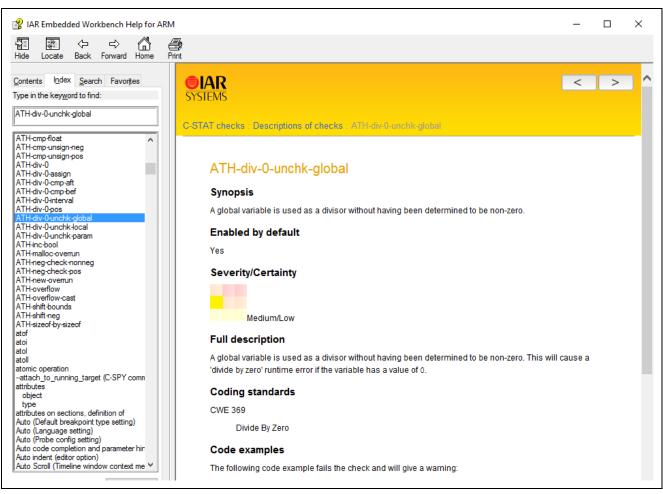


Figure 15 Warning details



Website and Support

Support: <u>https://synergygallery.renesas.com/support</u>

Technical Contact Details:

- America: <u>https://www.renesas.com/en-us/support/contact.html</u>
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Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Feb 2, 2017	-	Initial release
1.01	Feb 8, 2018	-	Updated for SSP v1.4.0

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