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H8/300H Tiny Series

Using Compare Match Function for Timer Z 0/1 Output

Introduction

Timer Z outputs 0 or 1 on a compare-match of its timer counter 0 (TCNT0).

Target Device

H8/3687

Contents

1. Specifications

1. Timer Z outputs 0 or 1 on a compare-match of its timer counter 0 (TCNT0).
2. The FTIOA pin normally outputs 1 and outputs 0 when TCNT0 matches GRA0.
3. The FTIOB pin normally outputs 0 and outputs 1 when TCNT0 matches GRB0.

2. Description of Functions

1. In this sample task, timer Z outputs 0 or 1 from its output pins on a compare-match of the timer counter 0 (TCNT0) of timer Figure 2.1 is a block diagram of timer Z. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) specifies the input clock for TCNT0 and the condition for clearing TCNT0. In this sample task, the TCNT0 is incremented at the rising edge of ϕ/2, and the TCNT0 is specified not to be cleared.
- Timer I/O control register A0 (TIORA0) controls GRA0 and GRB0. In this sample task, GRA0 and GRB0 are used as output-compare registers, the FTIOA0 pin outputs 0 on compare-match with GRA0, and the FTIOB0 outputs 1 on compare-match with GRB0.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by an internal clock or external clock input. In this sample task, TCNT0 is incremented at the rising edge of ϕ/2.
- General register A0 (GRA0) is a 16-bit readable/writable register. The value of GRA0 is always compared with that of TCNT0. In this sample task, GRA0 is set to 0x4000.
- General register B0 (GRB0) is a 16-bit readable/writable register. The value of GRB0 is always compared with that of TCNT0. In this sample task, GRB0 is set to 0x8000.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 is specified to start counting and TCNT1 is specified to stop counting.
- Timer mode register (TMDR) selects synchronous or independent operation of TCNT0 and TCNT1. In this sample task, TCNT0 operates independently of TCNT1.
- Timer PWM mode register (TPMR) sets the output pins in normal operation mode or PWM mode. In this sample task, all outputs pins are set to normal operation mode.
- Timer function control register (TFCR) specifies operation modes and selects output levels. In this sample task, normal operation is specified for channels 0 and 1.
- Timer output master enable register (TOER) enables or disables channels 0 and 1 outputs. In this sample task, the FTIOA0 and FTIOB0 outputs are enabled.
- Timer output control register (TOCR) specifies the initial value that is output until the first compare-match is generated. In this sample task, the initial values of FTIOA0 and FTIOB0 are specified as 1 and 0, respectively.
- Input-capture/output-compare A0 pin (FTIOA0) is specified as an output-compare output pin and outputs 0 when the TCNT0 matches the GRA0.
- Input-capture/output-compare B0 pin (FTIOB0) is specified as an output-compare output pin and outputs 1 when the TCNT0 matches the GRB0.

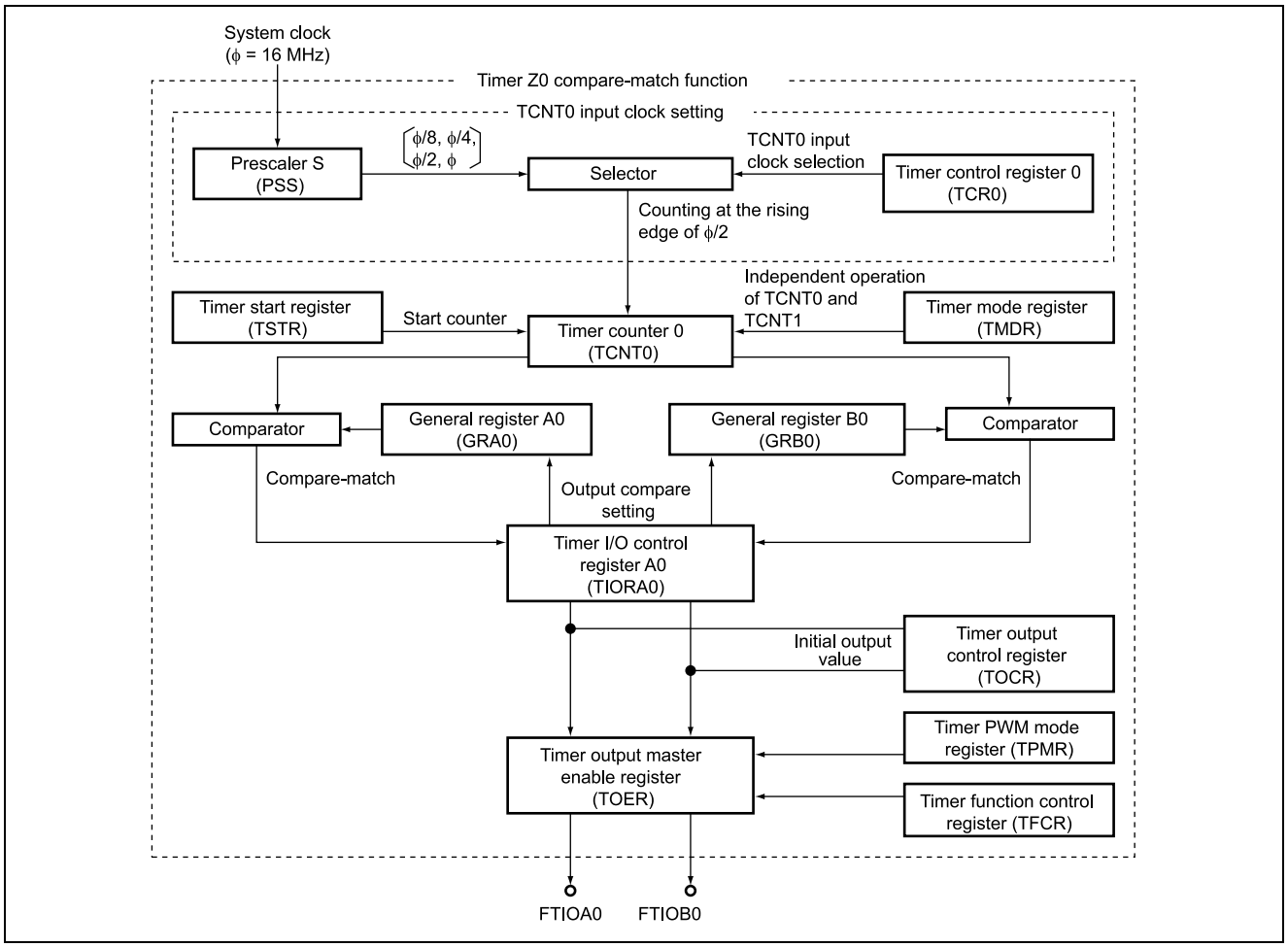


Figure 2.1 Block Diagram of Timer Z Compare-Match 0/1 Output

2. Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated so that 0 or 1 is on a compare-match of timer Z.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCR0	Specifies the TCNT0 input clock.
TIORA0	Setting for the FTIOA0 and FTIOB0 pins
TCNT0	16-bit counter
GRA0	Compared with TCNT0.
GRB0	Compared with TCNT0.
TSTR	Starts counting by TCNT0.
TMDR	Specifies TCNT0 to operate independently of TCNT1.
TPMR	Specifies all output pins for normal operation.
TOER	Enables the FTIOA0 and FTIOB0 pin outputs.
TOCR	Specifies the initial output values for the FTIOA0 and FTIOB0 pins.
FTIOA0 pin	Outputs 0 on a compare-match with GRA0.
FTIOB0 pin	Outputs 1 on a compare-match with GRB0.

3. Description of Operation

Operation of this sample task is described in figure 3.1. Hardware and software processing are applied in the way shown in figure 3.1 to output 0 or 1 on a compare-match of timer Z.

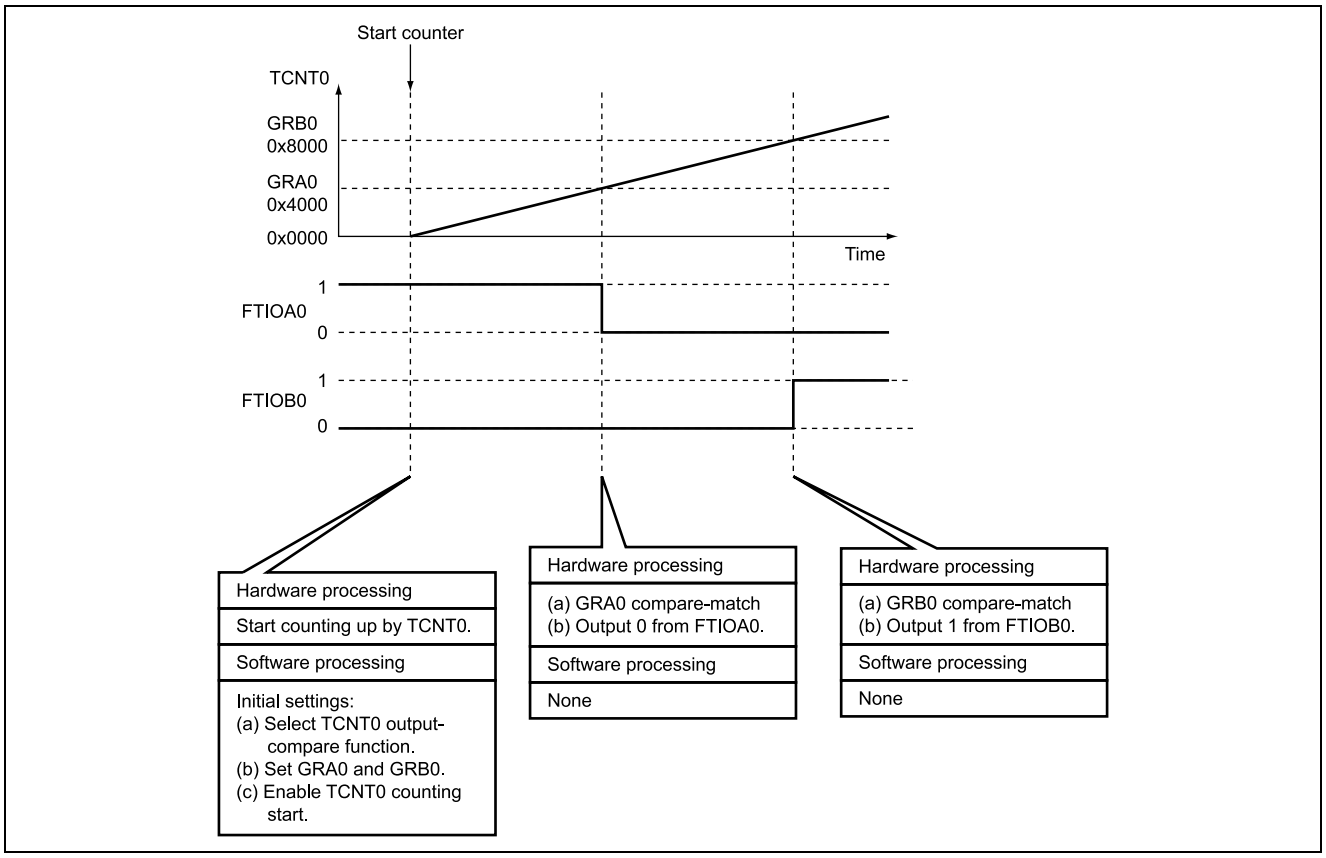


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of Module

Module Name	Label Name	Function
Main routine	main	Sets the timer Z compare-match function, starts the counter, and sets output pins.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = 0	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = x, CCLR1 = 0, CCLR0 = 0: Disables clearing of TCNT0
5	CCLR0	CCLR0 = 0	(x: Don't care)
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts on the rising edge of the clock
2	TPSC2	TPSC2 = 0	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 0	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts by ϕ/2
0	TPSC0	TPSC0 = 1	

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
6	IOB2	IOB2 = 0	I/O control B2 to B0
5	IOB1	IOB1 = 1	IOB2 = 0, IOB1 = 1, IOB0 = 0:
4	IOB0	IOB0 = 0	Specifies the GRB0 as an output-compare register and the FTIOB0 pin to output 1 on a compare-match with GRB0.
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 0, IOA1 = 0, IOA0 = 1:
0	IOA0	IOA0 = 1	Specifies the GRA0 as an output-compare register and the FTIOA0 pin to output 0 on a compare-match with GRA0.

- TCNT0 Timer counter 0 Address: 0xF706
  Function: A 16-bit up-counter that is incremented at the rising edge of ϕ/2.
  Setting: 0x0000

- GRA0 General register A0 Address: 0xF708
  Function: A compare-match is generated if the GRA0 value matches TCNT0 counter value.
  Setting: 0x04000

- GRB0 General register B0 Address: 0xF70A
  Function: A compare-match is generated if the GRB0 value matches TCNT0 counter value.
  Setting: 0x08000

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0.

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TPMR Timer PWM mode register Address: 0xF722

Bit	Bit Name	Setting	Function
0	PWMB0	0	PWM mode B0 PWMB0 = 0: The FTIOB0 pin operates in normal operation mode. PWMB0 = 1: The FTIOB0 pin operates in PWM mode.

- TFCR Timer function control register Address: 0xF723

Bit	Bit Name	Setting	Function
1	CMD1	CMD1 = 0	Combination mode 1 to 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMDk0 = 0: Channels 0 and 1 operates in normal operation mode.

- TOER Timer output master enable register Address: 0xF724

Bit	Bit Name	Setting	Function
1	EB0	0	Master enable B0 EB0 = 0: Enables the FTIOB0 pin output. EB0 = 1: Disables the FTIOB0 pin output.
0	EA0	0	Master enable A0 EA0 = 0: Enables the FTIOA0 pin output. EA0 = 1: Disables the FTIOA0 pin output.

- TOCR Timer output control register Address: 0xF725

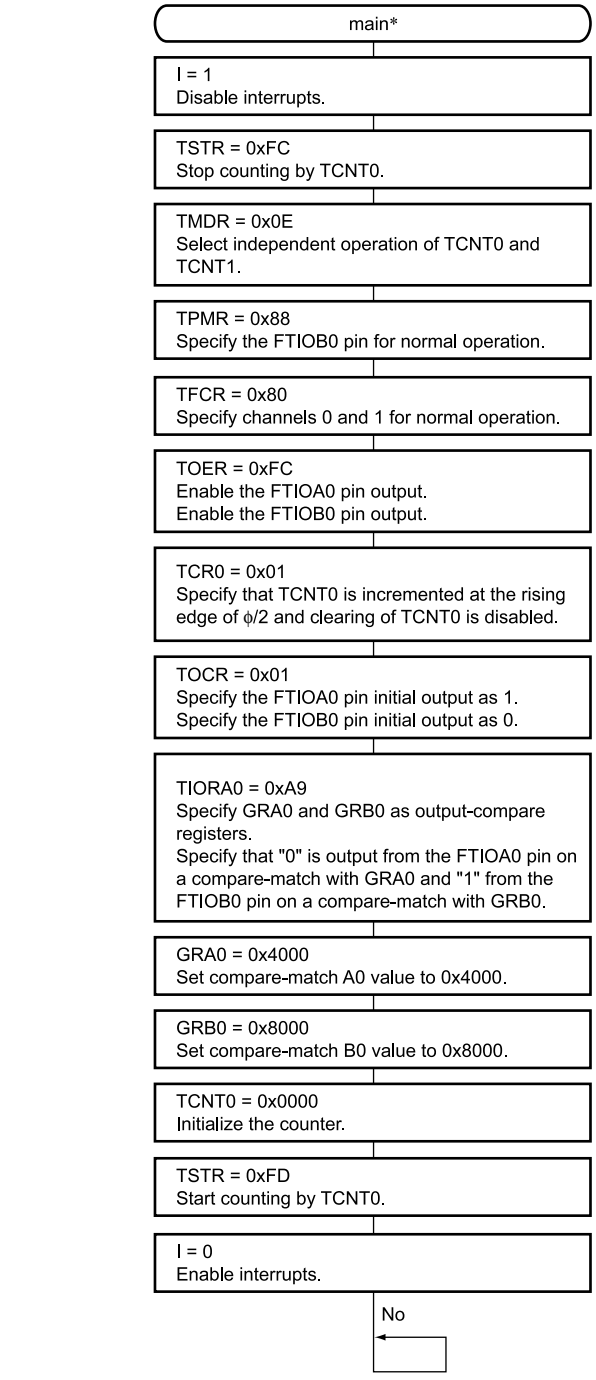
Bit	Bit Name	Setting	Function
1	TOB0	1	Output level select B0 TOB0 = 0: Specifies the initial output value on the FTIOB0 pin as 0. TOB0 = 1: Specifies the initial output value on the FTIOB0 pin as 1.
0	TOA0	0	Output level select A0 TOA0 = 0: Specifies the initial output value on the FTIOA0 pin as 0. TOA0 = 1: Specifies the initial output value on the FTIOA0 pin as 1.

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

6. Program List

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/      Application Note                                                                                                  */
/*                                                                                                                      */
/*   'Output 0 and 1 by output compare function'                                                                        */
/*                                                                                                                      */
/*   Function                                                                                                           */
/    : Timer Z output compare function                                                                                   */
/*                                                                                                                      */
/    External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0               */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0         */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                        */
#define        GRA0           *(volatile unsigned short *)0xF708                 /* General register A_0                   */
#define        GRB0           *(volatile unsigned short *)0xF70A                 /* General register B_0                   */
#define        TCR1           *(volatile unsigned char *)0xF710                  /* Timer control register_1               */
#define        TIORA1         *(volatile unsigned char *)0xF711                  /* Timer I/O Control Register A_1         */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                   */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                    */
#define        TPMR           *(volatile unsigned char *)0xF722                  /* Timer PWM mode register                */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register        */
#define        TOER           *(volatile unsigned char *)0xF724                  /* Timer output master enable register    */
#define        TOCR           *(volatile unsigned char *)0xF725                  /* Timer output control register          */

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                      /* SP Set                                 */
void main ( void );
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                       */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                              */
     INIT                                                               /* 00 Reset                                 */
};

#pragma section                                                         /* P                                        */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     set_imask_ccr(1);                                                  /* Interrupt Disable                        */

     TSTR = 0xFC;                                                       /* TCNT0 count stop                         */
     TMDR = 0x0E;                                                       /* TCNT0,TCNT1 Single Mode                  */
     TPMR = 0x88;                                                       /* FTIOB0 is Normal Mode                    */
     TFCR = 0x80;                                                       /* Chanel 0,1 is Normal Mode                */
     TOER = 0xFC;                                                       /* FTIOA0,FTIOB0 Output Enable              */
     TCR0 = 0x01;                                                       /* Rising edge, phi/2 Clock count           */
     TOCR = 0x01;                                                       /* First level set FTIOA0:1 FTIOB0:0        */
     TIORA0 = 0xA9;                                                     /* 0 output by GRA compare match            */
                                                                        /* 1 output by GRB compare match            */
     GRA0 = 0x4000;                                                     /* Set GRA0                                 */
     GRB0 = 0x8000;                                                     /* Set GRB0                                 */
     TCNT0 = 0x0000;                                                    /* Set TCNT0                                */
     TSTR = 0xFD;                                                       /* TCNT0 count start                        */

     set_imask_ccr(0);                                                  /* Interrupt Enable                         */
     while(1);
}
```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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