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SH7262/SH7264 Group

USB Isochronous Transfer by the USB Function Controller

Summary

This application note describes the configuration to use the SH7262/SH7264 USB 2.0 host/function module as the USB function controller and transfer data to the USB host in isochronous transfer.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

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1. Introduction

1.1 Specifications

Specifies the SH7264 MCU as the USB function to transfer data to the USB host in isochronous transfer.

1.2 Modules Used

- USB 2.0 Host/Function Module (USB module)
- Direct Memory Access Controller (DMAC)
- Interrupt controller (INTC)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Note

For more information, refer to the following application notes:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Implementing the USB Enumeration on the USB Function Controller
- SH7262/SH7264 Group USB Bulk Transfer by the USB Function Controller
- SH7262/SH7264 Group USB Interrupt Transfer by the USB Function Controller

2. Applications

This application uses the USB 2.0 host/function module (USB module) as the USB function to transfer data to the USB host in isochronous transfer.

2.1 Overview of USB Module

(1) Includes the USB host controller and function controller compliant to USB high-speed
- Includes the USB host controller and function controller
- USB host controller and function controller can be switched by setting registers
- Includes the USB transceiver

(2) Reduced number of external pins and space-saving installation
- Includes the D+ pull-up resistor (When operating as the function)
- Includes the D+ and D− pull-down resistors (When operating as the host)
- Includes the D+ and D− terminator (When operating at high-speed)
- Includes the D+ and D− output resistor (When operating at full-speed)

(3) Supports all types of USB transfer
- Control transfer
- Bulk transfer
- Interrupt transfer (High-bandwidth is not supported)
- Isochronous transfer (High-bandwidth is not supported)

(4) Internal bus interface
- Includes two channels of DMA interface

(5) Pipe configuration
- Includes 8-KB buffer memory for USB communication
- Up to 10 pipes can be specified (including the default control pipe)
- Programmable pipe configuration
- Any endpoint number can be assigned to pipes 1 to 9
- Transfer conditions for pipes are as follows:
  - Pipe 0: Control pipe (Default control pipe: DCP), 64-byte fixed single buffer
  - Pipes 1 and 2: Bulk or isochronous pipe, continuous transfer mode, programmable buffer size (Double buffering can be specified up to 2 KB)
  - Pipes 3 to 5: Bulk pipe, continuous transfer mode, programmable buffer size (Double buffering can be specified up to 2 KB)
  - Pipes 6 to 9: Interrupt pipe, 64-byte fixed single buffer

(6) Features as the host controller
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) supported
- Communicates with multiple peripherals via a hub (tier 1)
- Automatically responds to the reset handshake
- Automatically schedules to transmit SOF, and packets
- Specifies the interval on isochronous and interrupt transfers

(7) Features as the function controller
- High-speed (480 Mbps), and full-speed (12 Mbps) supported
- Automatically detects the high-speed or full-speed operation by replying to the reset handshake
- Manages stage on control transfer
- Manages the device state
- Automatically responds to the SET_ADDRESS request
- NAK response interrupt (NRDY)
- SOF Tracking and Recovery

(8) Other features
- Completes transfer by counting transactions
- Delays the BRDY interrupt event notification timing (BFRE)
- Automatically clears the buffer memory after reading data from the pipe specified by the DnFIFO (n = 0, 1) port (DCLRM)
- Specifies NAK to the response PID by the end of transfer (SHTNAK)

2.2 Isochronous Transfer

Isochronous transfer is used to transfer large amounts of data periodically. It is useful for transferring data with bounded-latency, however, does not detect and correct an error. Isochronous transfer is popularly used for transferring audio and video.

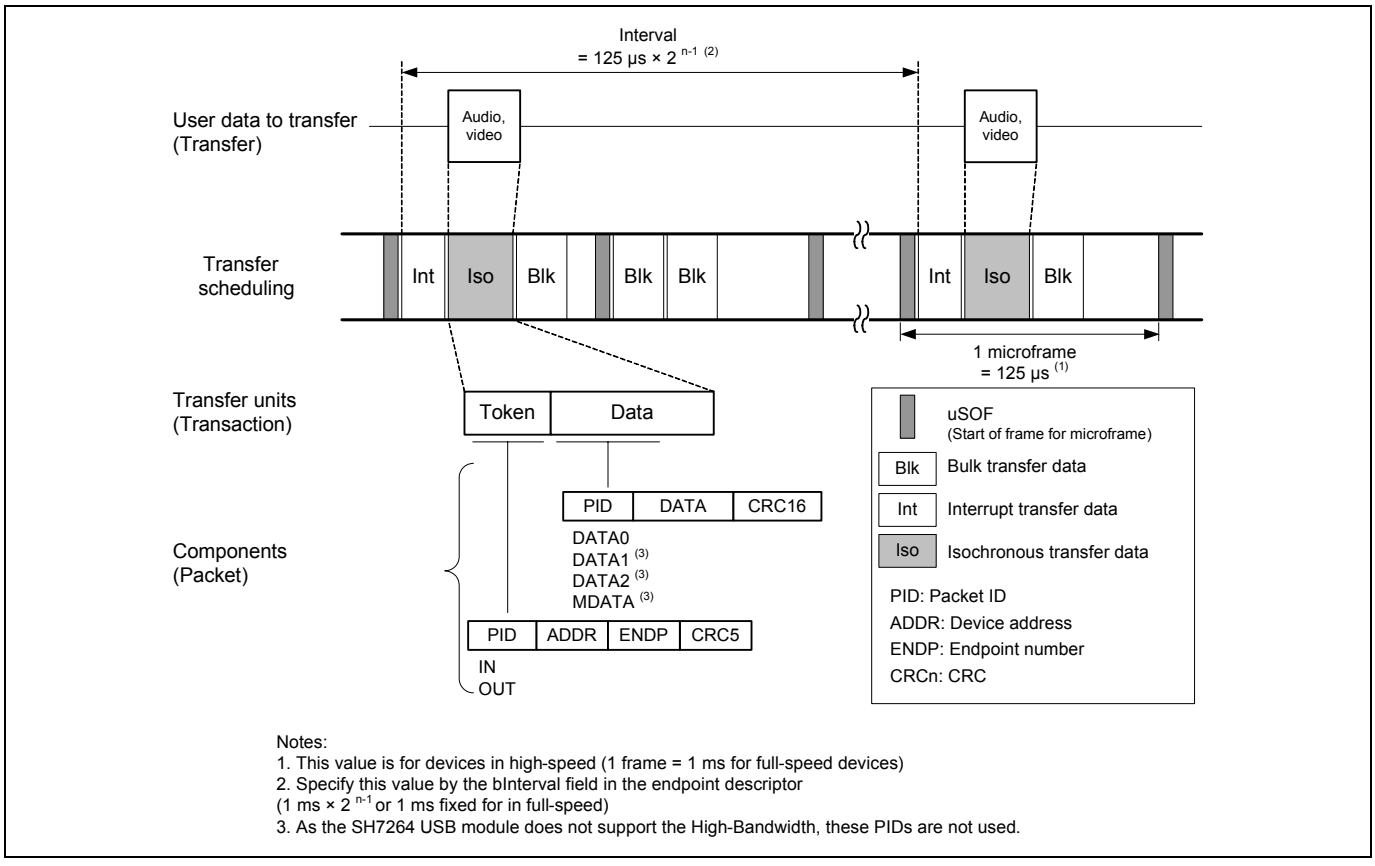
Isochronous transfer includes the following features:

- Periodic transfer
- Unidirectional (Isochronous IN transfer or isochronous OUT transfer)
- Consists of two packets such as the token, and data
- Maximum packet size: 1 to 1024 bytes (for high-speed endpoints)
  1 to 1023 bytes (for full-speed endpoints)

As the periodic transfer is preferentially executed when scheduling (micro) frames, its latency is guaranteed. However, the number of transactions per (micro) frame is restricted to 1 (see note). Isochronous transfer does not detect and correct an error, since it does not allow the handshake.

Note: High-Bandwidth endpoint supports up to three transactions, however, the SH7264 USB module does not support the High-Bandwidth.

Figure 1 shows the isochronous transfer image.



Notes:
1. This value is for devices in high-speed (1 frame = 1 ms for full-speed devices)
2. Specify this value by the bInterval field in the endpoint descriptor
(1 ms × 2 n-1 or 1 ms fixed for in full-speed)
3. As the SH7264 USB module does not support the High-Bandwidth, these PIDs are not used.

Figure 1 Isochronous Transfer Image

Figure 2 shows the packet response pattern for isochronous IN transfer. Figure 3 shows the packet response pattern for isochronous OUT transfer.

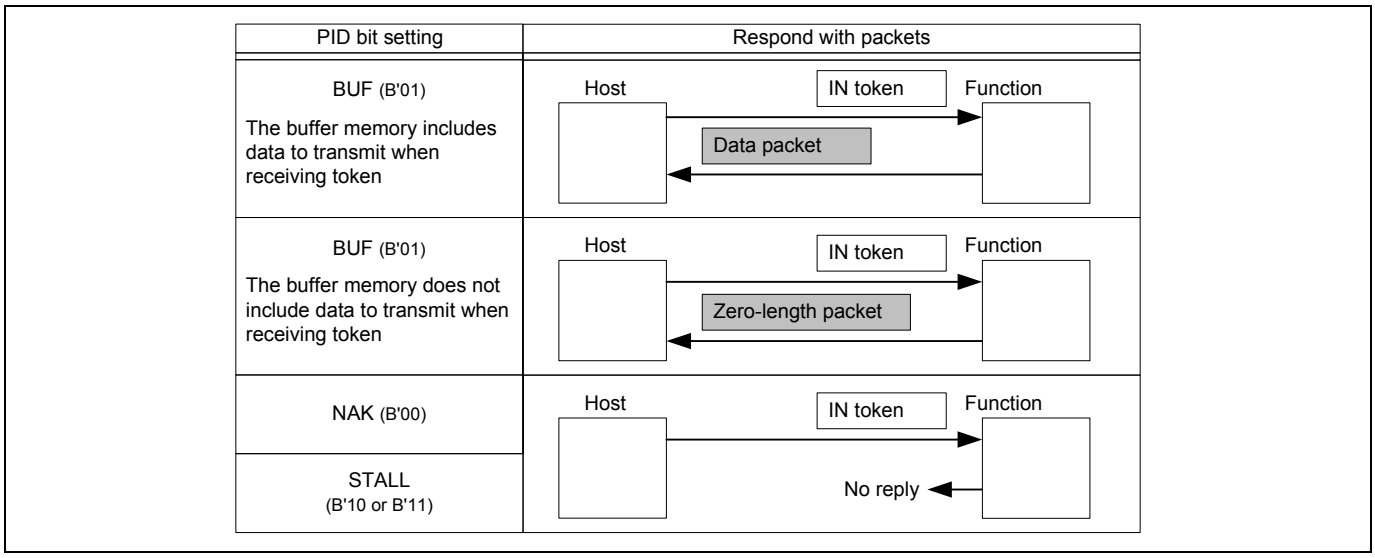


Figure 2 Packet Response Pattern for Isochronous IN Transfer

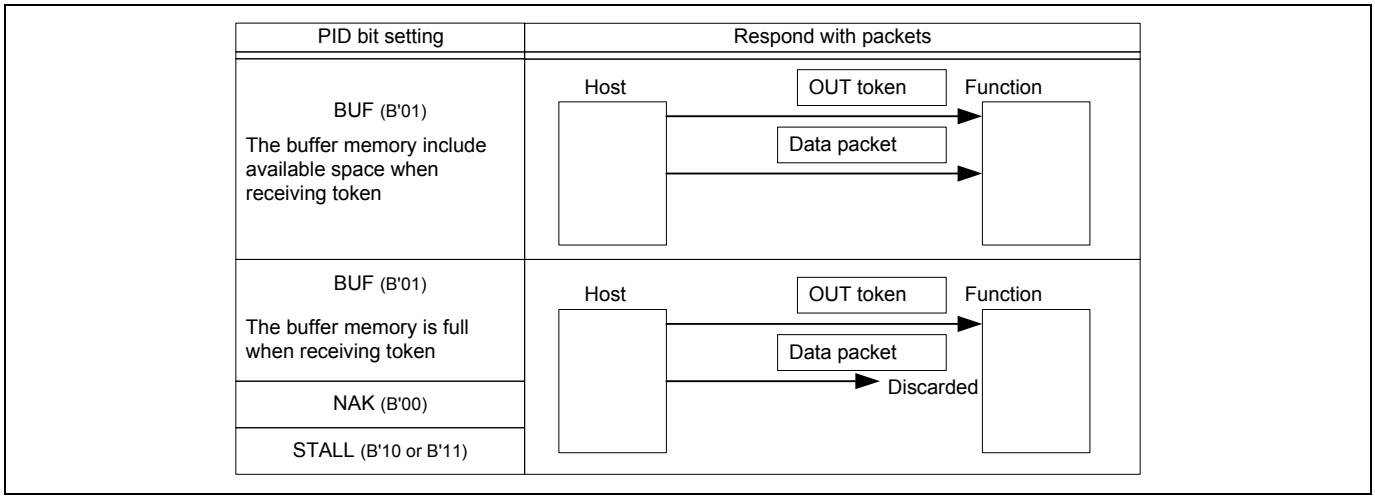


Figure 3 Packet Response Pattern for Isochronous OUT Transfer

Figure 4 shows isochronous transfer setting procedures (overview).

For more information on how to initialize the pipe, refer to 2.3 Pipes. Refer to 2.4 FIFO Port for how to access FIFO port.

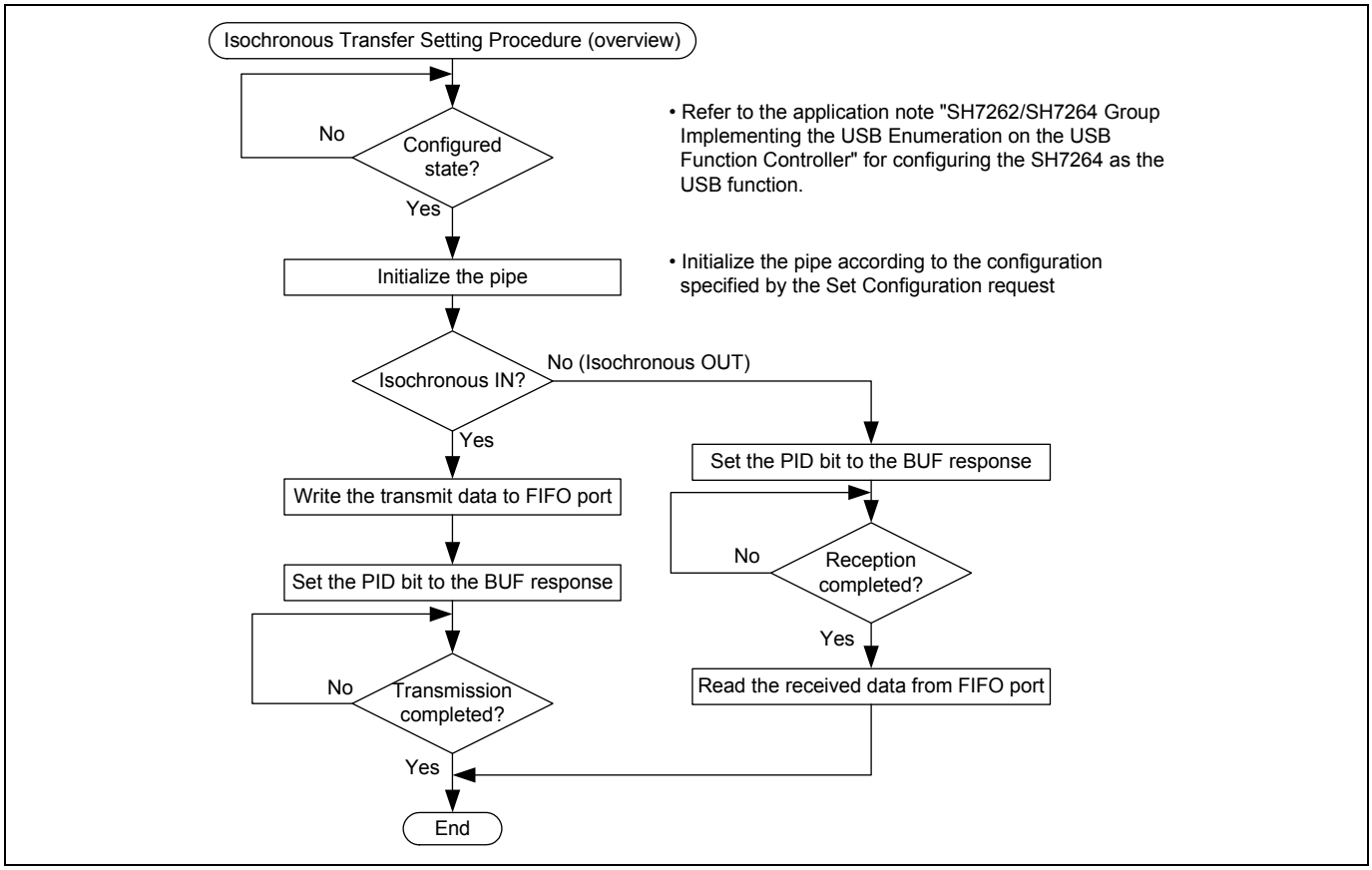


Figure 4 Isochronous Transfer Setting Procedure (Overview)

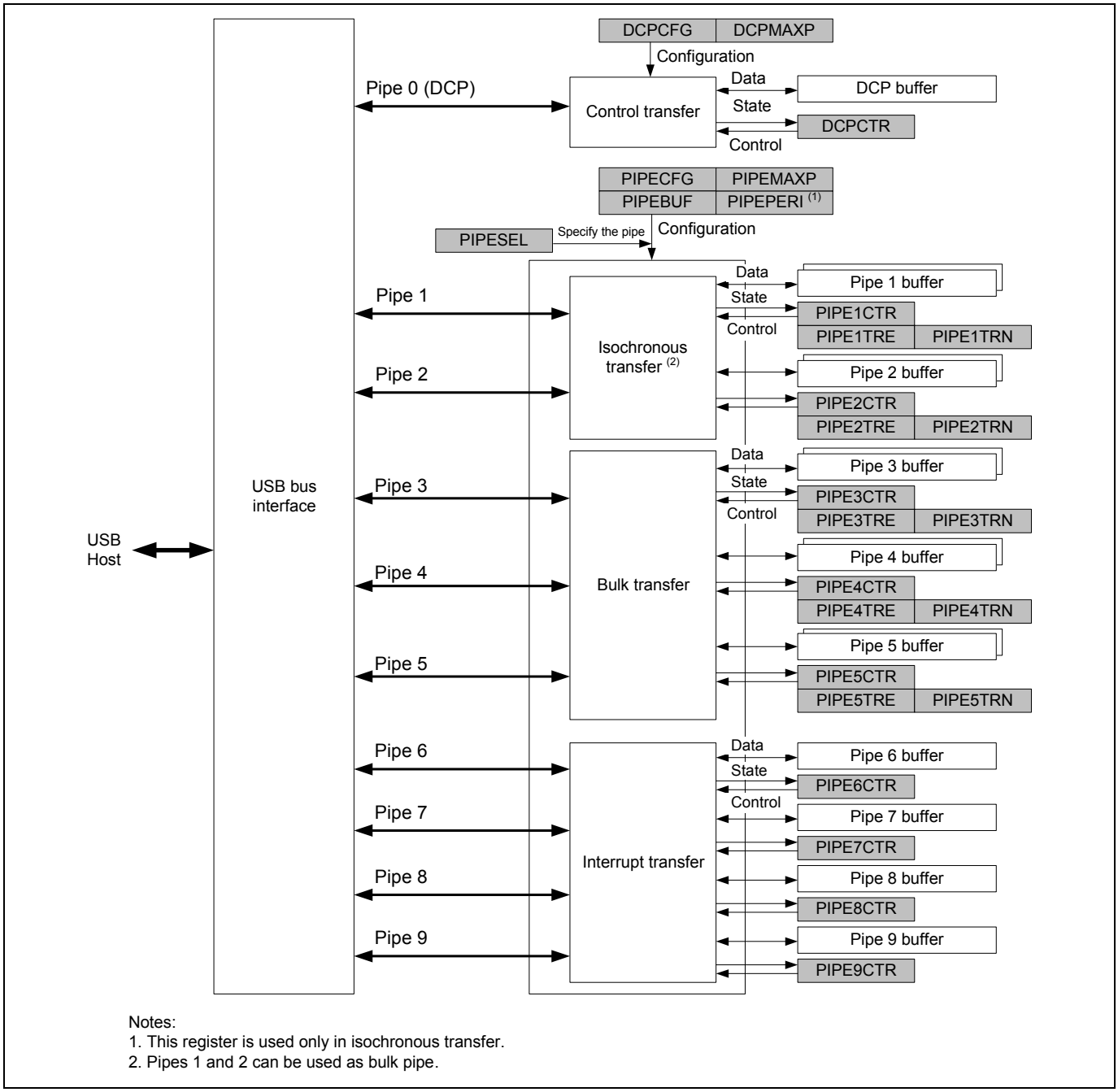
2.3 Pipes

A USB pipe is a logic communication path in the USB transfer. Specify the transfer type and direction on every pipe to execute multiple USB transfers on a device.

2.3.1 Overview

Figure 5 shows an overview of the pipe.

A USB module uses 10 pipes including the default control pipe (DCP). Pipe 0 (DCP) supports control transfer only. Refer to the "SH7262/SH7264 Group Implementing the USB Enumeration on the USB Function Controller" for details on the DCP. Pipes 1 and 2 are for isochronous transfer, pipes 3 to 5 are for bulk transfer, and pipe 6 to 9 are for interrupt transfer. Note that pipes 1 and 2 can be used for bulk transfer. Pipes 1 to 5 are allowed for using the double buffering and transaction counter to transfer large amount of data. For setting pipes 1 to 9, see 2.3.2 Pipe Configuration Procedure.



Notes:
1. This register is used only in isochronous transfer.
2. Pipes 1 and 2 can be used as bulk pipe.

Figure 5 Pipes (Overview)

2.3.2 Pipe Configuration Procedure

Figure 6 shows the configuration procedure of pipes. For details on the pipe setting, refer to 2.3.3 Transmit Pipe Setting (Isochronous IN Transfer) and 2.3.4 Receive Pipe Setting (Isochronous OUT Transfer).

Pipes can be set dynamically. Normally, pipes are set when the target endpoint is decided. As pipes 1 to 9 use some of registers in common, set the target pipe by the Pipe window select register (PIPESEL) before configuration. Note that pipes cannot be configured when the target pipe is already allocated to the FIFO port, or when the PID bit setting is other than NAK.

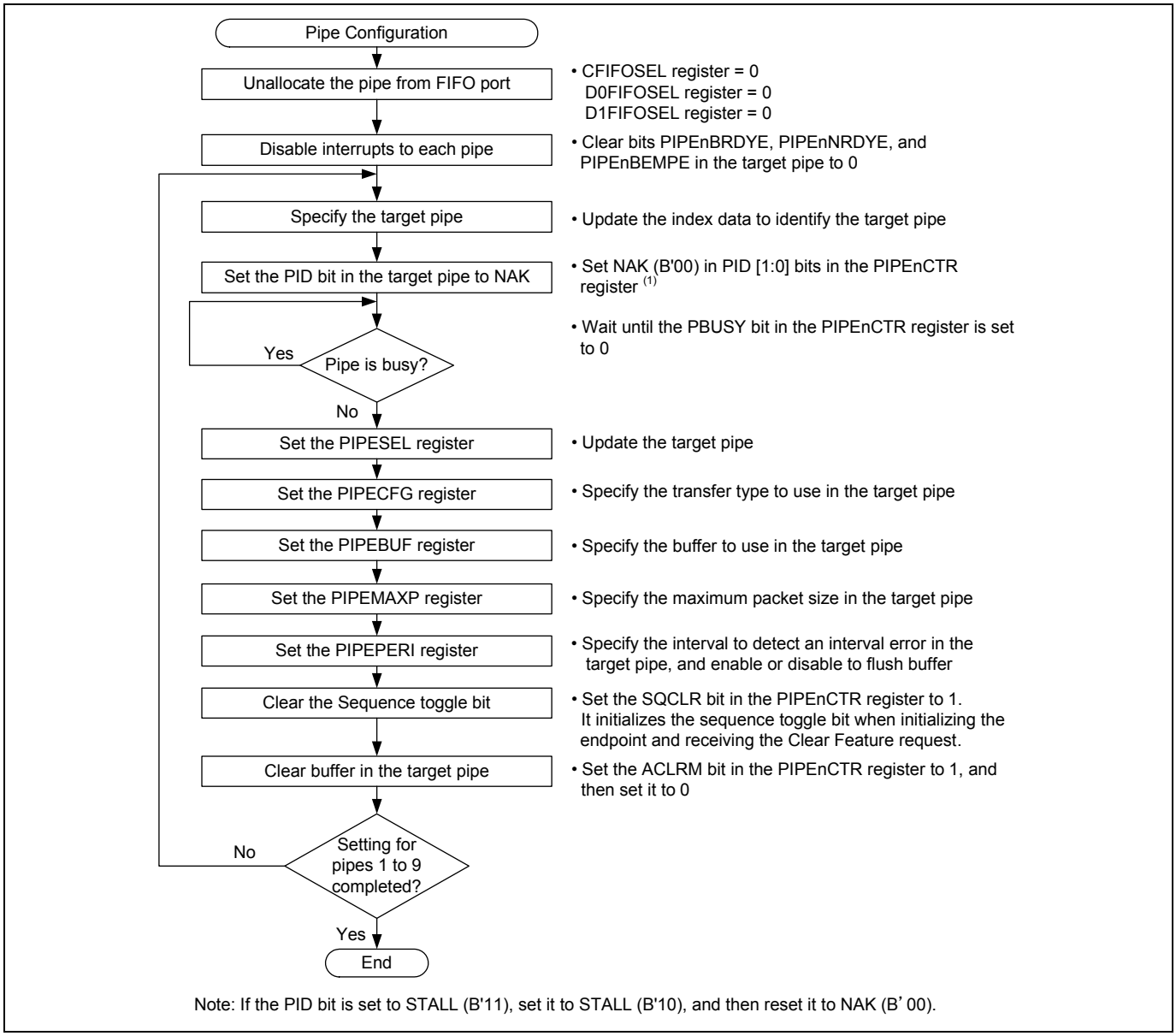


Figure 6 Pipe Configuration Procedure

2.3.3 Transmit Pipe Setting (Isochronous IN Transfer)

This section describes an example of pipe setting when transferring large amounts of data in isochronous IN transfer.

Table 1 lists the setting example of isochronous IN transfer using pipe 1. Figure 7 shows the operation example using the setting listed in Table 1. Double buffering is enabled in this example. As this example assumes to use the DMA transfer to write data to buffer, BRDY and BEMP interrupts are not used. For details, refer to (1) to (8) described in following pages.

Table 1 Isochronous IN Transfer Setting Example Using Pipe 1

Register Name	Setting		Description
PIPESEL register	H'0001		Set pipe 1 as the target pipe
PIPECFG register	H'C211	TYPE [1:0] bits = 3	Set the transfer type as isochronous transfer
		BFRE bit = 0	BRDY interrupt when transmitting/receiving data (Not used)
		DBLB bit = 1	Double buffering
		CNTMD bit = 0	Non-continuous transfer mode (This bit is not enabled in isochronous transfer)
		SHTNAK bit = 0	(Only 0 can be specified when transmitting data)
		DIR bit = 1	Set the transfer direction as transmit
		EPNUM bit = 1	Set the endpoint number as 1
PIPEBUF register	H'3C08	BUFSIZE [4:0] bits = B'01111	Set the buffer size as 1 KB
		BUFNMB [6:0] bits = 8	Set the first block of a buffer as 8
PIPEMAXP register	H'0400		Set the maximum packet size as 1 KB
PIPEPERI register	H'1007	IFIS bit = 1	Buffer is flushed when an interval error is detected
		IITV [2:0] bits = 7	Interval to detect an interval error (note) 16 ms = 125 µs × 2^7
BRDYENB register	PIPE1BRDYE bit = 0		BRDY interrupt is disabled
NRDYENB register	PIPE1NRDYE bit = 0		NRDY interrupt is disabled
BEMPENB register	PIPE1BEMPE bit = 0		BEMP interrupt is disabled
SOFCFG register	BRDYM bit = 0		Clearing the BRDY interrupt status automatically is disabled

Note: The USB module executes isochronous transfer according to the cycle controlled by the USB host. Specify the interval by the bInterval field in the endpoint descriptor.

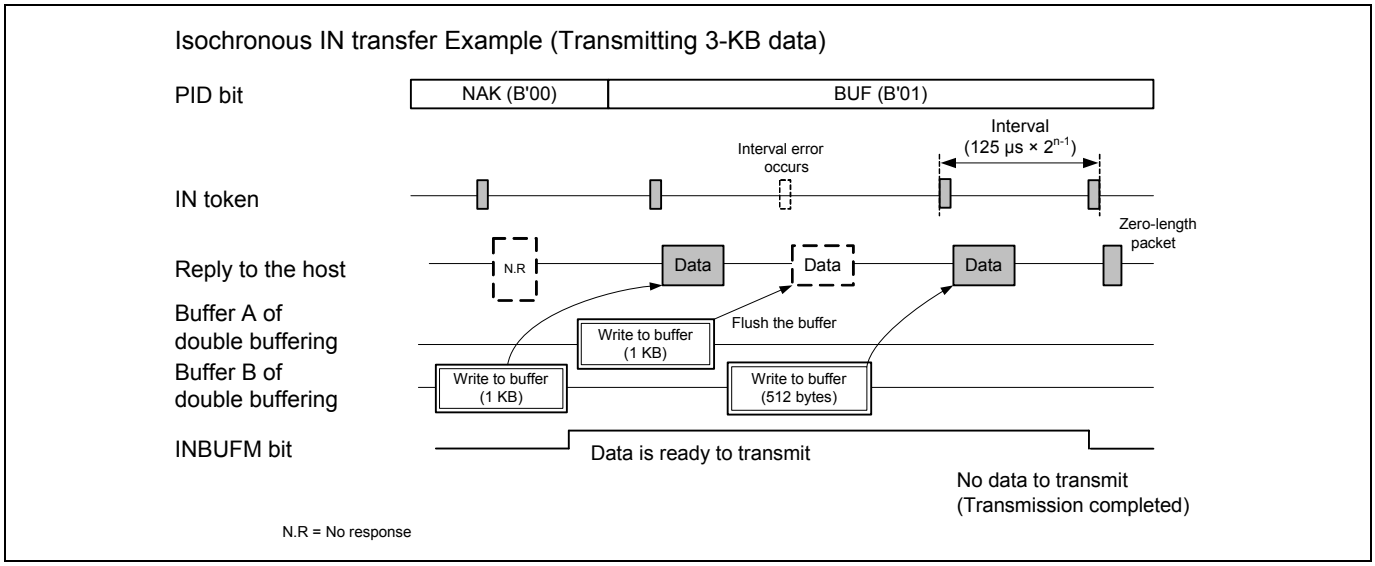


Figure 7 Isochronous IN Transfer Example

(1) Double buffering (DBLB bit)

Double buffering ensures an efficient transmission of large amounts of data. Buffer is operated either by the USB module or the CPU. When using single buffering, the USB module cannot access buffer while the CPU (or DMAC) accesses the buffer. While the CPU accesses the buffer, double buffering allows the USB module to access another buffer to execute the USB transfer efficiently.

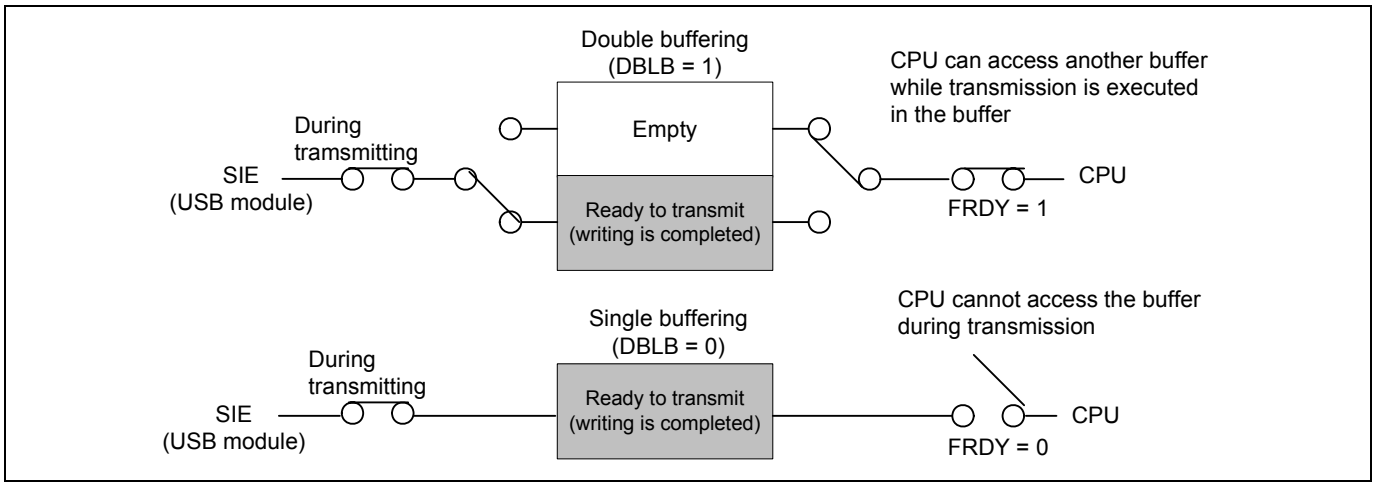


Figure 8 Double Buffering

(2) Continuous transfer mode (CNTMD bit)

Use the continuous transfer mode to transmit or receive multiple transactions continuously. In a single transfer, interrupts are generated when the size of the transmitted or received data reaches the maximum packet size. In a continuous transfer, however, data can be transferred without interrupts to CPU until the size of data reaches the buffer size allocated to each pipe. If the size of data is smaller than the buffer size, set the BVAL bit to 1 to transmit the data.

Note: Continuous transfer mode cannot be used in isochronous transfer.

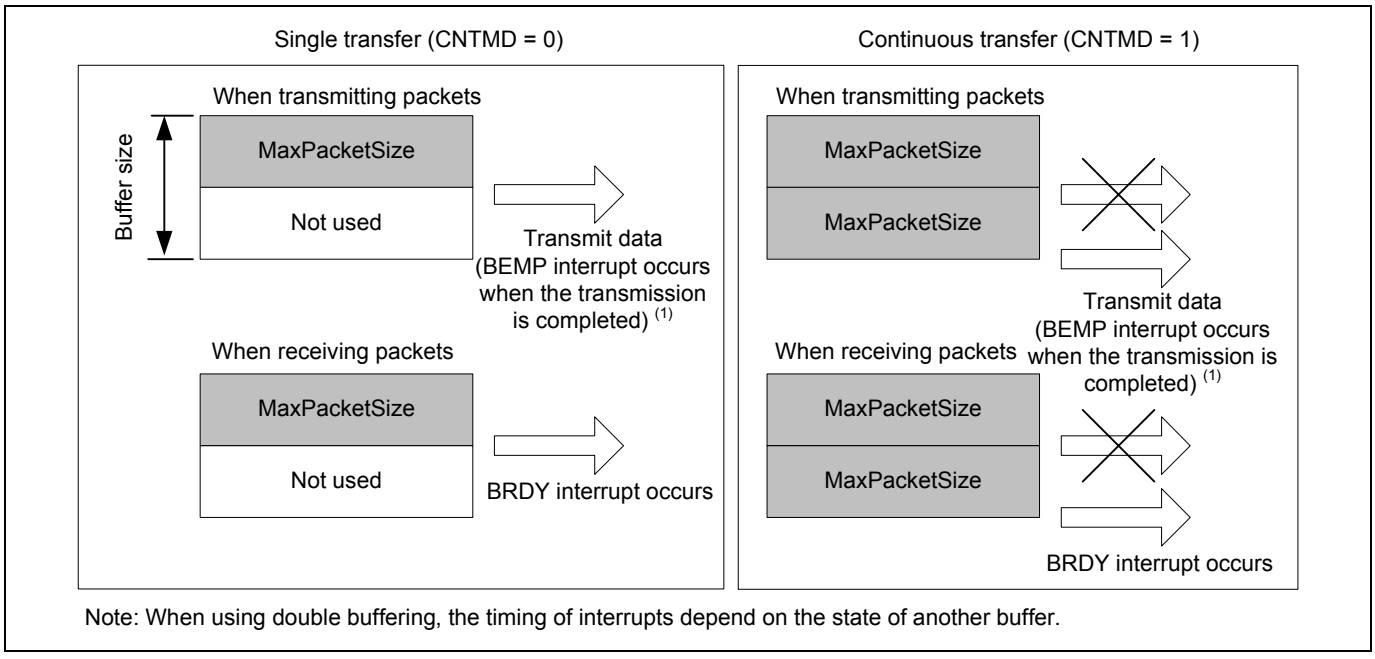


Figure 9 Continuous Transfer Mode

(3) Endpoint Number (EPNUM bit)
Specify the same value as the value of the corresponding endpoint descriptor.

(4) Maximum packet size (PIPEMAXP register)
Specify the value defined in the USB specifications. The USB defines the allowable maximum packet size to be between 1 to 1024 bytes for high-speed transfer, or between 1 to 1023 bytes for full-speed transfer.

(5) Buffer size and the number of the first block in the buffer (PIPEBUF register)
Figure 10 shows the setting example of the buffer size and the block number. To use the pipe, allocate the area from the USB module internal FIFO buffer memory. Specify the first block number and the number of blocks in units of 64-byte blocks as the area. Specify the first block number in the BUFNMB bit, and the value of the number of blocks to allocate -1 in the BUFSIZE bit. Pipes 1 to 5 can be specified up to 2 KB, however, not less than the maximum packet size. Two buffers of the specified memory are allocated when using the double buffering (DBLB bit = 1)

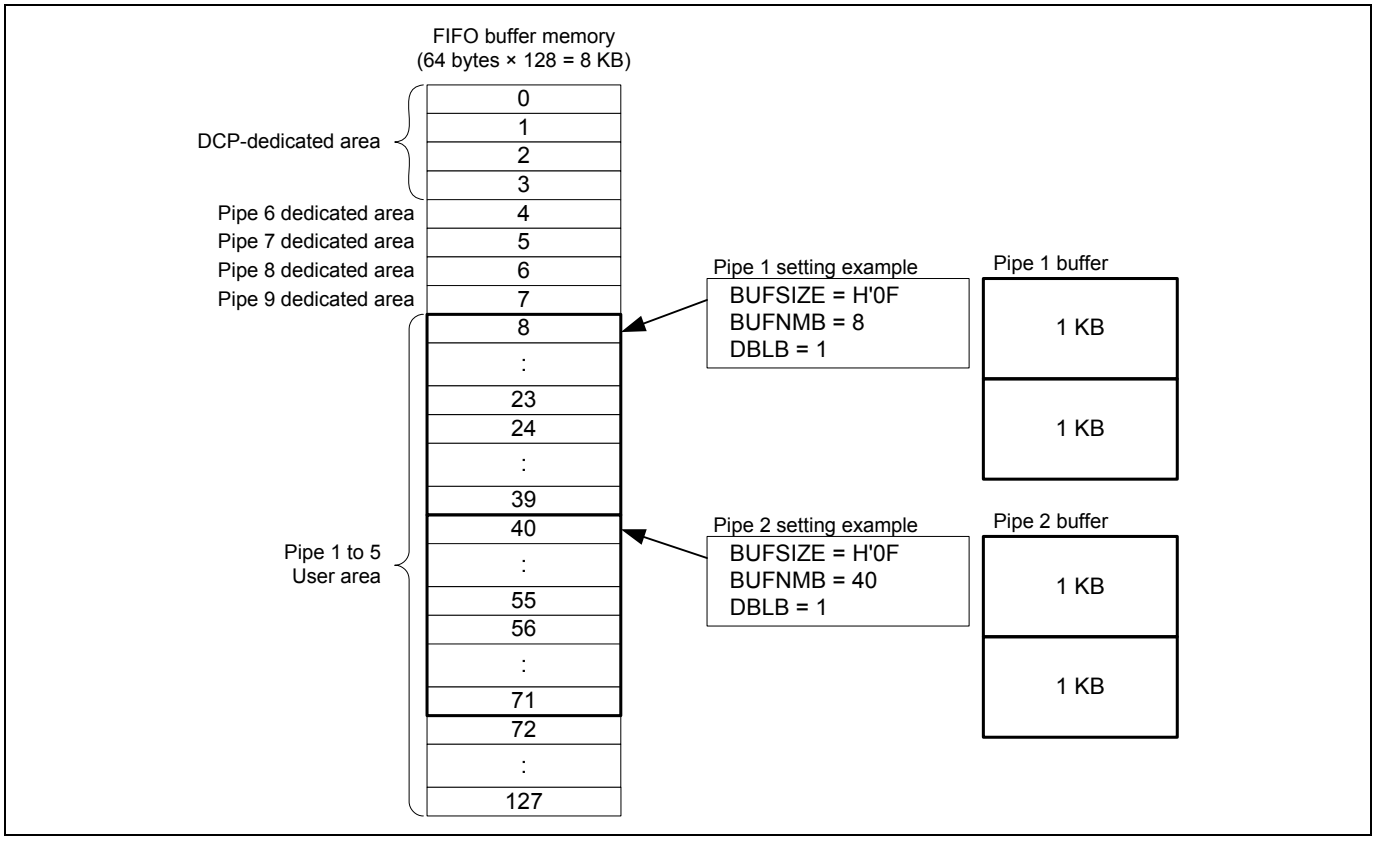


Figure 10 Buffer Size and Block Number Setting

(6) Enabling interrupts (BRDYENB register, BEMPENB register)

Figure 11 shows the interrupt timing in transmission. Enable the required interrupts on each pipe.

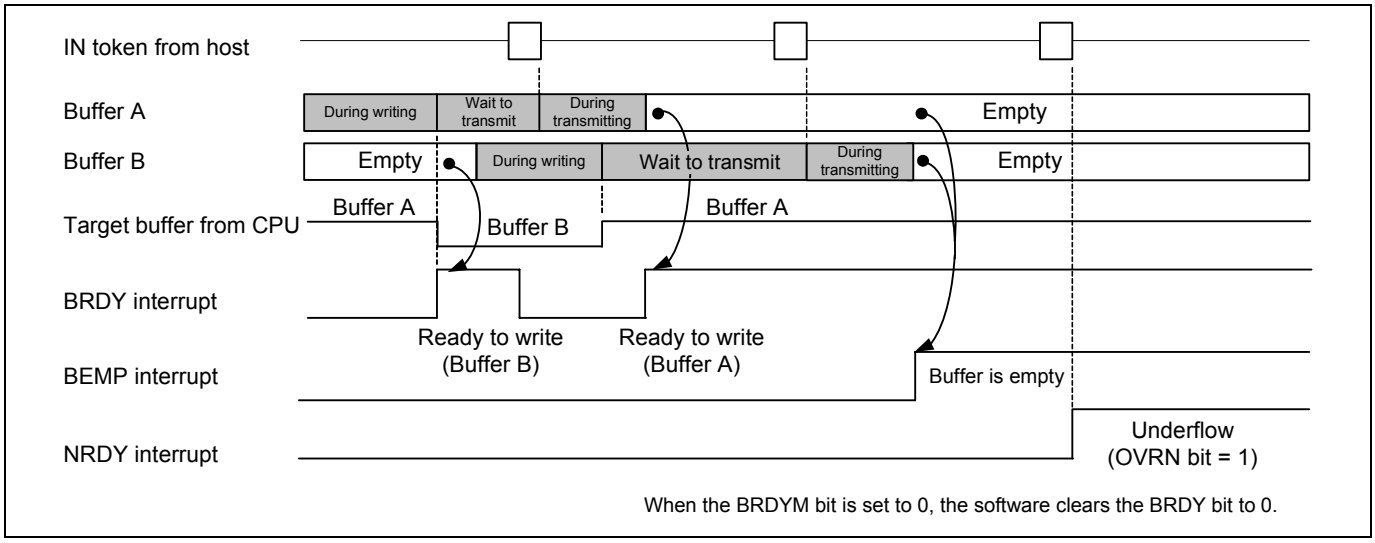


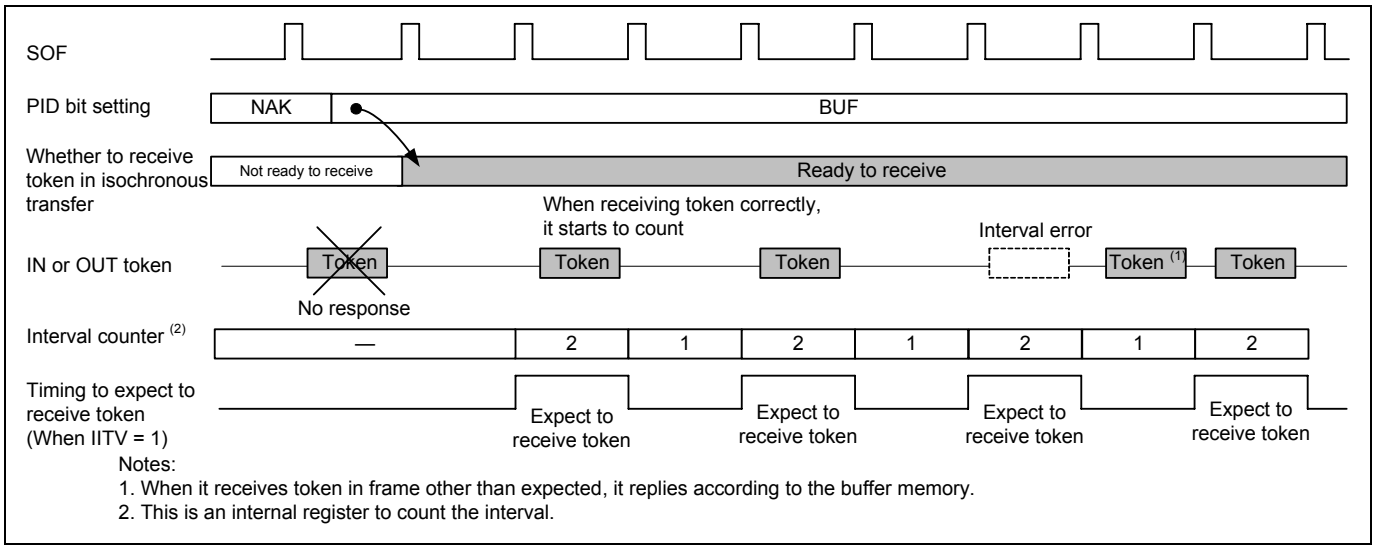
Figure 11 Interrupt Timing in Transmission

(7) Interval to detect an interval error (IITV bit)

Figure 12 shows the timing to occur an interval error. The USB host controls intervals in isochronous transfer, however, the USB function can detect an interval error. Specify the interval in the IITV bit as specified in the bInterval field. The interval must be specified as (micro) frame timing × 2 to the n-th power.

After changing the PID bit to BUF, the USB function starts to count the interval when it completes to transfer data correctly. An interval error occurs when the USB function cannot receive token in expected frame timing in that case. When setting the IITV to 0, however, the USB function starts to count the interval from the next frame after setting the PIF bit to BUF.

When a transfer is aborted after setting the PID bit to NAK or STALL, the interval counter is not initialized. Therefore, clear the buffer memory by the ACLRM bit to start the transfer again, and the USB function starts to count with the IITV bit.



Notes:
1. When it receives token in frame other than expected, it replies according to the buffer memory.
2. This is an internal register to count the interval.

Figure 12 Interval Error Timing

(8) Buffer flushing (IFIS bit)

Buffer flushing feature allows the USB module for continuing to transfer when an interval error occurs in isochronous IN transfer. When setting the IFIS bit to 1, the buffer which was scheduled to transmit at the time when an interval error occurred is automatically cleared.

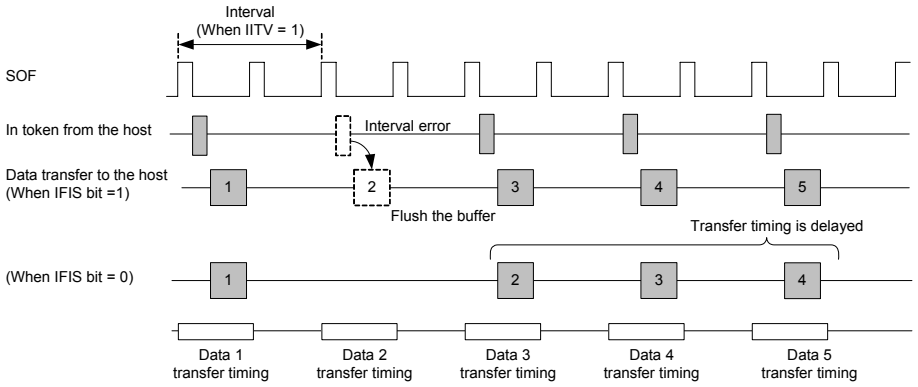


Figure 13 Buffer Flushing

2.3.4 Receive Pipe Setting (Isochronous OUT Transfer)

This section describes an example of pipe setting when transferring large amounts of data in isochronous OUT transfer.

Table 2 lists the setting example of isochronous OUT transfer using pipe 2. Figure 14 shows the operation example using the setting listed in Table 2. Double buffering and continuous transfer mode are enabled in this example. To use the DMA transfer effectively, specify the BRDY interrupt to occur when reading data is completed. For details, refer to (1) to (9) described in following pages.

Table 2 Isochronous OUT Transfer Setting Example Using Pipe 2

Register Name	Setting		Description
PIPESEL register	H'0002		Set pipe 2 as the target pipe
PIPECFG register	H'C682	TYPE [1:0] bits = 3	Set the transfer type as isochronous transfer
		BFRE bit = 1	BRDY interrupt when reading data is completed
		DBLB bit = 1	Double buffering
		CNTMD bit = 0	Non-continuous transfer mode (This bit is not enabled in isochronous transfer)
		SHTNAK bit = 1	Return NAK after receiving the transfer
		DIR bit = 0	Set the transfer direction as receive
		EPNUM bit = 2	Set the endpoint number as 2
PIPEBUF register	H'3C28	BUFSIZE [4:0] bits = B'01111	Specify the buffer size as 1 KB
		BUFNMB [6:0] bits = 40	Specify the first block of a buffer as 40
PIPEMAXP register	H'0400		Specify the maximum packet size as 1 KB
PIPEPERI register	H'0007	IFIS bit = 0	Buffer is not flushed when an interval error is detected (This bit is not enabled in isochronous OUT transfer)
		IITV [2:0] bits = 7	Interval to detect an interval error (note) 16 ms = 125 µs × 2^7
PIPE2TRN register	H'0003		Specify the number of transactions as 3
PIPE2TRE register	H'0100	TRCLR bit = 1	Clear the transaction counter
	H'0200	TRENB bit = 1	Enable the transaction counter
BRDYENB register	PIPE2BRDYE bit = 1		BRDY interrupt is enabled
NRDYENB register	PIPE2NRDYE bit = 0		NRDY interrupt is disabled
BEMPENB register	PIPE2BEMPE bit = 0		BEMP interrupt is disabled
SOFCFG register	BRDYM bit = 0		Clearing the BRDY interrupt status automatically is disabled

Note: The USB module executes isochronous transfer according to the cycle controlled by the USB host. Specify the interval by the bInterval field in the endpoint descriptor.

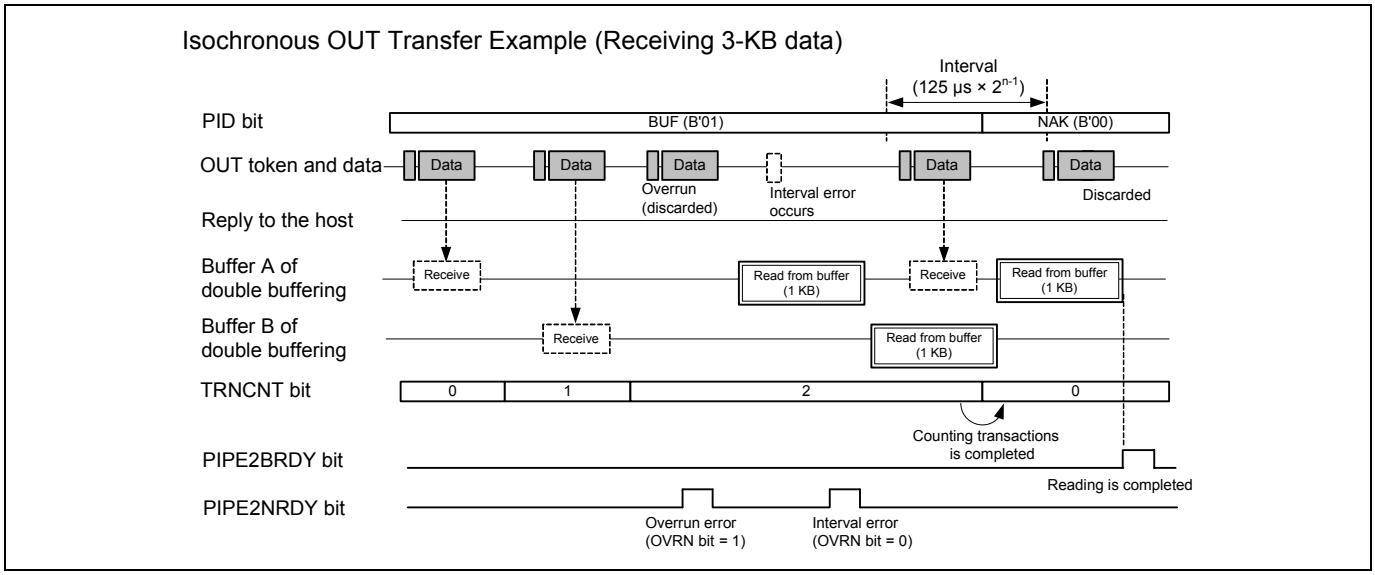


Figure 14 Isochronous OUT Transfer Example

(1) Enabling the transaction counter (PIPEnTRN register, PIPEnTRE register)

Figure 15 shows the transaction counter operation. Enable the transaction counter to receive data by transfer. Specify the total number of transactions in the TRNCNT bit of the receive pipe, and the specify 1 in the TRENB bit. Refer to 2.4.3 Reading Data from the FIFO Port (Isochronous OUT Transfer) for details.

The USB module executes following processing when receiving the same number of packets as set in the TRNCNT bit is completed (transfer is completed). These functions can be used with pipes 1 to 5, receive pipes.

- Hands over the access to buffer from the SIE (USB module) to the CPU if the FIFO buffer is not full in continuous transfer mode (CNTMD = 1)
- When the SHTNAK bit is 1, changes the PID bit to NAK
- When the BFRE bit is 1, asserts the BRDY interrupt after reading data is completed

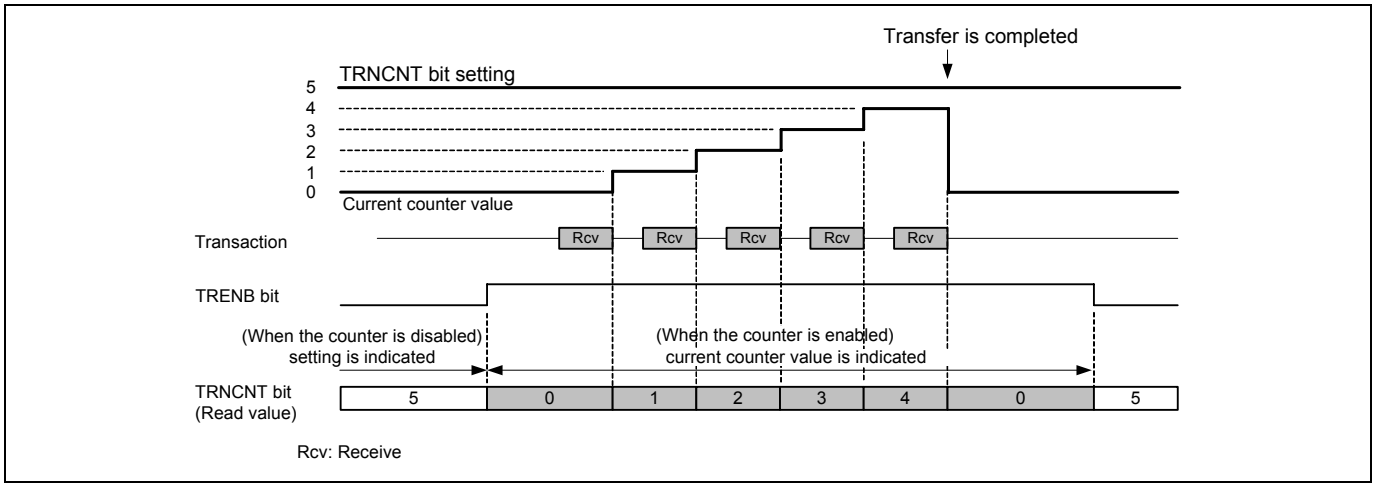


Figure 15 Transaction Counter

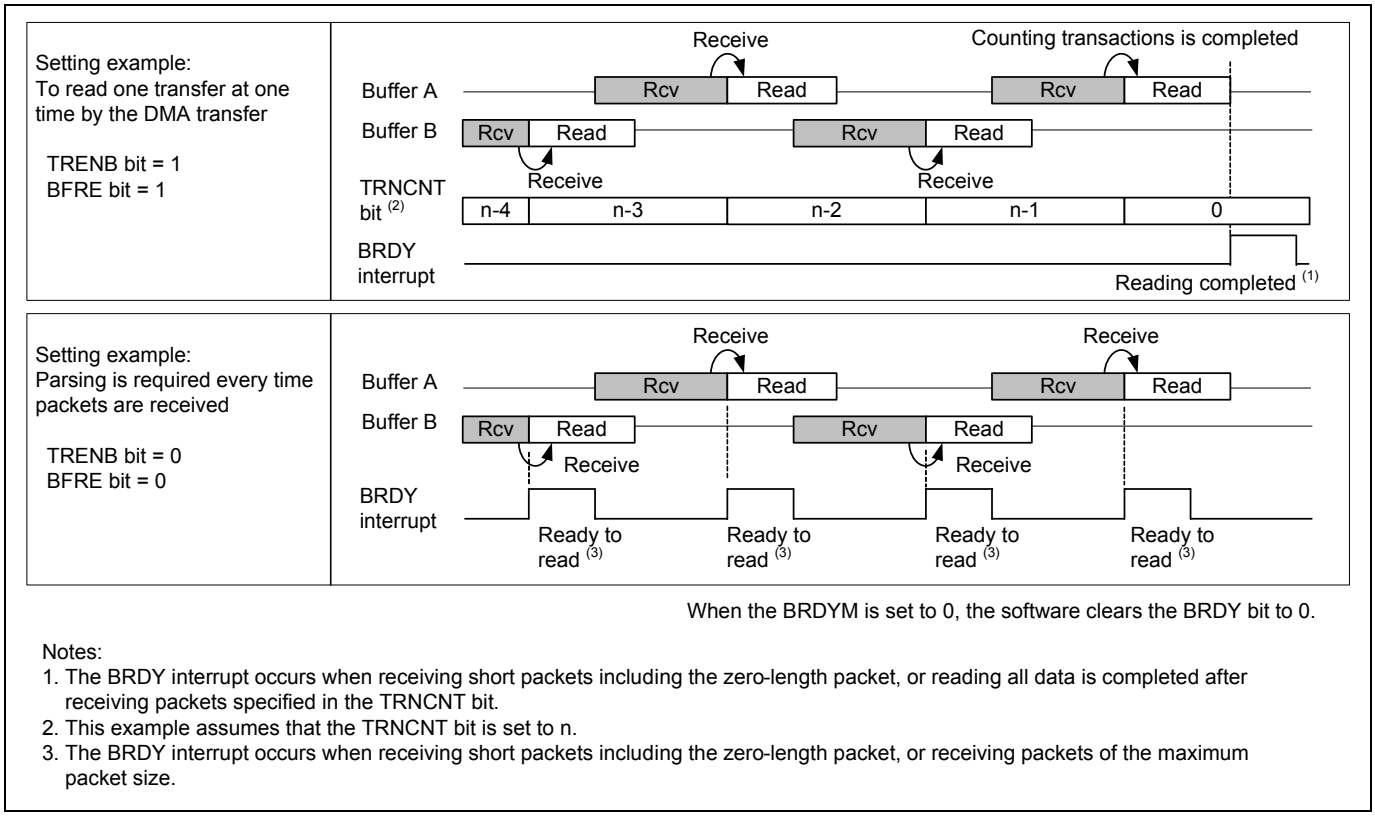
(2) Disabling pipes when transfer is completed (SHTNAK bit)

When setting the SHTNAK bit to disable pipes when a transfer is completed, the USB module automatically changes the PID bit to NAK on receiving transfer is completed, which facilitates the transfer processing. When setting the SHTNAK of the receive pipe to 1, the USB module sets the PID bit corresponding to the target pipe to NAK. The USB module determines that the transfer is completed when the following conditions are satisfied. These functions can be used with pipes 1 to 5, receive pipes.

- When receiving the short packet data (including zero-length packet) correctly
- Using the transaction counter to receive packets of transaction counted correctly

(3) Enabling interrupts (BRDYENB/NRDYENB registers) and specifying the BRDY interrupt (BFRE bit)

Figure 16 shows the BRDY interrupt timing in reception. The BRDY interrupt timing depends on the BFRE bit setting. Set the DREQE bit in the DnFIFOSEL register to 1, and the DMA transfer request is issued when CPU is ready to access buffer. For details on the DMA transfer setting, refer to 2.4 FIFO Port.



Notes:
1. The BRDY interrupt occurs when receiving short packets including the zero-length packet, or reading all data is completed after receiving packets specified in the TRNCNT bit.
2. This example assumes that the TRNCNT bit is set to n.
3. The BRDY interrupt occurs when receiving short packets including the zero-length packet, or receiving packets of the maximum packet size.

Figure 16 BRDY Interrupt Timing in Reception

Figure 17 shows NRDY interrupt timing in reception. Use the NRDY interrupt to detect an interval error, and an overrun. The OVRN bit in the FRMNUM register indicates which source causes the NRDY interrupt.

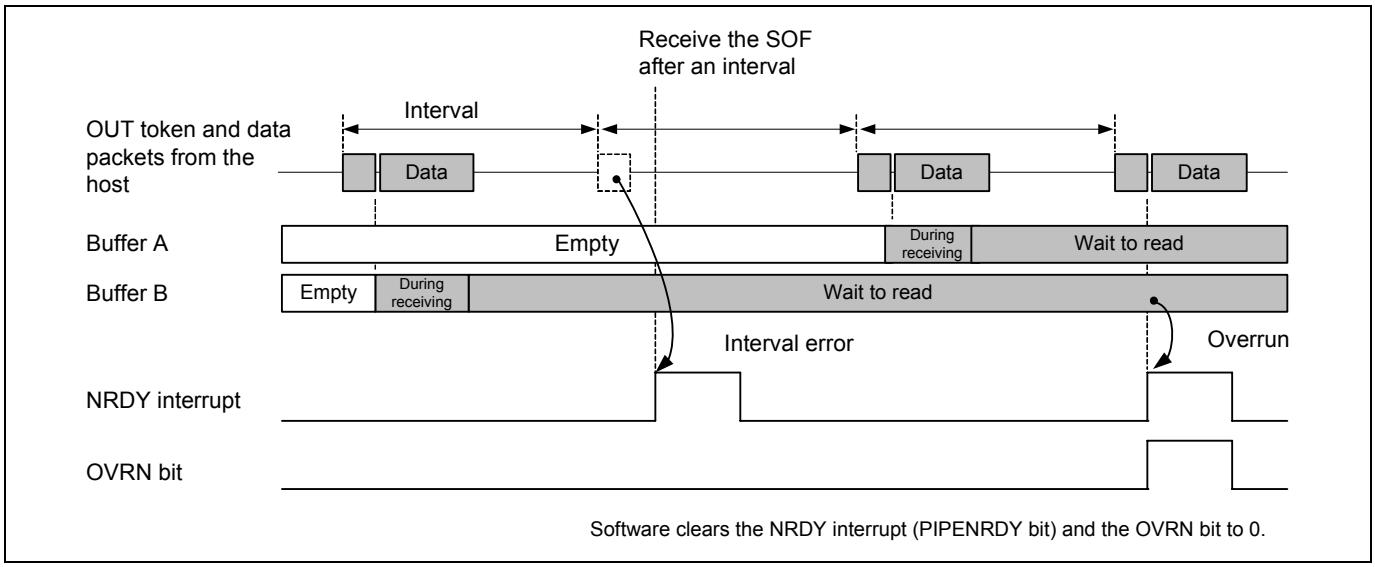


Figure 17 NRDY Interrupt Timing in Reception

(4) Double buffering (DBLB bit)
Apply the same setting as the transmission. See 2.3.3 for details.

(5) Continuous transfer mode (CNTMD bit)
Apply the same setting as the transmission. See 2.3.3 for details.

(6) Maximum packet size (PIPEMAXP register)
Apply the same setting as the transmission. See 2.3.3 for details.

(7) Endpoint number (EPNUM bit)
Apply the same setting as the transmission. See 2.3.3 for details.

(8) Buffer size and the number of the first block in the buffer
Apply the same setting as the transmission. See 2.3.3 for details.

(9) Interval to detect an interval error
Apply the same setting as the transmission. See 2.3.3 for details.

2.4 FIFO Port

Use FIFO port to access (read or write data) the FIFO buffer memory allocated to pipes. This section describes how to access the FIFO buffer memory.

2.4.1 FIFO Port Overview

Figure 18 shows an overview of the FIFO port. The FIFO port has three registers (C/DnFIFO port registers). Specify the pipe number in the CURPIPE bit in the C/DnFIFOSEL register to access the FIFO buffer memory allocated to the specified pipe via the C/DnFIFO port register. Specify the access bit width and endianness in the C/DnFIFOSEL register. The C/DnFIFOCTR register indicates the write end in the buffer memory, and clears buffer.

Make sure to check the setting in the FRDY bit in the C/DnFIFOCTR register before accessing the C/DnFIFO port register, since the FIFO buffer memory may be operated by the system (CPU) or by the USB module (SIE). See bits BSTS and INBUFM in the DCPCTR register and the PIPEnCTR register to check the buffer status in each pipe.

The DCP buffer can be allocated only to the CFIFO port register. The DMA transfer can be used in the D0FIFO port register and the D1FIFO port register.

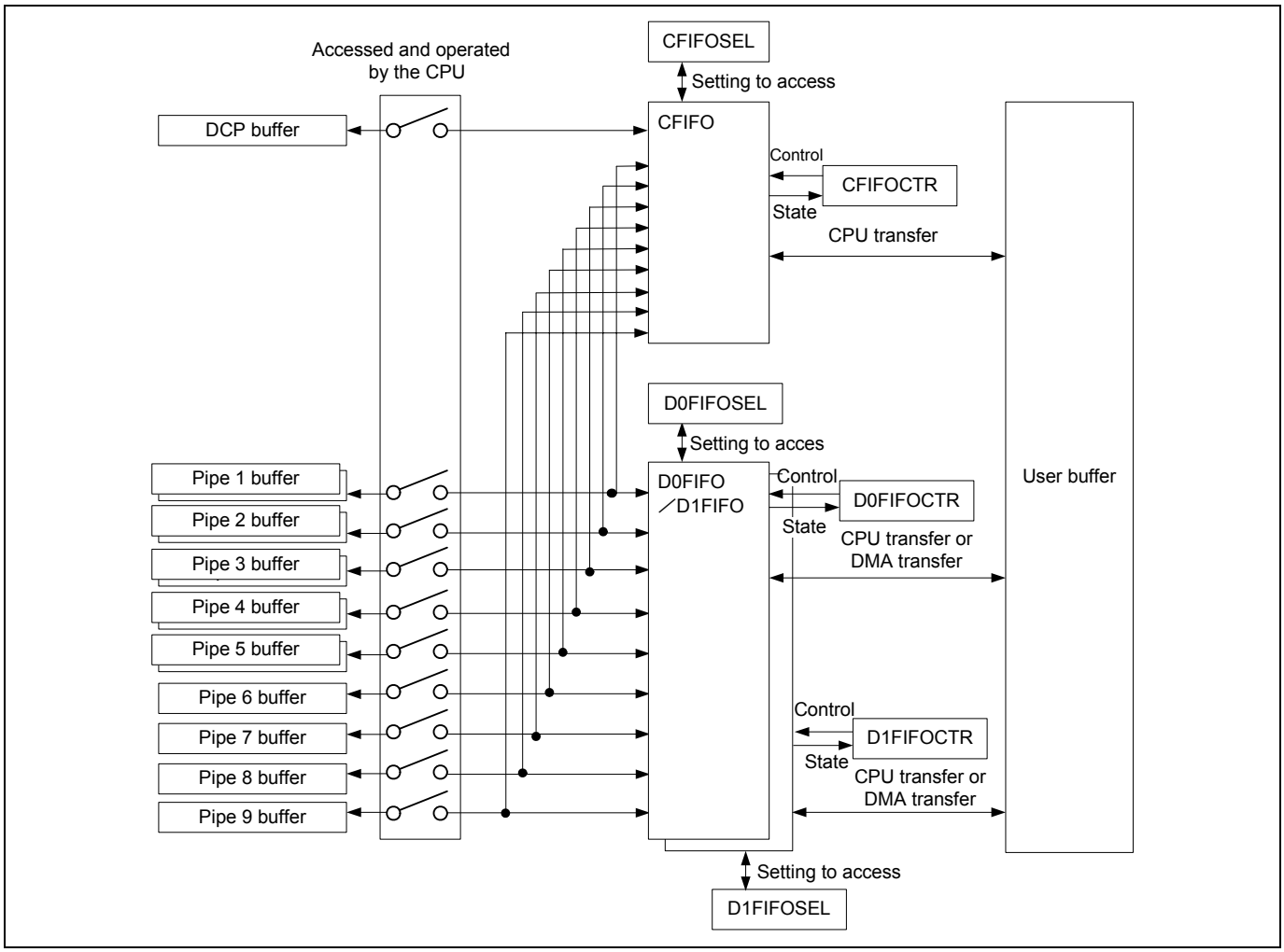


Figure 18 FIFO Port (Overview)

2.4.2 Writing Data to the FIFO Port (Isochronous IN Transfer)

Use the DMA transfer to transfer large amounts of data effectively such as isochronous IN transfer. This section describes the procedures on writing data in the D0FIFO port register using the DMA transfer.

Figure 19 shows an example or writing data to the FIFO port. Figure 20 shows the DMAC setting example. Note that the target pipe cannot be changed during the DMA transfer.

Figure 21 shows an example of the DMA transfer end interrupt (Isochronous IN transfer). The DMAC transfer end interrupt detects when writing to buffer is completed. Refer the INBUFM bit setting after the DMA transfer is completed to confirm that isochronous IN transfer is completed.

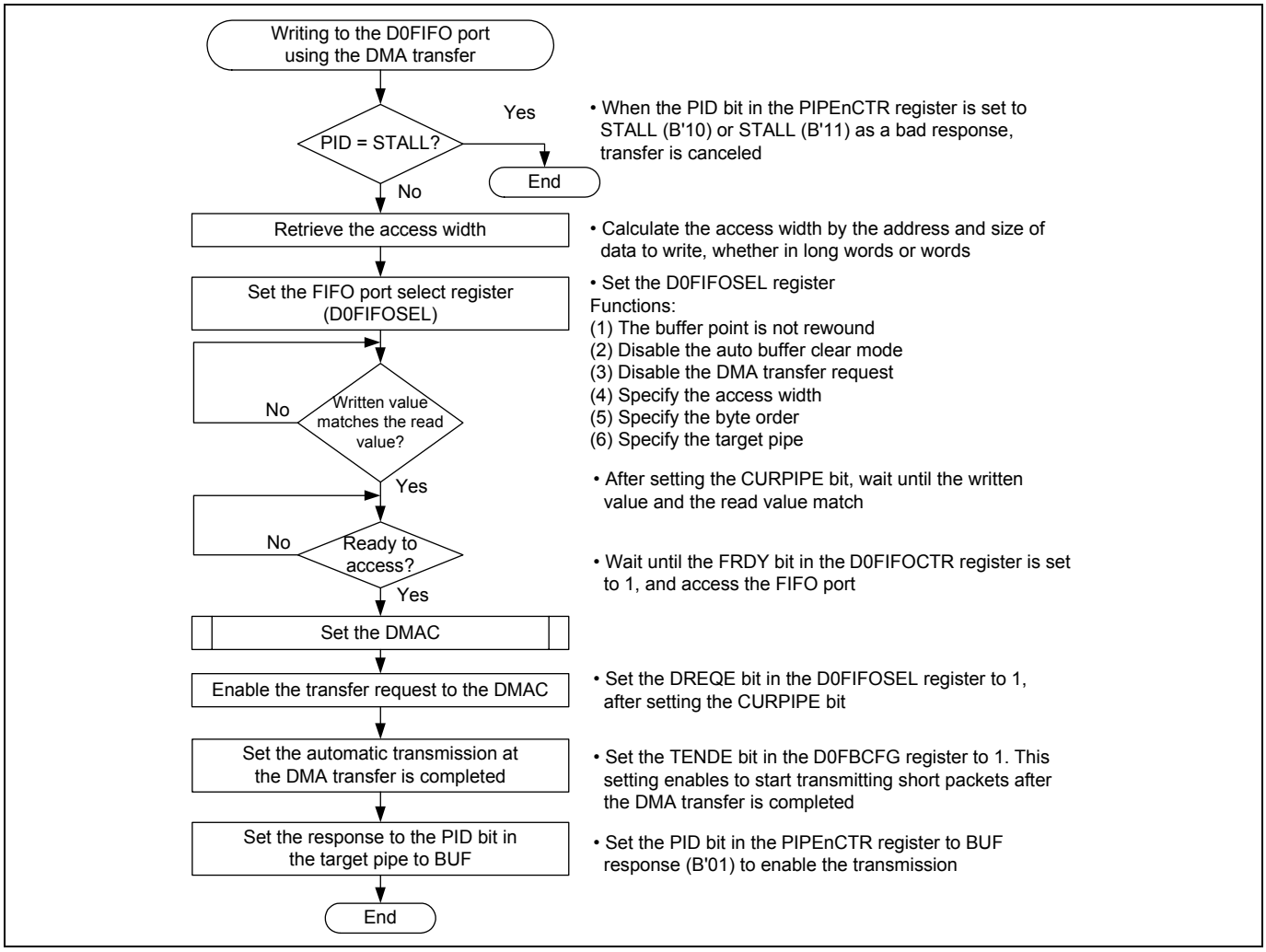


Figure 19 Writing Data to the FIFO Port

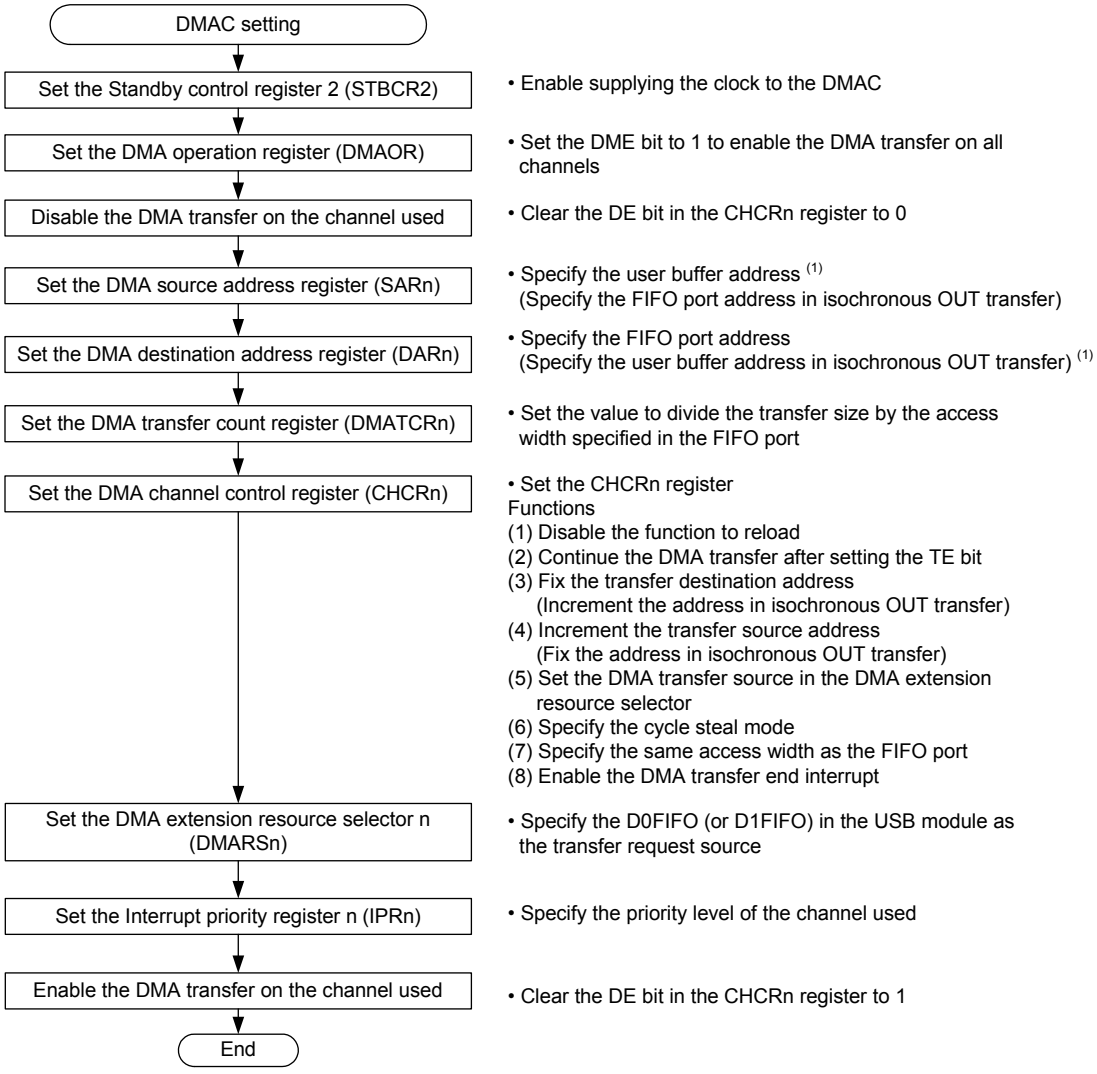


Figure 20 DMAC Setting

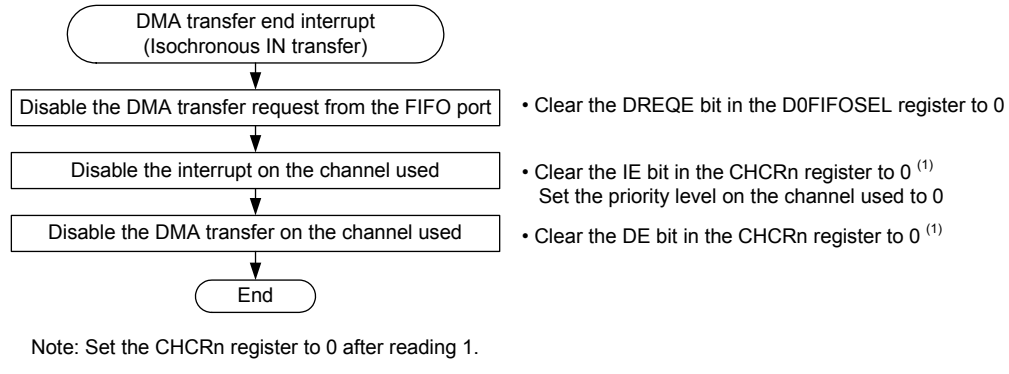


Figure 21 DMA Transfer End Interrupt Example (Isochronous IN Transfer)

2.4.3 Reading Data from the FIFO Port (Isochronous OUT Transfer)

This section describes the procedure to read data from the D1FIFO port register. Read one transfer data using the DMA transfer, and generate the BRDY interrupt.

Figure 22 and Figure 23 show examples of reading data from FIFO port. Refer to Figure 20 for procedures to set the DMAC. Figure 24 shows an example of the DMA transfer end interrupt (isochronous OUT transfer). Figure 25 shows an example of the BRDY interrupt. As same as writing data to the FIFO port, the target pipe cannot be changed during the DMA transfer.

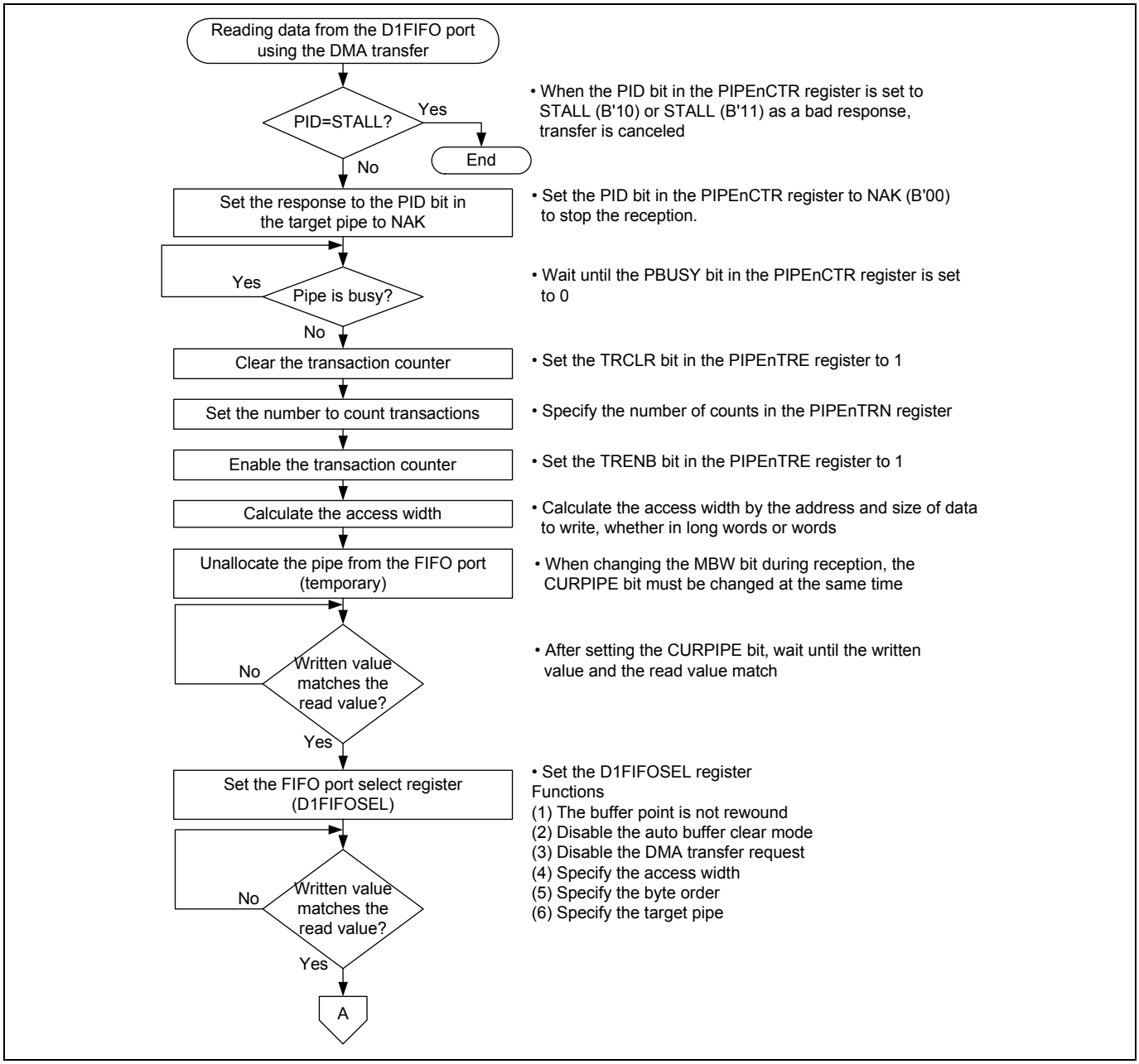


Figure 22 Reading Data from the FIFO Port (1/2)

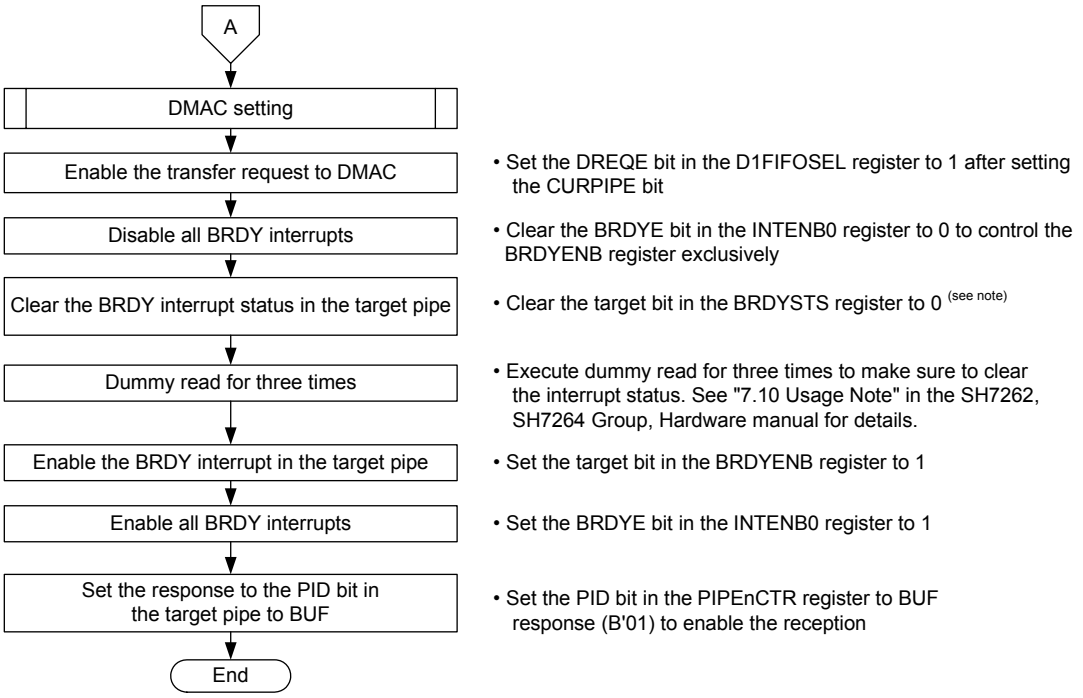


Figure 23 Reading Data from the FIFO Port (2/2)

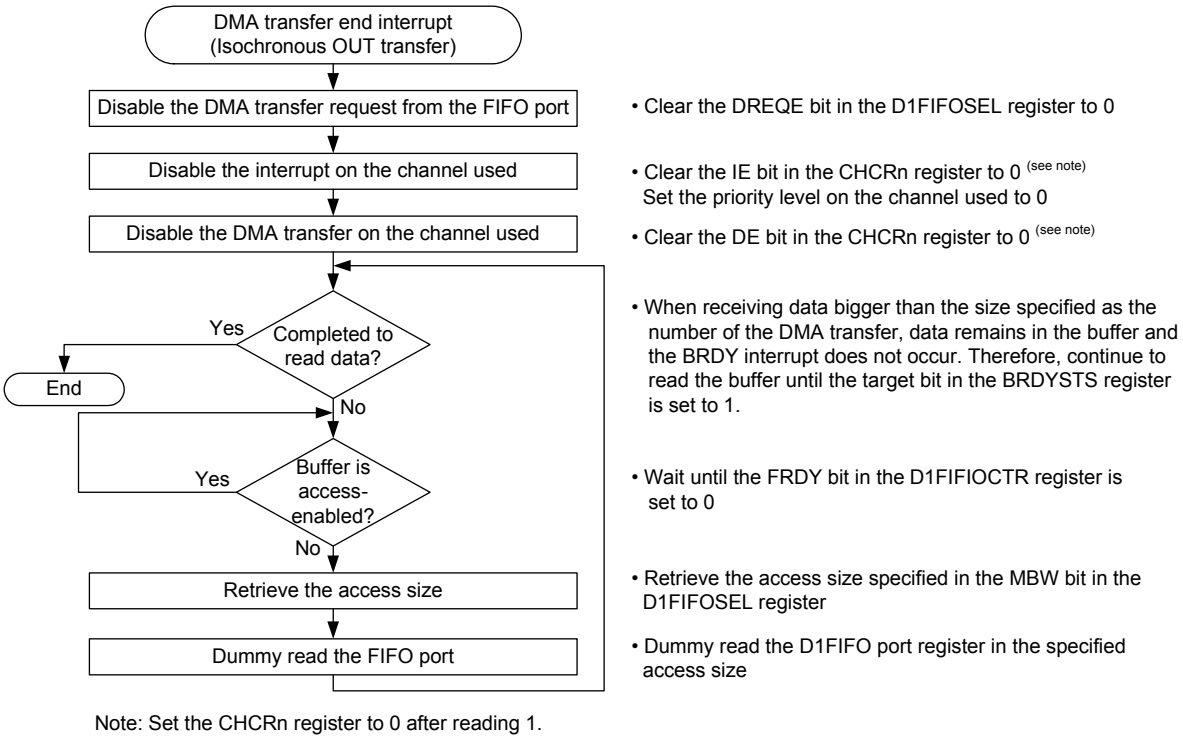


Figure 24 DMA Transfer End Interrupt (Isochronous OUT Transfer)

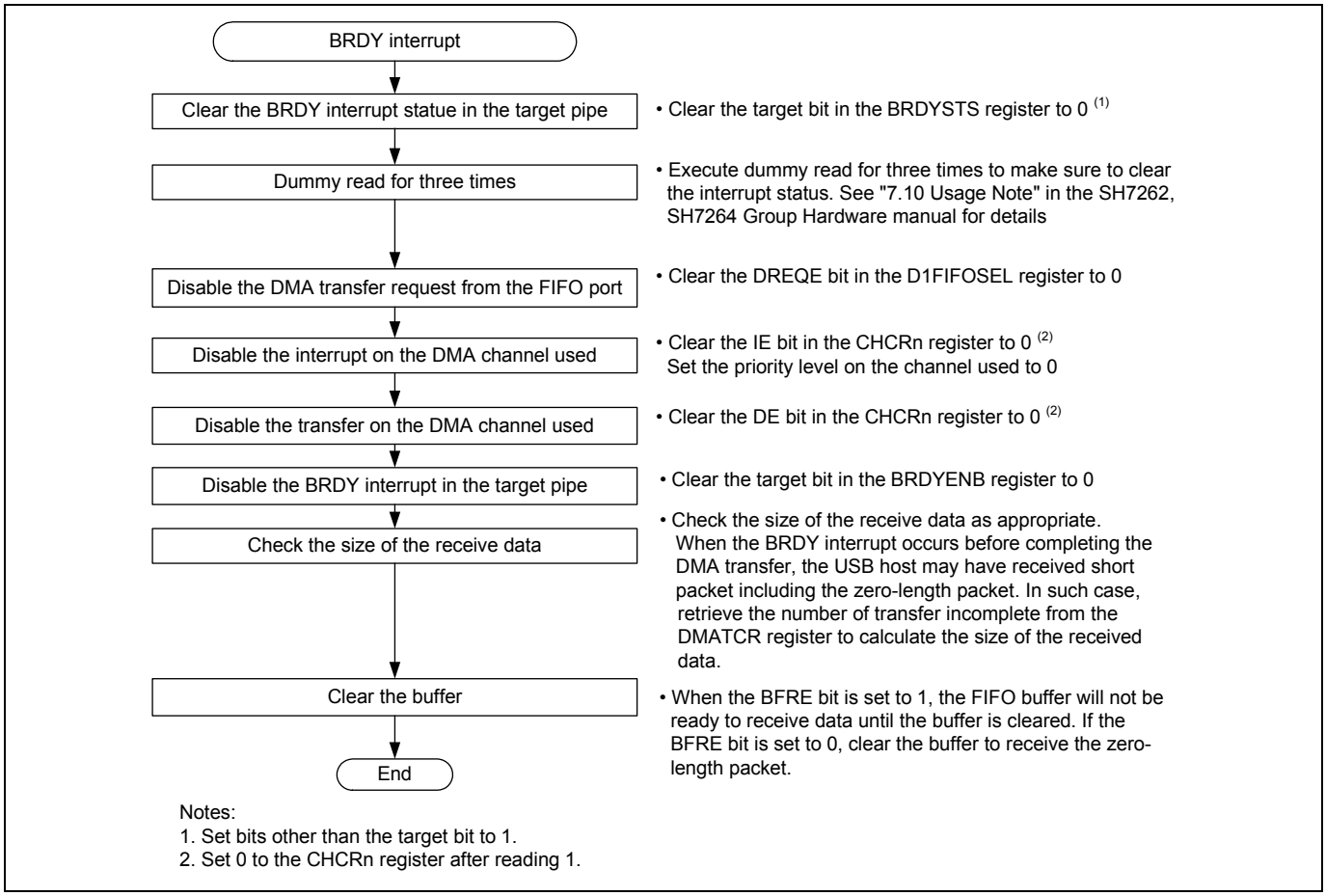


Figure 25 BRDY Interrupt (Isochronous OUT Transfer)

3. References

- Software Manual
  SH-2A/SH-2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas website.

- USB 2.0 Specifications
  Universal Serial Bus Specification Revision 2.00
  (http://www.usb.org/developers)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb. 12, 2010	—	First edition issued

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