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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

Unsigned 64-Bit Binary Division

Introduction

The software DIVIDE64 carries out division in this format:

Dividend (unsigned, 64 bits)/divisor (unsigned, 32 bits) = quotient (unsigned, 32 bits) … remainder (unsigned, 32 bits). Division by 0 sets the Z flag.

Target Device

H8/300H Tiny Series

Contents

1. Functions

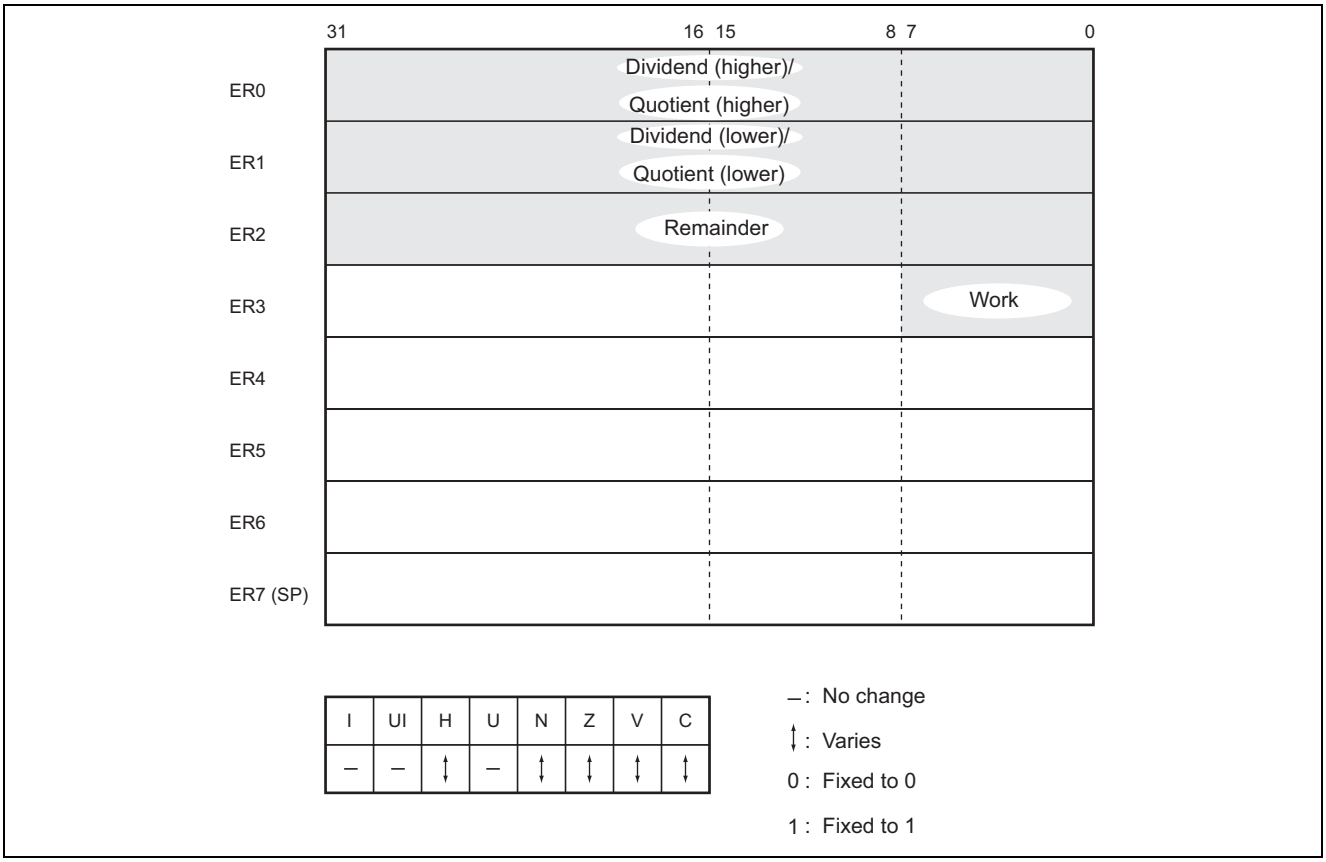
The software DIVIDE64 carries out division in this format:

Dividend (unsigned, 64 bits)/divisor (unsigned, 32 bits) = quotient (unsigned, 32 bits) … remainder (unsigned, 32 bits). Division by 0 sets the Z flag.

2. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Dividend: higher-order bytes (unsigned, 32 bits)	ER0	4
	Dividend: lower-order bytes (unsigned, 32 bits)	ER1	4
	Divisor (unsigned, 32 bits)	ER2	4
Output	Quotient: higher-order bytes (unsigned, 32 bits)	ER0	4
	Quotient: lower-order bytes (unsigned, 32 bits)	ER1	4
	Remainder (unsigned, 32 bits)	ER3	4
	Occurrence of error (division by 0) (Yes: Z = 1; No: Z = 0)	Z flag (CCR)	—

3. Changes to Internal Registers and Flags



4. Programming Specifications

Program memory (bytes)
32
Data memory (bytes)
0
Stack (bytes)
0
Number of cycles
3894
Re-entrant
Yes
Relocatable
Yes
Interrupts during execution
Yes

5. Note

The number of states in the programming specifications is the value for calculation of H'FFFFFFFFFFFFFFFF/H'01.

6. Description

6.1 Description of Functions

1. The arguments are as follows:
   ER0: Sets the higher-order bytes of a dividend (unsigned, 32 bits) as an input argument. The higher-order bytes of the quotient (unsigned, 32 bits) is also set here, as an output argument.
   ER1: Sets the lower-order bytes of a dividend (unsigned, 32 bits) as an input argument. The lower-order bytes of the quotient (unsigned, 32 bits) is also set here, as an output argument.
   ER2: Sets the divisor (unsigned, 32 bits) as an input argument.
   ER3: The remainder (unsigned, 32 bits) is set here as an output argument.
   Z flag (CCR): Indicates whether there are any errors (division by 0) after execution of DIVIDE64.
   Z flag = 1: The division was in error.
   Z flag = 0: The division was processed without error.

2. The following figure illustrates the execution of the software DIVIDE64. When the input arguments are set as shown below, DIVIDE64 places the quotient in ER0 and ER1, and the remainder in ER3.

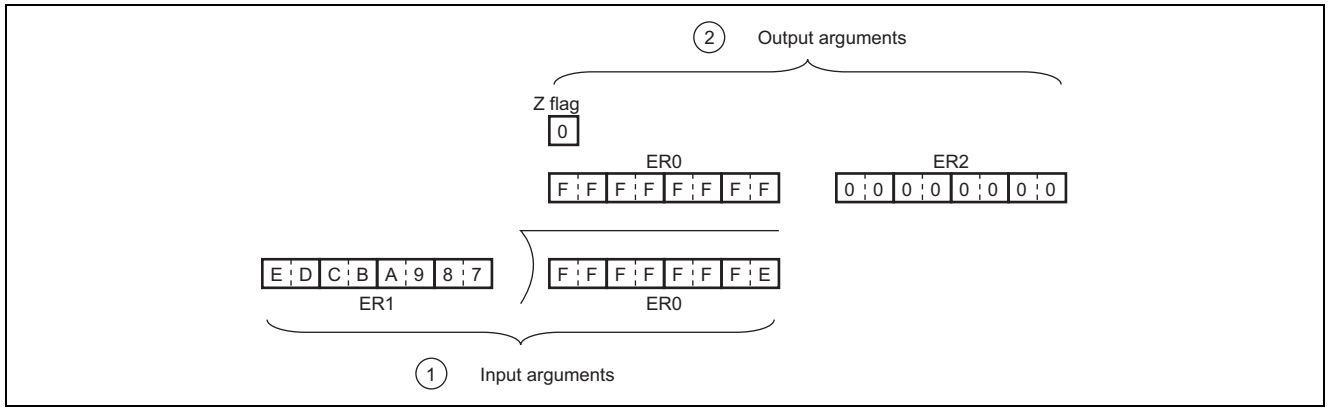


Figure 1 Example of Software DIVIDE64

3. The software DIVEDE64 first checks whether the given divisor is 0; and if so, the software DIVEDE64 ends.

6.2 Usage Notes

Since the quotient is set in ER0 and ER1, the dividend will be lost through the execution of DIVIDE64. If the dividend is still required, save it elsewhere in memory beforehand.

6.3 Description of Data Memory

No data memory is used by DIVIDE64.

6.4 Example of Usage

```
WORK1   . RES. L 1          ..... Reservation of the data memory area
                                  for setting of the higher 32 bits of the dividend (unsigned) by the user program.
WORK2   . RES. L 1          ..... Reservation of the data memory area
                                  for setting of the lower 32 bits of the dividend (unsigned) by the user program.
WORK3   . RES. L 1          ..... Reservation of the data memory area for setting of the divisor (unsigned, 32 bits) by the user program.
          .
          .
          .
        MOV. L @WORK1, ER0  ..... Sets, as an input argument, the higher 32 bits of the dividend (unsigned) specified by the user program.
        MOV. L @WORK2, ER1  ..... Sets, as an input argument, the lower 32 bits of the dividend (unsigned) specified by the user program.
        MOV. L @WORK3, ER2  ..... Sets, as an input argument, the divisor (unsigned, 32 bits) specified by the user program.
        JSR  @DIVIDE64      ..... Subroutine call of DIVIDE64.
```

6.5 Principle of Operation

1. In binary division, the quotient and remainder are found through repeated subtraction. In the following figure, the division of H'0D by H'03 is given as an example of this operation.

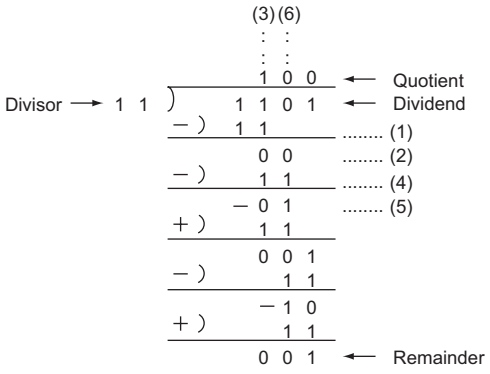
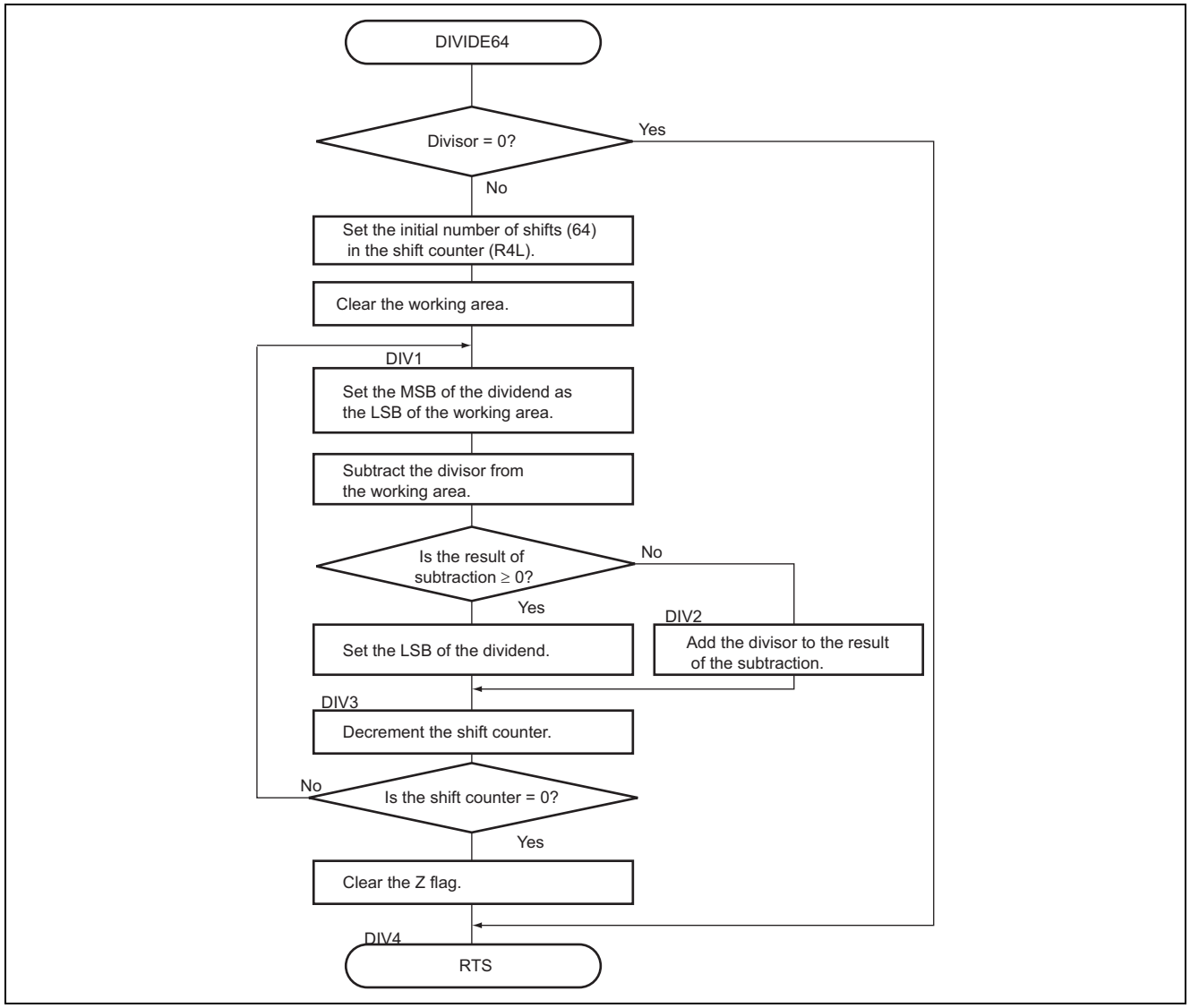


Figure 2 Example of Division (H'0D divided by H'03)

2. Detailed description of the program:
   1) The initial number of shifts is set in the counter R4L, which indicates the number of shifts.
   2) The dividend is shifted 1 bit to the left and the MSB thus loaded to the C bit is set as the LSB of ER3, which will hold the remainder.
   3) The divisor is subtracted from ER3. When the result of subtraction is positive, the LSB of ER1 is set ((1) → (2) → (3) in the figure). When the result of subtraction is negative, the LSB of ER1 is cleared and the divisor is added to the result of subtraction, returning it to the state prior to subtraction ((4) → (5) → (6) in the figure).
   4) The shift counter set in step 1) above is decremented.
   5) Steps 2) to 4) are repeated until the shift counter reaches –1.

7. Flowchart


DIVIDE64
Divisor = 0?
Yes
No
Set the initial number of shifts (64) in the shift counter (R4L).
Clear the working area.
DIV1
Set the MSB of the dividend as the LSB of the working area.
Subtract the divisor from the working area.
Is the result of subtraction ≥ 0?
No
Yes
DIV2
Add the divisor to the result of the subtraction.
Set the LSB of the dividend.
DIV3
Decrement the shift counter.
No
Is the shift counter = 0?
Yes
Clear the Z flag.
DIV4
RTS

8. Program Listing

```
   1                1  ;*************************************************************************
   2                2  ;*                                    *
   3                3  ;*         NAME   :   64 BIT DIVISION (DIVIDE64)           *
   4                4  ;*                                    *
   5                5  ;*************************************************************************
   6                6  ;*                                    *
   7                7  ;*         ENTRY  :   ER0             (DIVIDEND UPPER)     *
   8                8  ;*                    ER1             (DIVIDEND LOWER)     *
   9                9  ;*                    ER2             (DIVISOR)     *
  10               10  ;*         RETURN :   ER0             (QUOTIENT UPPER)     *
  11               11  ;*                    ER1             (QUOTIENT LOWER)     *
  12               12  ;*                    ER3             (RESIDUAL)    *
  13               13  ;*                                    *
  14               14  ;*************************************************************************
  15               15  ;
  16               16             .CPU        300HN
  17 0000          17             .SECTION              DIVIDE64_code,CODE,ALIGN=2
  18               18             .EXPORT               DIVIDE64
  19               19  ;
  20       00000000  20  DIVIDE64   .EQU        $          ;Entry point
  21 0000  0FA2      21             MOV.L       ER2,ER2
  22 0002  471A      22             BEQ         DIV4
  23 0004  FC40      23             MOV.B       #64,R4L    ;Set shift counter
  24 0006  1AB3      24             SUB.L       ER3,ER3    ;Clear residual
  25 0008  1031      25  DIV1       SHLL.L      ER1        ;Shift dividend 1 bit left
  26 000A  1230      26             ROTXL.L               ER0
  27 000C  1233      27             ROTXL.L               ER3 ;Set MSB of dividend to LSB of residual
  28 000E  1AA3      28             SUB.L       ER2,ER3    ;Sub divisor from residual
  29 0010  4404      29             BCC         DIV2       ;Branch if residual >= divisor
  30 0012  0AA3      30             ADD.L       ER2,ER3    ;Add divisor to residual
  31 0014  4002      31             BRA         DIV3       ;Branch always
  32 0016  7009      32  DIV2       BSET        #0,R1L     ;Set 1 to dividend LSB
  33 0018  1A0C      33  DIV3       DEC.B       R4L        ;Decrement shift counter
  34 001A  46EC      34             BNE         DIV1       ;Branch until shift counter = 0
  35 001C  06FB      35             ANDC        #B'11111011,CCR
  36               36  ;
  37 001E  5470      37  DIV4       RTS
  38               38  ;
  39               39             .END
*****TOTAL ERRORS   0
*****TOTAL WARNINGS    0
```

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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