Tsi107™ Revision 1.3/1.4 Device Differences

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About this Document

This document describes electrical and functional differences between Revision 1.3 and Revision 1.4 of the Tsi107 PowerPC Host Bridge, which provides system interconnect between PowerPC processors, PCI peripherals and local memory.

This document covers the following topics:

1 Overview

Revision 1.3 of the Tsi107 is limited to a processor/memory bus frequency of 100 MHz, and has errata that some customers have deemed unsuitable for their design requirements. Revision 1.4 of the Tsi107 implements fixes for the errata to make it more suitable for new designs. Specification changes for Rev 1.4 address the frequency limitation. Because many existing designs are unaffected by the 100-MHz limit and the errata on Rev 1.3, and because Rev 1.4 introduces timing and functional changes to the Tsi107, many customers choose to continue specifying Rev 1.3 in their designs.

This document describes the differences between Rev 1.3 and Rev 1.4. It helps to assess which revision is appropriate for a specific design and what changes may be necessary when migrating a system design from Rev 1.3 to Rev 1.4.

Table 1 describes how to distinguish between Rev 1.3 and Rev 1.4 devices. The orderable part number and the part marking contain a revision code that refers to the die mask revision number. Reading the Revision ID register at configuration address offset 0x08 can determine the revision level of an installed device.

Table 1. Identifying Revision Level

Tsi107 Die Mask Revision Level	Revision Code	Revision ID Register (offset 0x08)
1.3	C	0x13
1.4	D	0x14

2 Electrical Differences

The only changes in the electrical specifications are to allow the Tsi107 to achieve 133-MHz processor/memory bus operation timing. Note that these are specification changes that manufacturing supports, and are not design changes. Therefore, Rev 1.4 devices marked for 100-MHz operation have the same electrical characteristics as Rev 1.3 devices. Table 2 summarizes the changes for the 133-MHz-rated Rev 1.4 Tsi107.

Table 2. Electrical Differences—100 MHz/133 MHz

Electrical Characteristic	Rev 1.3/Rev 1.4 (100-MHz Device)	Rev 1.4 (133-MHz Device Only)
Maximum 60x and memory bus frequency	100 MHz	133 MHz
Supply voltages—core, PLL, and DLL (V_{DD}, AV_{DD}, and LAV_{DD})	2.5 V_{DC}	2.7 V_{DC}
60x and memory interface signals—output valid time (Specs 12 b and 12e)	5.5 nsec	4.5 nsec
Maximum die junction temperature (T_j)	105 °C	85 °C
Power consumption	See Tsi107 *Hardware Specification*	Slightly higher due to elevated supply voltage
I^2C frequencies	See Tsi107 *Hardware Specification*	Higher due to higher memory bus frequency of 133 MHz (the divisors are the same)
PLL[0:4] configurations	Frequency range limited to 100 MHz for PLL[0:4] configurations 0x5, 0x8, and 0xC	Frequency range higher for PLL[0:4] configurations 0x5, 0x8, and 0xC

3 Functional Differences

Rev 1.3 of the Tsi107 has known errata that affect functionality. Rev 1.4 fixes some of those errata, but implementing the fixes introduced functionality changes. The following sections describe the specific Rev 1.3 errata that Rev 1.4 addresses.

3.1 Fast Back-to-Back Capability

For all revisions of the Tsi107 before Rev 1.4, bit 7 of the PCI status register is hardwired to 1, indicating that the Tsi107 can support fast back-to-back transactions. Due to a chip errata, if an external PCI master issues a type 2 fast back-to-back transaction (read or write) to a Tsi107, the transaction causes data corruption. (Type 2 fast back-to-back transactions access multiple targets sequentially.)

The suggested work-around for this errata is to use software to disable the ability to run fast back-to-back transactions on any potential master devices by clearing bit 9 of the PCI command register in the master device. The solution implemented in Rev 1.4 of the Tsi107 is to hardwire bit 7 of the PCI status register to 0, indicating that it is not capable of accepting fast back-to back transactions as a target.

3.2 MPC7450 Compatibility

Revisions of the Tsi107 before Rev 1.4 have compatibility issues with the MPC7450 and its derivatives. The compatibility issues are documented in the *Tsi107 PowerPC Host Bridge Device Errata*. The MPC7450 implementation of the 60x bus protocol is slightly more restrictive, in that data must never be transferred before the last cycle of the $\overline{\text{ARTRY}}$ window (the cycle after $\overline{\text{AACK}}$ is asserted). Similarly, $\overline{\text{TEA}}$ must not be asserted to terminate a data tenure before the last cycle of the $\overline{\text{ARTRY}}$ window.

The actual protocol restriction for the MPC7450 is that any transaction receiving a simultaneous $\overline{\text{AACK}}$ and $\overline{\text{TA}}$/$\overline{\text{TEA}}$ must not be retried. Improperly forwarded data causes data corruption in the code stream. In addition, any transaction that requires a data tenure that follows a transaction receiving a simultaneous $\overline{\text{AACK}}$ and $\overline{\text{TA}}$/$\overline{\text{TEA}}$ must not be retried. When the MPC7450 receives a simultaneous $\overline{\text{AACK}}$ and $\overline{\text{TA}}$/$\overline{\text{TEA}}$, it sets an internal sticky flag that causes the next transaction to ignore $\overline{\text{ARTRY}}$.

For revisions of the Tsi107 before Rev 1.4, data is returned to the processor starting with the cycle when $\overline{\text{AACK}}$ is asserted, which is one cycle before that permitted by the MPC7450. Before Rev 1.4, the Tsi107 may drive $\overline{\text{DBG}}$*n* (and $\overline{\text{DBGLB}}$) as early as the cycle in which $\overline{\text{TS}}$ is asserted.

The problem is aggravated in dual-processor systems and systems where PCI accesses to memory cause significant snoop or retry activity on the 60x bus where 60x bus traffic is high.

Beginning with Rev 1.4, the Tsi107 no longer issues the first $\overline{\text{TA}}$ (or $\overline{\text{TEA}}$) for a data tenure simultaneously with the associated $\overline{\text{AACK}}$ for any transactions. To guarantee that $\overline{\text{TA}}$ is not asserted on or before $\overline{\text{AACK}}$, the timings for $\overline{\text{DBG}}$*n* and $\overline{\text{DBGLB}}$ were also changed.

3.2.1 Local Bus Slave Parameters

To implement the fix for MPC7450 compatibility, two local bus slave parameters, PICR1[CF_LBA_EN] and PICR2[CF_LBCLAIM_WS], were eliminated beginning with Rev 1.4. The CF_LBA_EN parameter enables or disables the local bus slave functionality on revisions before Rev 1.4, whereas, starting with Rev 1.4, local bus slave functionality is always enabled.

The CF_LBCLAIM_WS parameter controls when the Tsi107 samples the $\overline{\text{LBCLAIM}}$ input signal from the local bus slave on revisions before 1.4. Starting with Rev 1.4 of the Tsi107, the PICR2[CF_APHASE_WS] parameter controls the timing of both the address phase and the sampling of $\overline{\text{LBCLAIM}}$.

3.3 Latency for PCI Accesses to Local Memory

Due to a chip errata on revisions of the Tsi107 before Rev 1.4, the processor can prevent a PCI agent or DMA transfer from accessing the SDRAM. This affects the minimum PCI and/or DMA access latency if the processor is performing a series of pipelined reads or writes. PCI and DMA accesses to local memory may stall if snooping is disabled (PICR2[NO_SNOOP_EN] = 1) because pipelined processor transactions have a priority 1.5 (see the *Tsi107 User Manual*). The suggested work-around is to enable snooping (PICR2[NO_SNOOP_EN] = 1), even though the hardware-managed coherency is not needed. As an additional step, in single-processor systems, the $\overline{\text{GBL}}$ signal to the processor may be pulled down to eliminate false $\overline{\text{ARTRY}}$s due to pipeline collisions.

The solution implemented in Rev 1.4 of the Tsi107 is to add fairness to the internal arbitration logic that does not allow the pipelined 60x transaction to keep winning over non-snooped PCI/DMA initiated read transactions.

3.4 60x Bus Grants After sync or eieio Broadcasts

Due to a chip errata on Tsi107 devices before Rev 1.4, if the processor issues a **sync** or **eieio** instruction to the Tsi107, the Tsi107 does not grant the 60x bus to any processor until all the internal write buffers are empty. These buffers are the processor-to-PCI-write data buffers (PRPWB0 and PRPWB1), the PCI-to-local-memory-write buffers (PCMWB0, and PCMWB1), and the copyback buffer.

In this case, a PCI device can perform continuous accesses into SDRAM so that the internal buffers (PCMWB0, PCMWB1, and copyback) are never empty. In such a case, the processor is prevented from progressing beyond the **sync**/**eieio** address broadcast.

The suggested work-around is to disable broadcasts of address-only transactions (HID0[ABE]=0) on processors that implement the ABE bit. For systems using processors that do not implement the ABE bit (such as the MPC7410), the work-around is much more difficult, involving external logic that decodes address-only broadcasts and inhibits the PCI arbitration signals to allow for transactions in the internal PCMWBs buffers to complete to memory before resuming normal operation.

The solution implemented in Rev 1.4 of the Tsi107 is to remove the dependency on flushing the PCI-to-local-memory-write buffers (PCMWBs) after a **sync**/**eieio** broadcast before the Tsi107 can grant the bus to the processor. Thus, only the processor-to-PCI-write buffers (PRPWBs) are flushed before the bus is granted to the processor.

4 Compatibility Factors

This section describes compatibility issues that may arise when migrating a Tsi107-based design from Rev 1.3 to Rev 1.4.

4.1 $\overline{\text{DBG}n}$ and $\overline{\text{DBGLB}}$ Timing

As described in Section 3.2, “MPC7450 Compatibility,” to guarantee that $\overline{\text{TA}}$ is not asserted on or before $\overline{\text{AACK}}$, the timings for $\overline{\text{DBG}n}$ and $\overline{\text{DBGLB}}$ were changed in Rev 1.4 to fix the MPC7450-compatibility problem. Before Rev 1.4, the Tsi107 may drive $\overline{\text{DBG}n}$ (and $\overline{\text{DBGLB}}$) as early as the cycle in which $\overline{\text{TS}}$ is asserted. Figure 1 shows the signal timing for $\overline{\text{DBG}n}$ and $\overline{\text{DBGLB}}$ on Rev 1.3 and Rev 1.4 devices.

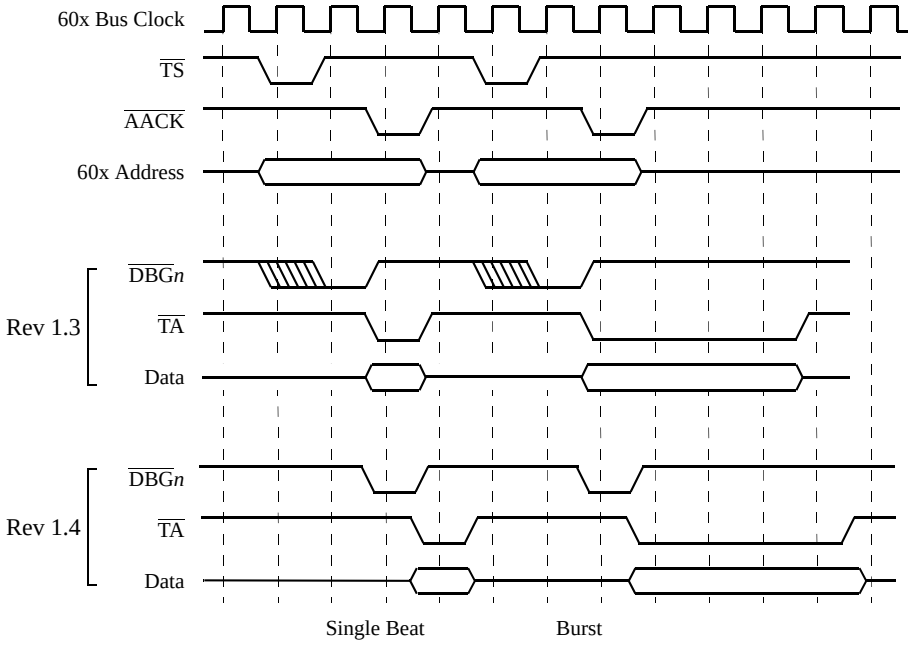

Figure 1. Rev 1.3 and Rev 1.4 $\overline{\text{DBG}n}$ Signal Timing

NOTE

For Rev 1.4 of the Tsi107, $\overline{\text{DBG}n}$ is asserted coincident with $\overline{\text{AACK}}$. If a Rev 1.3 system design incorporates external logic that depends on the timing of $\overline{\text{DBG}n}$ or $\overline{\text{DBGLB}}$, the external logic must be modified to accommodate the altered timing of Rev 1.4.

4.2 Local Bus Slave Compatibility

As described in Section 3.2.1, “Local Bus Slave Parameters,” an impact occurs on local bus slave functionality when moving from Rev 1.3 to Rev 1.4. Two local bus slave parameters, PICR1[CF_LBA_EN] and PICR2[CF_LBCLAIM_WS] were eliminated

Even though the CF_LBA_EN parameter was eliminated in Rev 1.4, initialization software that sets this bit to enable the local bus slave functionality do not cause any errors. Software that clears CF_LBA_EN to disable the

local bus slave functionality does not cause any errors; however, the functionality is always enabled in Rev 1.4 and the clearing of this bit is ignored. A Rev 1.3 design has no reason to rely on disabling the local bus slave functionality, and thus software should not be impacted.

The elimination of the CF_LBCLAIM_WS parameter in Rev 1.4 may affect initialization software. Starting with Rev 1.4 of the Tsi107, the PICR2[CF_APHASE_WS] parameter controls the timing of both the address phase and the sampling of $\overline{\text{LBCLAIM}}$. Software that attempts to program CF_LBCLAIM_WS does not cause any errors on Rev 1.4, but the $\overline{\text{LBCLAIM}}$ sampling logic ignores the parameter. Consider this situation to assert $\overline{\text{LBCLAIM}}$ in the appropriate cycle.

Many customers use equal settings for CF_APHASE_WS and CF_LBCLAIM_WS, and the change does not affect them. However, if the initialization code is setting CF_APHASE_WS greater than CF_LBCLAIM_WS and a local bus slave asserts $\overline{\text{LBCLAIM}}$ before CF_APHASE_WS expires, a Rev 1.4 Tsi107 does not recognize the assertion of $\overline{\text{LBCLAIM}}$ and asserts the appropriate number of $\overline{\text{TA}}$s for the transaction. Typically in this situation, the system eventually hangs. The work-around is to adjust CF_APHASE_WS for a shorter duration to accommodate the assertion of $\overline{\text{LBCLAIM}}$ or to modify the local bus slave to delay the assertion of $\overline{\text{LBCLAIM}}$ until CF_APHASE_WS expires.

4.3 Migrating from 100 MHz to 133 MHz

If the purpose of migrating to Rev 1.4 is to increase the processor/memory bus frequency from 100 MHz to 133 MHz, the system design must account for the electrical differences that Table 2 describes. Note that not all Rev 1.4 devices are rated for 133-MHz operation. In 133-MHz systems, use only those devices that are specifically rated for 133-MHz operation.

Most, but not necessarily all, system designs should be re-laid out to operate properly at 133 MHz. Because the 133-MHz Rev 1.4 Tsi107 requires 2.7 V_{DC} supply voltages for the core, PLL, and DLL, the power supply of an existing Rev 1.3 design should be augmented to support the additional increased supply voltage. Follow the recommendations in the Tsi107 *Hardware Specification* and in the *Tsi107 Design Guide* concerning memory timing. In general, for best signal integrity, keep trace lengths for SDRAM signals as short as possible and keep capacitive loads to a minimum (or use registered DIMMs that buffer the memory control signals).

5 Conclusion

Table 3 provides a summary of which revision of the Tsi107 is appropriate for specific design requirements. For designs that do not depend on the listed requirements, either revision provides the functionality described in the *Tsi107 User Manual*.

Table 3. Which Revision To Use?

Design Requirement	Tsi107 Rev 1.3	Tsi107 Rev 1.4
133-MHz processor/memory bus	Not suitable	Suitable (with 133 MHz-rated part)
External PCI masters that may run Type 2 fast-back-to-back transactions	May not be suitable	Suitable, but fast back-to-back transactions to the Tsi107 are still not supported. See Section 3.1, “Fast Back-to-Back Capability,” for more information.
MPC7450 family processor	Not-suitable	Suitable
Local bus slave device	Suitable	Existing logic/initialization software may need modification. See Section 4.2, “Local Bus Slave Compatibility,” for more information.
External logic that relies on $\overline{\text{DBG}n}$ or $\overline{\text{DBGLB}}$ timing	Suitable	Existing logic may need modification. See Section 4.1, “DBGn and DBGLB Timing,” for more information.
Snooping of PCI-to-local memory transactions disabled (PICR2[NO_SNOOP_EN] = 1)	May not be suitable	Suitable
MPC7400/MPC7410 processor	May not be suitable	Suitable

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