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H8/300L SLP Series

Transition to Subactive Mode

Introduction

This sample task shows an example of making transition to the subactive mode. The system enters the watch mode by executing a SLEEP instruction in the high-speed active mode. In the watch mode, an interrupt is generated on the $\overline{\text{IRQ0}}$ pin, which causes the system to enter the subactive mode. The system then goes back to the high-speed active by executing a SLEEP instruction.

Target Device

H8/38024

Contents

1. Specifications

1. This sample task shows an example of making transition to the subactive mode.
2. The system goes to the watch mode by executing a SLEEP instruction in the high-speed active mode.
3. In the watch mode, an $\overline{\text{IRQ0}}$ interrupt is generated when switch 0 (SW0), connected to the $\overline{\text{IRQ0}}$ pin, is turned on. Upon this interrupt, the system leaves the watch mode and enters the subactive mode.
4. In the subactive mode, a Timer A interrupt request is generated every 0.5 sec. Through Timer A interrupt handling, an LED is controlled to be turned on and off alternately every 0.5 sec.
5. In the subactive mode, an $\overline{\text{IRQ1}}$ interrupt is generated when switch 1 (SW1), connected to the $\overline{\text{IRQ1}}$ pin, is turned on. After the $\overline{\text{IRQ1}}$ interrupt handling is completed, the system makes a direct transition to the high-speed active mode by executing a SLEEP instruction.
6. The LED is connected to the P92 output pin of port 9.
7. P92 is a large-current port.
8. Figure 1.1 shows an example of connecting switches 1 and 0 to the $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ pins.

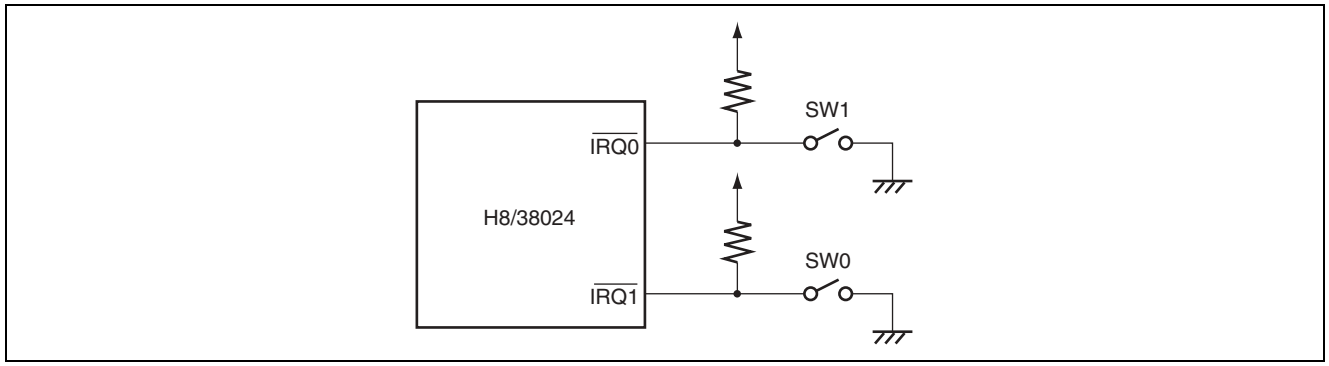


Figure 1.1 Example of Switch Connection for Making Transition to Subactive Mode

2. Description of Functions

1. In this sample task, the operating mode is changed to the subactive mode, a power down mode. Figure 2.1 shows a mode transition diagram to the subactive mode. The function of the subactive mode is described below.
   - The mode changes to the subactive mode when an interrupt (Timer A, Timer F, Timer G, IRQ0 or WKP7 to WKP0) is generated in the watch mode while LSON in SYSCR1 is set to 1. Or the mode changes to the subactive mode when an interrupt (Timer A, Timer C, Timer F, Timer G, SCI3, IRQ4, IRQ3, IRQ1, IRQ0, IRQAEC, WKP7 to WKP0, or AEC) is generated in the subsleep mode.
   - If the I bit in CCR is 1, or an acceptance of interrupts is disabled by the interrupt enable register, the mode does not change to the subactive mode.
   - The subactive mode is terminated by a SLEEP instruction or $\overline{\text{RES}}$ pin input.
   - When a SLEEP instruction is executed while SSBY in SYSCR1 is set to 1 and TMA3 in TMA is set to 1, the subactive mode is terminated and a transition is made to the watch mode.
   - By SLEEP instruction, direct transition to the high-speed active mode is also possible.
   - In the case of terminating the subactive mode by $\overline{\text{RES}}$ pin, the oscillation of the system clock starts when the $\overline{\text{RES}}$ pin is driven "Low". When the $\overline{\text{RES}}$ pin is driven "High" after the specified oscillation stabilization time has elapsed, the CPU starts reset exception handling. It should be noted that the system clock is supplied to the entire LSI at the moment the system clock oscillation has started. The $\overline{\text{RES}}$ pin must be kept "Low" until the oscillation of the system clock stabilizes.
   - The oscillation stabilization time after the termination of subactive mode is set by STS2 to STS0 in SYSCR1.
   - In this sample task, the oscillation stabilization time is set to 1.638 ms.

— The CPU operates in three modes to execute programs, namely, the high-speed active mode, medium-speed active mode and subactive mode. A direct transition is a transition between these three operation modes which is made without stopping the program execution. A direct transition is made by setting DTON in SYSCR2 to 1 and executing a SLEEP instruction. After a direct transition, direct transition interrupt exception handling starts. If direct transition interrupts are disabled by the interrupt enable register 2, the mode changes to the sleep mode or watch mode instead. If the direct transition is attempted while the I bit in CCR is set to 1, the mode changes to the sleep mode or watch mode, and the mode cannot be terminated by an interrupt.

— A direct transition from the subactive mode to the high-speed active mode takes place when a SLEEP instruction is executed in the subactive mode while SSBY is set to 1 and LSON is set to 0 in SYSCR1, MSON is set to 0 and DTON is set to 1 in SYSCR2, and TMA3 in TMA is set to 1. The mode changes directly to the high-speed active mode via the watch mode after the time set by STS2 to STS0 in SYSCR1 has elapsed.

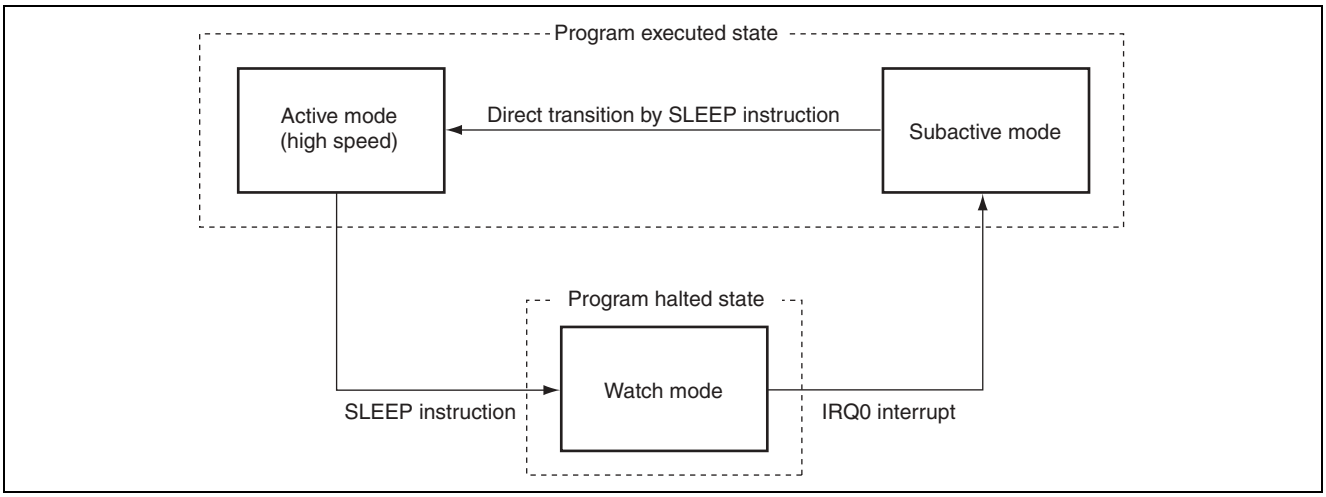


Figure 2.1 Mode Transition from/to Subactive Mode

2. Table 2.1 shows the assignment of functions in this sample task. Transition to the subactive mode is performed by assigning the functions as shown in table 2.1.

Table 2.1 Function Assignment

Function	Assignment
PSW	A 5-bit up counter using the subclock (32.768 kHz) / 4 as input.
SYSCR1	Controls power down modes.
SYSCR2	Controls power down modes.
PDR9	P92 output pin data storage
P92	LED output
IEG1	Selects $\overline{\text{IRQ1}}$ pin input edge
IEG0	Selects $\overline{\text{IRQ0}}$ pin input edge
IENTA	Enables or disables Timer A interrupt requests.
IENI1	Enables or disables IRQ1 interrupt requests.
IENI0	Enables or disables IRQ0 interrupt requests.
IENDT	Enables direct transition interrupt requests
IRRTA	Indicates whether a Timer A interrupt has been requested.
IRRI1	Indicates whether an IRQ1 interrupt has been requested.
IRRI0	Indicates whether an IRQ0 interrupt has been requested.
IRRDT	Indicates whether a direct transition interrupt has been requested.
$\overline{\text{IRQ1}}$	Switch 1 input
$\overline{\text{IRQ0}}$	Switch 0 input

3. Principle of Operation

1. Figure 3.1 illustrates the operation of this sample task. Transition to the subactive mode is made through hardware and software processing as shown in the figure.

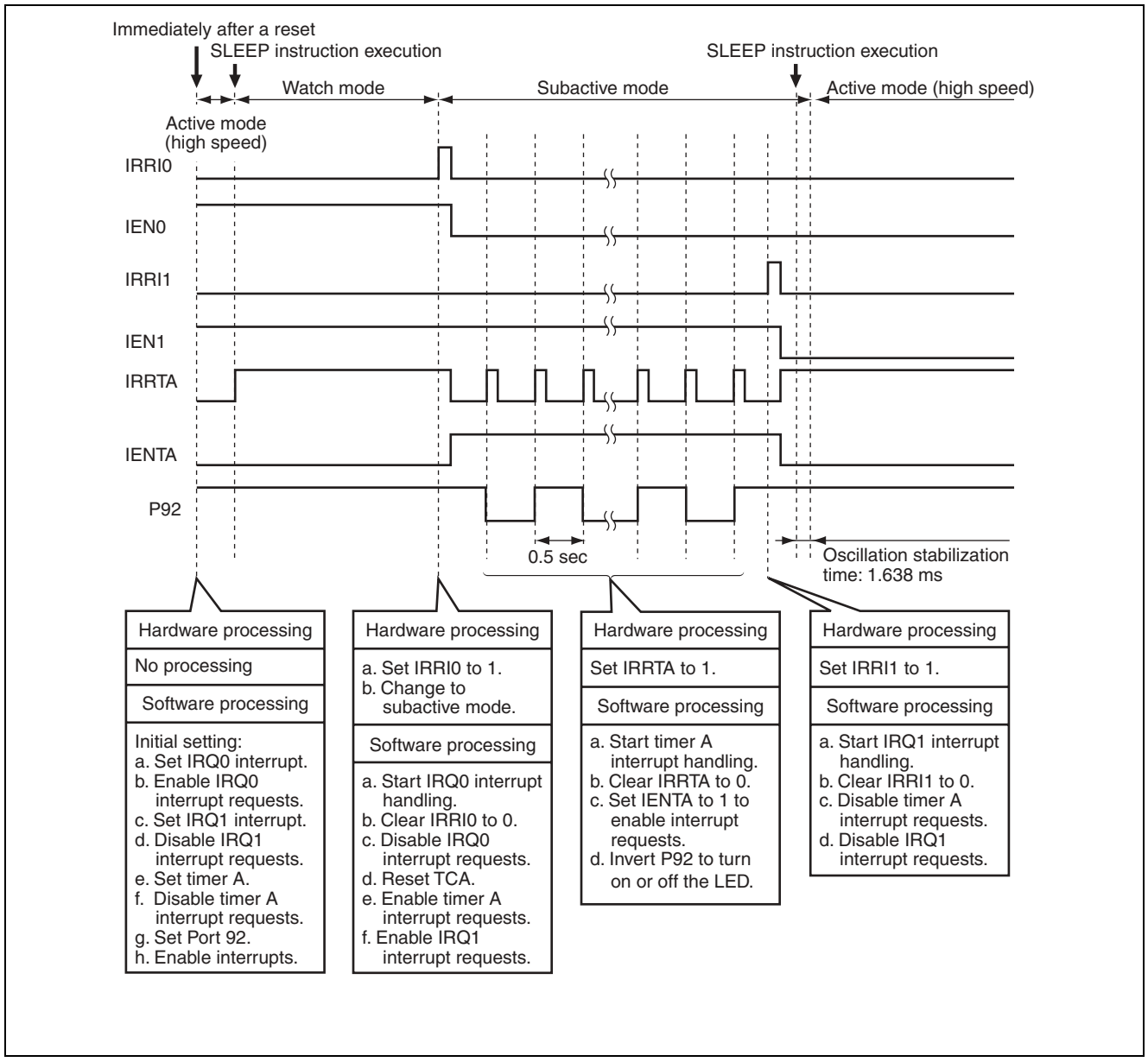


Figure 3.1 Operation Principle of Making Transition to Subactive Mode

4. Description of Software

4.1 Modules

The modules used in this sample task are shown in table 4.1.

Table 4.1 Description of Modules

Module	Label	Function
Main routine	main	Makes settings for IRQ0, IRQ1, and Timer A interrupts and port 9, enables interrupts, and makes transitions to the watch mode and active mode.
Switch 1 ON	irq1int	An IRQ1 interrupt handling routine which sets SWONF and disables Timer A and IRQ1 interrupt requests.
Switch 0 ON	irq0int	An IRQ1 interrupt handling routine which disables IRQ0 interrupt requests.
LED control	taint	A Timer A interrupt handling routine which enables interrupt requests and controls the LED.
Direct transition	dtint	A direct transition interrupt handling routine which clears the direct transition interrupt request flag.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

Table 4.2 shows the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
TMA		Timer Mode Register A If TMA = H'19, Timer A function is set to the clock time-based function and TCA overflow period is set to 0.5 sec.	H'FFB0	H'19
TCA		Timer Counter A An 8-bit up counter which overflows every 0.5 sec by the clock time-base function and uses PSW output clock as input.	H'FFB1	H'00
PDR9	P92	Port Data Register 9 (Port Data Register 92) If P92 = 0, the output level on P92 pin is "Low". If P92 = 1, the output level on P92 pin is "High".	H'FFDC Bit 2	1
PMR2	IRQ0	Port mode Register 2 (IRQ0 I/O Port Select) If IRQ0 = 0, $\overline{\text{IRQ0}}$ pin functions as a general I/O port. If IRQ0 = 1, $\overline{\text{IRQ0}}$ pin functions as $\overline{\text{IRQ0}}$ input pin.	H'FFC9 Bit 0	1
PMRB	IRQ1	Port mode Register B (IRQ1 I/O Port Select) If IRQ1 = 0, $\overline{\text{IRQ1}}$ pin functions as a general I/O port. If IRQ1 = 1, $\overline{\text{IRQ1}}$ pin functions as $\overline{\text{IRQ1}}$ input pin.	H'FFEE Bit 3	1
IEGR	IEG1	IRQ Edge Select Register (IRQ1 Edge Select) If IEG1 = 0, falling edge of $\overline{\text{IRQ1}}$ pin input is detected. If IEG1 = 1, rising edge of $\overline{\text{IRQ1}}$ pin input is detected.	H'FFF2 Bit 1	0
	IEG0	IRQ Edge Select Register (IRQ0 Edge Select) If IEG0 = 0, falling edge of $\overline{\text{IRQ0}}$ pin input is detected. If IEG0 = 1, rising edge of $\overline{\text{IRQ0}}$ pin input is detected.	H'FFF2 Bit 0	0

Register		Function	Address	Setting
IENR1	IENTA	Interrupt Enable Register 1 (Timer A Interrupt Enable) If IENTA = 0, Timer A interrupt requests are disabled. If IENTA = 1, Timer A interrupt requests are enabled.	H'FFF3 Bit 7	1
	IEN1	Interrupt Enable Register 1 (IRQ1 Interrupt Enable) If IEN1 = 0, $\overline{\text{IRQ1}}$ pin interrupt requests are disabled. If IEN1 = 1, $\overline{\text{IRQ1}}$ pin interrupt requests are enabled.	H'FFF3 Bit 1	1
	IEN0	Interrupt Enable Register 1 (IRQ0 Interrupt Enable) If IEN0 = 0, $\overline{\text{IRQ0}}$ pin interrupt requests are disabled. If IEN0 = 1, $\overline{\text{IRQ0}}$ pin interrupt requests are enabled.	H'FFF3 Bit 0	1
IENR2	IENDT	Interrupt Enable Register 2 (Direct Transition Interrupt Enable) If IENDT = 0, direct transition interrupt requests are disabled. If IENDT = 1, direct transition interrupt requests are enabled.	H'FFF4 Bit7	1
SYSCR1	SSBY	System Control Register 1 (Software Standby) If SSBY = 1, a transition is made to the standby mode or watch mode after a SLEEP instruction is executed in the active mode. A transition is made to the subsleep mode after a SLEEP instruction is executed in the subactive mode.	H'FFF0 Bit 7	1
	STS2 STS1 STS0	System Control Register 1 (Standby Timer Select 2, 1, 0) If STS2 = 0, STS1 = 0, and STS0 = 0, oscillation stabilization time after the termination of watch mode is set to 1.638 ms.	H'FFF0 Bit 6 Bit 5 Bit 4	STS2 = 0 STS1 = 0 STS0 = 0
	LSON	System Control Register 1 (Low Speed ON Flag) If LSON = 0, the CPU operating clock is set to the system clock after the watch mode is terminated. If LSON = 1, the CPU operating clock is set to the subsystem clock after the watch mode is terminated.	H'FFF0 Bit 3	1
SYSCR2	DTON	System Control Register 2 (Direct Transfer ON Flag) If DTON = 0, a transition is made to the standby, watch or sleep mode when a SLEEP instruction is executed in the active mode. a transition is made to the watch or subsleep mode when a SLEEP instruction is executed in the subactive mode. If DTON = 1, a direct transition is made to the high-speed active mode (when SSBY = 1, TMA3 = 1,LSON = 0, MSON = 0) or to the medium-speed active mode (when SSBY = 1, TMA3 = 1, LSON = 0, MSON = 1) when a SLEEP instruction is executed in the subactive mode.	H'FFF1 Bit 3	1

Register		Function	Address	Setting
SYSCR2	MSON	System Control Register 2 (Medium Speed ON Flag) If MSON = 0, the system operates in the high-speed active mode after the standby, watch or sleep mode is terminated. The system operates in the high-speed sleep mode if a SLEEP instruction is executed in the active mode. If MSON = 1, the system operates in the medium-speed active mode after the standby, watch or sleep mode is terminated. The system operates in the medium-speed sleep mode if a SLEEP instruction is executed in the active mode.	H'FFF1 Bit 2	0
	SA1 SA0	System Control Register 2 (Subactive Mode Clock Select 1, 0) If SA1 = 0 and SA0 = 0, the CPU operating clock in the subactive mode is set to ϕ_w/8.	H'FFF1 Bit 1 Bit 0	SA1 = 0 SA0 = 0
IRR1	IRRTA	Interrupt Request Register 1 (Timer A Interrupt Request Flag) If IRRTA = 0, Timer A interrupt is not requested. If IRRTA = 1, Timer A interrupt has been requested.	H'FFF6 Bit 7	0
	IRRI1	Interrupt Request Register 1 (IRQ1 Interrupt Request Flag) If IRRI1 = 0, $\overline{IRQ1}$ interrupt is not requested. If IRRI1 = 1, $\overline{IRQ1}$ interrupt has been requested.	H'FFF6 Bit 1	0
	IRRI0	Interrupt Request Register 1 (IRQ0 Interrupt Request Flag) If IRRI0 = 0, $\overline{IRQ0}$ interrupt is not requested. If IRRI0 = 1, $\overline{IRQ0}$ interrupt has been requested.	H'FFF6 Bit 0	0
IRR2	IRRDT	Interrupt Request Register 2 (Direct Transition Interrupt Request Flag) If IRRDT = 0, direct transition interrupt is not requested. If IRRDT = 1, direct transition interrupt has been requested.	H'FFF7 Bit 7	0

4.4 Description of RAM

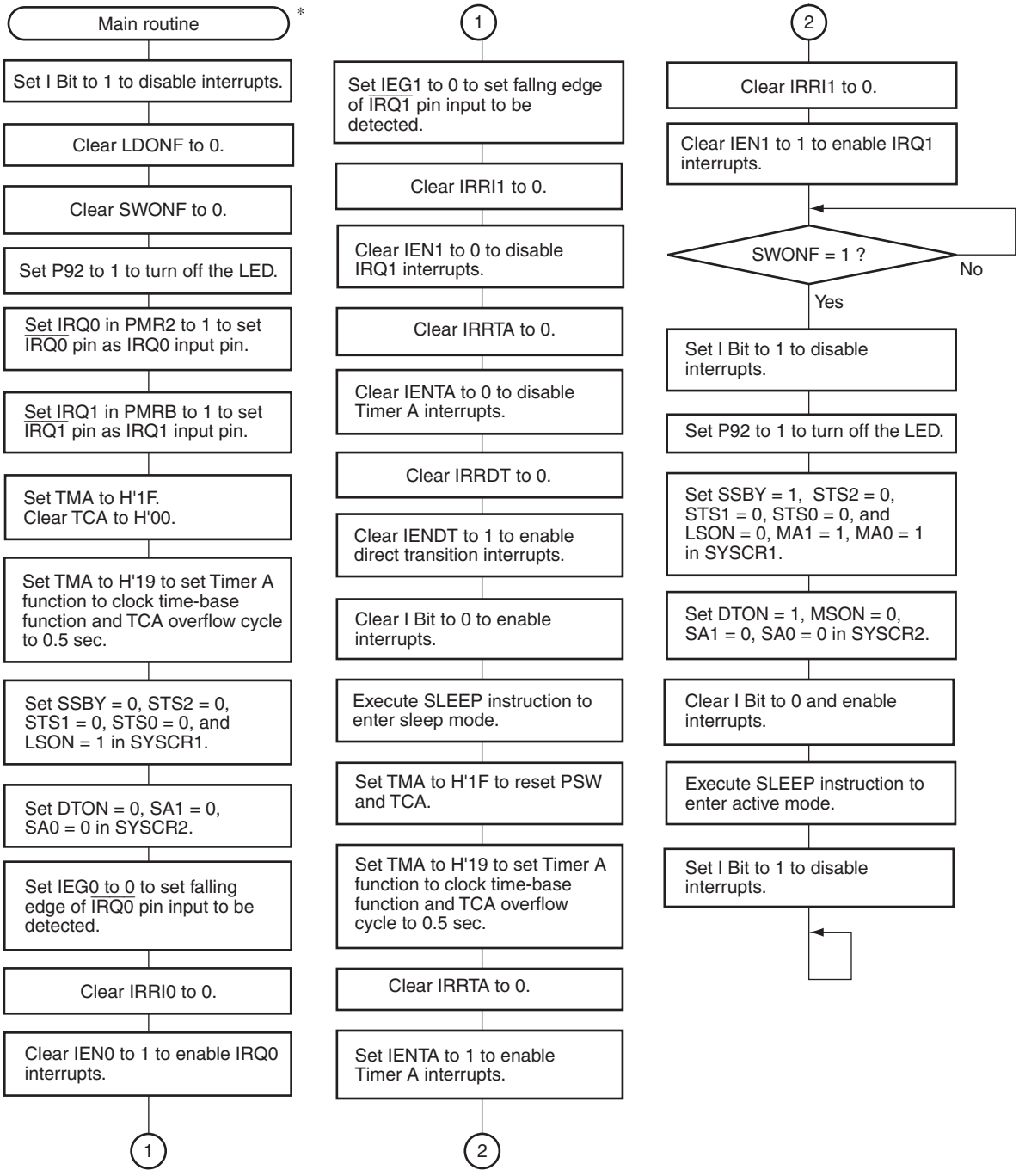
Table 4.3 describes the RAM area used in this sample task.

Table 4.3 Description of RAM

Label		Function	Address	Used in
USRF	SWONF	Flag to judge whether the switch 1 input is on or off.	H'FB80 Bit 1	Main routine Switch 1 ON
	LDONF	Flag to judge whether the LED is on or off.	H'FB80 Bit 0	LED control

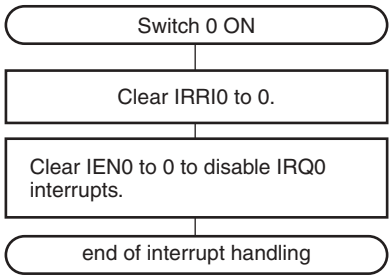
5. Flowchart

1. Main routine

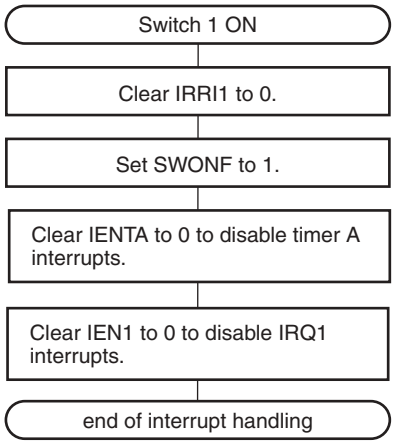


Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

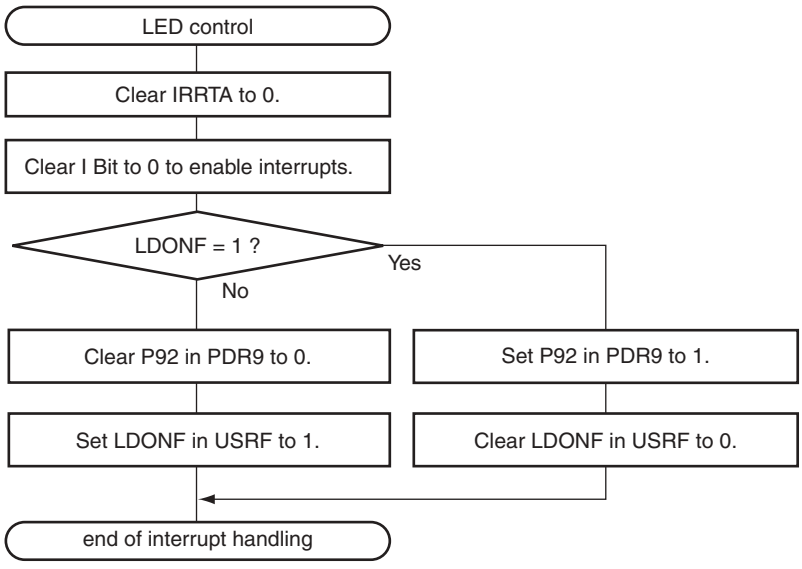
2. IRQ0 interrupt handling routine



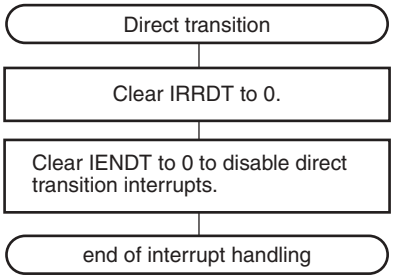
3. IRQ1 interrupt handling routine



4. Timer A interrupt handling routine



5. Direct transition interrupt handling routine



6. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Transition to Subactive Mode'                                                                                      */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Power-Down Mode                                                                                                   */
/*     Subactive Mode                                                                                                   */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0       /* Timer Mode Register A                */
#define     TCA         *(volatile unsigned char *)0xFFB1       /* Timer Counter A                      */
#define     PMR2_BIT    (*(struct BIT *)0xFFC9)                 /* Port Mode Register 2                 */
#define     IRQ0        PMR2_BIT.b0                             /* Port Mode Register 2 bit0            */
#define     PDR9_BIT    (*(struct BIT *)0xFFDC)                 /* Port Data Register 9                 */
#define     P92         PDR9_BIT.b2                             /* Port Data Register 92                */
#define     PMRB_BIT    (*(struct BIT *)0xFFEE)                 /* Port Mode Register B                 */
#define     IRQ1        PMRB_BIT.b3                             /* Port Mode Register B bit3            */
#define     SYSCR1      *(volatile unsigned char *)0xFFF0       /* System Control Register 1            */
#define     SYSCR1_BIT  (*(struct BIT *)0xFFF0)                 /* System Control Register 1            */
```

```
#define     SSBY        SYSCR1_BIT.b7                       /* Software Standby                         */
#define     STS2        SYSCR1_BIT.b6                       /* Standby Timer Select 2                   */
#define     STS1        SYSCR1_BIT.b5                       /* Standby Timer Select 1                   */
#define     STS0        SYSCR1_BIT.b4                       /* Standby Timer Select 0                   */
#define     LSON        SYSCR1_BIT.b3                       /* Low Speed On Flag                        */
#define     MA1         SYSCR1_BIT.b1                       /* Active Mode Clock Select 1               */
#define     MA0         SYSCR1_BIT.b0                       /* Active Mode Clock Select 0               */
#define     SYSCR2      *(volatile unsigned char *)0xFFF1   /* System Control Register 2                */
#define     SYSCR2_BIT  (*(struct BIT *)0xFFF1)             /* System Control Register 2                */
#define     NESEL       SYSCR2_BIT.b4                       /* Noise Elimination Sampling               */
                                                            /*                          Frequency Select */
#define     DTON        SYSCR2_BIT.b3                       /* Direct Transfer On Flag                  */
#define     MSON        SYSCR2_BIT.b2                       /* Middle Speed On Flag                     */
#define     SA1         SYSCR2_BIT.b1                       /* Subactive Mode Clock Select 1            */
#define     SA0         SYSCR2_BIT.b0                       /* Subactive Mode Clock Select 0            */
#define     IEGR_BIT    (*(struct BIT *)0xFFF2)             /* Interrupt Edge Select Register 1         */
#define     IEG1        IEGR_BIT.b1                         /* IRQ1 Edge Select                         */
#define     IEG0        IEGR_BIT.b0                         /* IRQ0 Edge Select                         */
#define     IENR1_BIT   (*(struct BIT *)0xFFF3)             /* Interrupt Enable Register 1              */
#define     IENTA       IENR1_BIT.b7                        /* Timer A Interrupt Enable                 */
#define     IEN1        IENR1_BIT.b1                        /* IRQ1 Interrupt Request Enable            */
#define     IEN0        IENR1_BIT.b0                        /* IRQ0 Interrupt Request Enable            */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 1              */
#define     IENDT       IENR2_BIT.b7                        /* Direct Transfer Interrupt Enable         */
#define     IRR1_BIT    (*(struct BIT *)0xFFF6)             /* Interrupt Request Register 1             */
#define     IRRTA       IRR1_BIT.b7                         /* Timer A Interrupt Request Flag           */
#define     IRRI1       IRR1_BIT.b1                         /* IRQ1 Interrupt Request Flag              */
#define     IRRI0       IRR1_BIT.b0                         /* IRQ0 Interrupt Request Flag              */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 1             */
#define     IRRDT       IRR2_BIT.b7                         /* Direct Transfer Interrupt Request Flag   */

#pragma interrupt   (dtint)
#pragma interrupt   (irq0int)
#pragma interrupt   (irq1int)
#pragma interrupt   (taint)
/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );
void        dtint ( void );
void        irq0int ( void );
void        irq1int ( void );
void        taint ( void );

/************************************************************************************************************/
/*  RAM define                                                                                              */
/************************************************************************************************************/
unsigned char   USRF;                                       /* User Flag Area                           */

#define     USRF_BIT    (*(struct BIT *)&USRF)
#define     SWONF       USRF_BIT.b1                         /* Switch On  Flag                          */
#define     LDONF       USRF_BIT.b0                         /* LED On Flag                              */
```

```
/*****************************************************************************************************************/
/*  Vector Address                                                                                               */
/*****************************************************************************************************************/
#pragma section     V1                                          /* Vector Section Set                        */
void (*const VEC_TBL1[])(void) = {
    INIT                                                        /* 0x0000 - 0x000F                           */
};
#pragma section     V2                                          /* Vector Section Set                        */
void (*const VEC_TBL2[])(void) = {
    irq0int                                                     /* 0x0008 IRQ0 Interrupt Vector              */
};
#pragma section     V3                                          /* Vector Section Set                        */
void (*const VEC_TBL3[])(void) = {
    irq1int                                                     /* 0x000A IRQ1  Interrupt Vector             */
};
#pragma section     V4                                          /* Vector Section Set                        */
void (*const VEC_TBL4[])(void) = {
    taint                                                       /* 0x0016 timer A  Interrupt Vector          */
};
#pragma section     V5                                          /* Vector Section Set                        */
void (*const VEC_TBL5[])(void) = {
    dtint                                                       /* 0x0028 Sleep Interrupt Vector             */
};

#pragma section                                                 /* P                                         */
/*****************************************************************************************************************/
/*  Main Program                                                                                                 */
/*****************************************************************************************************************/
void    main ( void )
{
    set_imask_ccr(1);                                           /* Interrupt Disable                         */

    LDONF = 0;                                                  /* Initialize LDONF                          */
    SWONF = 0;                                                  /* Initialize SWONF                          */

    P92 = 1;                                                    /* Initialize P92                            */

    IRQ1 = 1;                                                   /* Initialize IRQ1 Terminal Input            */
    IRQ0 = 1;                                                   /* Initialize IRQ0 Terminal Input            */

    TMA = 0x1F;                                                 /* Reset PSW & TCA                           */
    TMA = 0x19;                                                 /* Set TMA3                                  */
    SYSCR1 = 0x8F;                                              /* Initialize Function of Sleep Mode 1       */
    SYSCR2 = 0xE0;                                              /* Initialize Function of Sleep Mode 2       */

    IEG0 = 0;                                                   /* Initialize IRQ0 Terminal Input Edge       */
    IRRI0 = 0;                                                  /* Clear IRRI0                               */
    IEN0 = 1;                                                   /* IRQ0 Interrupt Enable                     */

    IEG1 = 0;                                                   /* Initialize IRQ1 Terminal Input Edge       */
    IRRI1 = 0;                                                  /* Clear IRRI1                               */
    IEN1 = 0;                                                   /* IRQ1 Interrupt Disable                    */

    IRRTA = 0;                                                  /* Clear IRRTA                               */
    IENTA = 0;                                                  /* Timer A Interrupt Disable                 */

    IRRDT = 0;                                                  /* Clear IRRDT                               */
    IENDT = 1;                                                  /* Direct Transfer Interrupt Enable          */
```

```
    set_imask_ccr(0);                                   /* Interrupt Enable                         */

    sleep();                                            /* Transition to Sleep Mode                 */

    TMA = 0x1F;                                         /* Reset PSW & TCA                          */
    TMA = 0x19;                                         /* Initialize Timer A Function              */

    IRRTA = 0;                                          /* Clear IRRTA                              */
    IENTA = 1;                                          /* Timer A Interrupt Enable                 */

    IRRI1 = 0;                                          /* Clear IRRI1                              */
    IEN1 = 1;                                           /* IRQ1 Interrupt Enable                    */

    while(SWONF ! = 1){                                 /* SWONF = "1" ?                            */
        ;
    }
    set_imask_ccr(1);                                   /* Interrupt Disable                        */

    P92 = 1;                                            /* Turn off LED                             */

    SYSCR1 = 0x87;                                      /* Initialize Function of Active Mode 1     */
    SYSCR2 = 0xE8;                                      /* Initialize Function of Active Mode 2     */

    set_imask_ccr(0);                                   /* Interrupt Enable                         */
    sleep();                                            /* Transition to Active Mode                */
    set_imask_ccr(1);                                   /* Interrupt Disable                        */

    while(1){
        ;
    }
}

/*****************************************************************************************************************/
/*  IRQ0 Interrupt                                                                                               */
/*****************************************************************************************************************/
void    irq0int ( void )
{
    IRRI0 = 0;                                          /* Clear IRRI0                              */
    IEN0 = 0;                                           /* IRQ0 Interrupt Disable                   */
}

/*****************************************************************************************************************/
/*  IRQ1 Interrupt                                                                                               */
/*****************************************************************************************************************/
void    irq1int ( void )
{
    IRRI1 = 0;                                          /* Clear IRRI1                              */
    SWONF = 1;                                          /* Set SWONF                                */
    IENTA = 0;                                          /* Timer A Interrupt Disable                */
    IEN1 = 0;                                           /* IEN1 Interrupt Disable                   */
}
```

```
/*****************************************************************************************************************/
/*  Timer A Interrupt                                                                                            */
/*****************************************************************************************************************/
void    taint ( void )
{
    IRRTA = 0;                                          /* Clear IRRTA                          */

    set_imask_ccr(0);                                   /* Interrupt Enable                     */

    if(LDONF == 1){                                     /* LDONF = "1" ?                        */
        P92 = 1;                                        /* Turn on LED                          */
        LDONF = 0;                                      /* Clear LDONF                          */
    }
    else{
        P92 = 0;                                        /* Turn off LED                         */
        LDONF = 1;                                      /* Set LDONF                            */
    }
}

/*****************************************************************************************************************/
/*  Direct Transfer Interrupt                                                                                    */
/*****************************************************************************************************************/
void    dtint ( void )
{
    IRRDT = 0;                                          /* Clear IRRDT                          */
    IENDT = 0;                                          /* Direct Transfer Interrupt Enable     */
}
```

Link address specifications

Section Name	Address
CV1	H'0000
CV2	H'0008
CV3	H'000A
CV4	H'0016
CV5	H'0028
P	H'0100
B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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