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SH7262/SH7264 Group

Transferring Program to RAM (CPU Transfer)

Summary

This application note describes an example of transferring program to RAM using the software.

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

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1. Introduction

1.1 Specifications

Transfers the program from an external ROM to internal RAM by software, and executes the program on internal RAM.

1.2 Modules Used

• Cache

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz
	Bus clock: 72 MHz
	Peripheral clock: 36 MHz
Integrated Development	Renesas Technology Corp.
Environment	High-performance Embedded Workshop Ver.4.04.01
C compiler	Renesas Technology SuperH RISC engine Family
	C/C++ compiler package Ver.9.02 Release 00
Compiler options	Default setting in the High-performance Embedded Workshop
	(-cpu=sh2afpu -fpu=single -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -
	gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -
	infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Transferring Program to RAM (DMA Transfer)



2. Applications

The SH7264 CPU transfers program from an external ROM to internal RAM, and executes the program on internal RAM.

2.1 Section Alignment in the Sample Program

Use the compiler extended specifications #pragma section to change the section name of the program to transfer. The sample program changes the section of the transfer source program to PROM, and the section of the transfer destination program on internal RAM to PRAM. The following figure shows the memory map in the sample program.

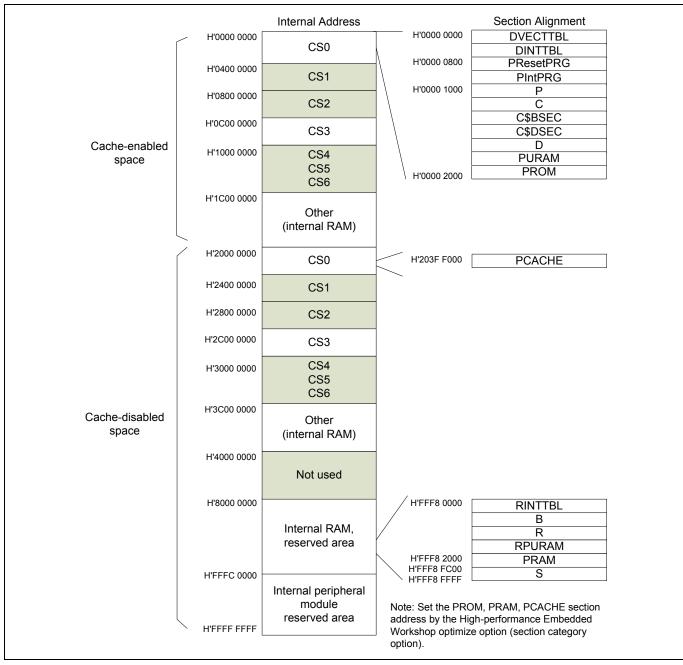


Figure 1 Memory Map



2.2 Linkage Editor Setting

Specify the section address by the linkage editor options. Table 1 lists sections to transfer in the sample program. Table 2 lists linkage editor options to use.

Table 1 Sections to Transfer

Section Name	Description
PROM	Transfer source
PRAM	Transfer destination

Note: When specifying the section address, select [Build] menu on the High-performance Embedded Workshop window, and open the [SuperH RISC engine Standard Toolchain] dialog box. For details, refer to the High-performance Embedded Workshop User's Manual.

Table 2 Linkage Editor Options

Option	Description
-rom=D=R,PROM=PRAM	Specifies ROM to RAM mapped sections
start=DVECTTBL,DINTTBL/00,PResetPRG,	Specifies a section starting address
PIntPRG/0800,P,C,C\$BSEC,C\$DSEC,D,PURAM	
PROM/01000, PRAM/01C000000, PCACHE/0203FF000,	
B,R,RPURAM/0FFF80000,	
S/0FFF8FC00	

2.3 Retrieving the Section Address

Use the section address operators listed in the following table to retrieve the section address in the program.

Table 3 Address Operators

Format	Description
sectop (" <section name=""> ")</section>	Refers to the starting address of the specified <section name="">.</section>
secend (" <section name=""> ")</section>	Refers to the end address +1 of the specified <section name="">.</section>
secsize (" <section name=""> ")</section>	Generates the size of the specified <section name="">.</section>

2.4 Sample Program Operation

The sample program uses software to transfer the section PROM size program from the section PROM starting address in CS0 space to the section PRAM allocated on internal RAM.

As the CPU transfers the program to the cache-enabled space while the operand cache (write back mode) is enabled, the program transferred may be fetched by the operand cache and the instruction fetch may not be executed. Write back the operand cache after transferring the program to the cache-enabled space by CPU.

To verify that this works, allocate a function using the compare match timer (io_blink_led function) to the section PROM, and transfers it on internal RAM. When the transfer is completed, the sample program executes the io_blink_led function.



2.5 Write Back the Operand Cache

The SH7264 operand cache can be read and programmed by MOV instruction. Access the operand cache address array to write back the operand cache. The address array for the operand cache is allocated from H'F080 0000 to H'F0FF FFFF. The data array for the operand cache is allocated from H'F180 0000 to H'F1FF FFFF.

When programming a cache line for which the U bit is 1 (data is programmed) and the V bit is 1 (the entry data is valid) in the operand cache address array, write back the cache line. How to write back the operand cache depends on the value of the associative bit (A bit).

• Non-associative Operation

When specifying A bit as 0, (non-associative operation), write back to the entry corresponding to the entry address and way specified.

Associative Operation

When specifying A bit as 1, (associative operation), write back to the entry of the way which has the same tag address with the tag address in cache corresponding to the specified entry address. Compares the tag addresses in 4 ways. Writes U bit and V bit in the entry matched, however, the tag address and LRU bit are not reflected in the entry. When addresses match in no ways, nothing is written.

Table 4 lists the overview of cache. Figure 2 shows the basic concept of searching cache. Figure 3 shows how to specify the memory-mapped cache access (operand cache).

Description			
Instruction cache: 8 KB			
Operand cache: 8 KB			
Instructions and data separated, 4-way set associative			
Way lock function Ways 2 and 3 can be locked (operand cache only)			
16 bytes			
128 entries/way			
Selectable from write-back or write-through modes			
LRU (Least Recently Used) algorithm			

Table 4 Cache Overview

Note: For details on cache, refer to the Cache chapter in the "SH7262 Group, SH7264 Group Hardware Manual".



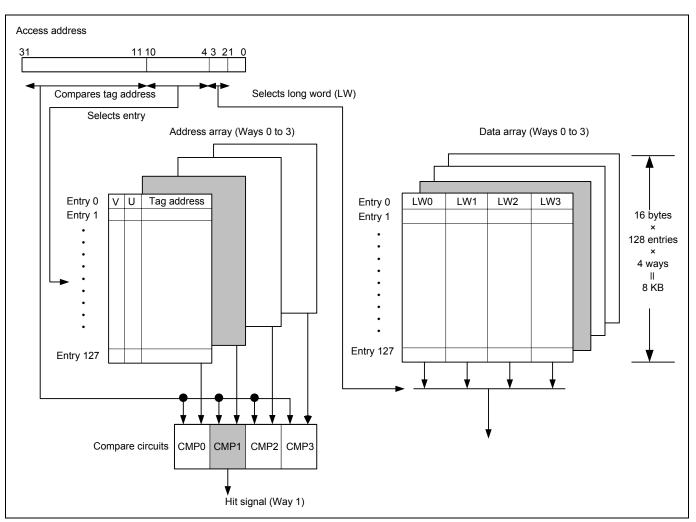


Figure 2 Basic Concept of Searching Cache



 Read address 	array							
	31	23 22	13 12 11 10		4 3 2 1 0			
Address	1 1 1 1 0 0 0	0 1	W	Entry address	0 - 0 0			
	<u></u>		· · · ·					
	31 29 28		11 10		4 3 2 1 0			
Data	0 0 0	Tag adress	E	LRU	0 0 U V			
	· · · · · ·				<u> </u>			
• Write in addres	ss array							
	31	23 22	13 12 11 10		4 3 2 1 0			
Address	1 1 1 1 0 0 0	0 1	W	Entry address	A — 0 0			
	31 29 28		11 10		4 3 2 1 0			
Data	0 0 0	Tag address	-	LRU	U V			
 Access data ar 	ray (Common for read	ng and writing)						
	31	23 22	13 12 11 10		4 3 2 1 0			
Address	1 1 1 1 0 0 0) 1 1	W	Entry address	L 0 0			
	• • • • • • • • •				<u> </u>			
	31				0			
Data		Long word data						
	-							
A : Associativ	e bit (1: associative, 0:	non-associative)						
		5'10: way 2, B'11: way 3)						
E: Entry addr								
LRU: LRU bit								
	ritten, 0: not written)	in dischlod)						
	V: V bit (1: entry is enabled, 0: entry is disabled) L: Position of longword (B'00: longword 0, B'01: longword 1, B'10: longword 2, B'11: longword 3)							

Figure 3 How to Specify the Memory-Mapped Cache Access (Operand Cache)



2.6 Sample Program Flow

Figure 4 shows the flow chart of the sample program. Figure 5 shows the flow chart of writing back the operand cache.

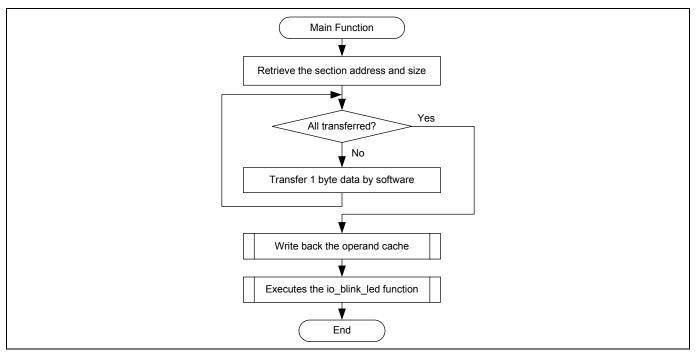


Figure 4 Sample Program Main Flow Chart



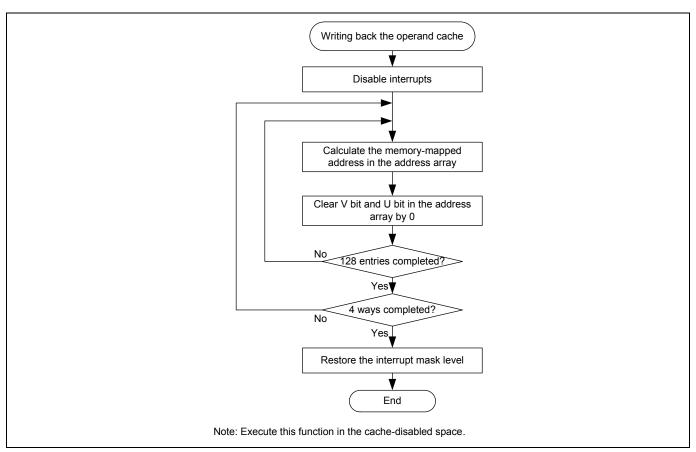


Figure 5 Flow Chart of Writing Back Operand Cache



3. Sample Program Listing

3.1 Sample Program Listing "main.c" (1/5)

```
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2
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        *""FILE COMMENT""********* Technical reference data ******************************
29
       *
           System Name : SH7264 Sample Program
30
31
          File Name : main.c
32
        * Abstract : Transferring Program to RAM (CPU transfer).
          Version : 1.00.00
33
34
           Device
                     : SH7262/SH7264
       *
35
           Tool-Chain : High-performance Embedded Workshop (Ver.4.04.01).
36
       *
                     : C/C++ compiler package for the SuperH RISC engine family
37
                     :
                                               (Ver.9.02 Release00).
38
          OS
                     : None
39
       *
          H/W Platform: M3A-HS64G50 (CPU board)
40
          Description :
       41
                     : Aug.04,2009 Ver.1.00.00
42
           History
       43
44
        #include <machine.h>
45
        #include "iodefine.h"
```



3.2 Sample Program Listing "main.c" (2/5)

```
46
47
    /* ==== Prototype declaration ==== */
48
    void main(void);
49
   void io_blink_led(void);
50
   void io_init_cmt0(void);
51
    extern int io_cache_writeback(void);
52
    53
54
    * ID
         :
55
     * Outline
             : Sample program main (Transfer program from ROM to RAM).
56
     *_____
57
     * Include
              : iodefine.h
58
     *_____
59
     * Declaration : void main(void);
60
     *_____
61
     * Description : Transfers the section PROM to the section PRAM allocated on
62
              : internal RAM by software, and executes the transferred proram
63
              : (io_blink_led) function.
64
     *_____
65
     * Argument
              : void
     *_____
66
67
     * Return Value : void
68
    *_____
69
     * Note
              :
70
     71
    void main(void)
72
   {
73
     unsigned char *src,*dst;
74
     unsigned long size;
75
76
     /* ==== Retrieves the section address and size ==== */
77
     src = __sectop("PROM");
78
     dst = __sectop("PRAM");
79
     size = __secsize("PROM");
80
81
     /* ==== Transfers the section ==== */
82
     while(size-- > 0ul){
83
      *dst++ = *src++;
84
     }
85
86
     /* ==== Writes back the operand cache ==== */
87
     io_cache_writeback();
88
89
     /* ==== Executes the io_blink_led function ==== */
90
     io_blink_led(); /* Inverts the port A0 */
91
    }
92
93
    #pragma section ROM /* Following section P is handled as section PROM. */
```



3.3 Sample Program Listing "main.c" (3/5)

* ID	:	
* Outline	: Count at a constan	nt period
* Include	: iodefine.h	
* Declaration	: void io_blink_led	
		/O port PAO (connected to the LED) and the
*	: compare match time	er CMT0 at 1 ms to turn ON or OFF the LED
*		PAO onece every 1000 times 1 ms flagff
* Argument	: void	
* Return Valu	e : void	
		ROM and transfer section PRAM in the linkage
		he [ROM to RAM mapped sections].
*""FUNC COMME	- NT END""************	 ***********************************
oid io_blink_	led(void)	
volatile uns	igned int CountCMT0 =	1000; /* For 1 sec soft count */
/* ==== Init	ializes the LED ====	*/
/* PB22	(Control signal to e	nable the PAO) */
PORT.PBCR5.B	SIT.PB22MD = 0;	/* Sets the function of the PB22 pin
		to general-purpose I/O */
PORT.PBDR1.B	SIT.PB22DR = 1;	/* Specifies the output data as 1 */
PORT.PBIOR1.	BIT.PB22IOR = 1;	/* Specifies the direction to output */
/* PAO	(Signal to turn ON or	OFF the LED) */
	SIT.PA0DR = $1;$	/* Specifies the output data as 1 */
PORT.PADR0.B		



3.4 Sample Program Listing "main.c" (4/5)

```
127
      /* ==== Initializes the CMT0 (1 ms periodic timer) ==== */
128
      io_init_cmt0();
129
130
     while(1){
131
       /* ---- Verifies the compare match (1 ms) flag ---- */
132
       while (CMT.CMCSR0.BIT.CMF == 0){
133
          /* Waits for 1 ms elapsed */
134
      }
135
       CMT.CMCSR0.BIT.CMF = 0;
                                   /* Clears the compare match flag (CMF) to 0 */
136
       CountCMT0--;
                                /* Updates the 1 sec soft counter (CountCMT0) */
137
       /* ---- Verifies the 1 sec soft counter ---- */
138
      if(CountCMT0 == 0u){
139
          CountCMT0 = 1000u;
                                /* Initializes the 1 sec soft counter again */
140
          PORT.PADR0.BIT.PA0DR ^= 1u ; /* Inverts the port A0 output */
141
      }
142
     }
143
     }
     144
145
     * ID
               :
146
     * Outline
               : CMT0 periodic timer setting
147
     *_____
148
     * Include
                : iodefine.h
149
     *_____
150
     * Declaration : void io_init_cmt0(void);
151
     *_____
152
     * Description : Sets the CMT0 to set the CMF flag at every 1 ms.
153
     *_____
154
     * Argument
                : void
155
     *_____
156
     * Return Value : void
157
     *_____
158
     * Note
                : Add the section PROM and transfer section PRAM in the linkage
159
                : editor options and set the [ROM to RAM mapped sections].
160
     161
    void io_init_cmt0(void)
162
     {
163
      /* ==== Configures the periodic (1 ms) timer ==== */
164
      /* ---- Sets the Standby control register 7 (STBCR7) ---- */
165
      CPG.STBCR7.BIT.MSTP72 = 0x0;/* Enables the CMT */
166
167
      /* ---- Sets the Compare match timer start register (CMSTR) ---- */
168
      CMT.CMSTR.BIT.STR0 = 0;
                            /* Stops channel 0 to count */
169
170
      /* ---- Sets the Compare match control/status register (CMCSR0) ---- */
171
      CMT.CMCSR0.WORD = 0x0002; /* Disables the compare match interrupt,
172
                           specifies 1/128 of the peripheral clock */
173
```



3.5 Sample Program Listing "main.c" (5/5)

```
174
       /* ---- Sets the Compare match timer counter register (CMCNT0) ---- */
       CMT.CMCNT0.WORD = 0x0000; /* Clears the timer counter */
175
176
177
       /* ---- Sets the Compare match timer constant register (CMCOR0) ---- */
178
      CMT.CMCOR0.WORD = 280; /* Sets the period to compare match (1 ms) */
                                 /* 1 ms = 1/P clock (36 MHz) * 128 * (280+1) */
179
       /* ---- Sets the Compare match timer start register (CMSTR) ---- */
180
      CMT.CMSTR.BIT.STR0 = 1; /* Starts channel 0 to count */
181
182 }
183 /* End of File */
```



3.6 Sample Program Listing "cache.c" (1/3)

```
1
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3
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28
       *
       *""FILE COMMENT""********* Technical reference data ******************************
29
       *
          System Name : SH7264 Sample Program
30
       * File Name : cache.c
31
32
       * Abstract : sample of cache register
       * Version
                   : 1.01.00
33
34
       *
          Device
                    : SH7262/SH7264
       * Tool-Chain : High-performance Embedded Workshop (Ver.4.04.01).
35
36
       *
                    : C/C++ compiler package for the SuperH RISC engine family
37
                     :
                                              (Ver.9.02 Release00).
       * OS
38
                    : None
       * H/W Platform: M3A-HS64G50(CPU board)
39
       * Description :
40
       41
       *
42
          Historv
                    : Dec.03,2008 Ver.1.00.00
43
       *
                    : Jun.29,2009 Ver.1.01.00 Changed FILE FORMAT
       44
45
       #include <machine.h>
46
       #include "iodefine.h"
```



3.7 Sample Program Listing "cache.c" (2/3)

```
47
48
49
    /* ==== Prototype Declaration ==== */
   void io_init_cache(void);
50
51
   int io_cache_writeback(void);
52
53
54
    #pragma section CACHE /* It is placed in the CS0 cache-disabled space */
101
   102
    * ID
           :
103
    * Outline
            : Write-back of cache
104
    *_____
           : iodefine.h
105
    * Include
    *_____
106
107
    * Declaration : int io_cache_writeback(void);
108
    *_____
109
    * Description : All lines of operand cache are disabled, and the contents of
110
             : cache memory are written back to the external memory.
111
    *
            : It has nothing to do with the write-through mode.
    *_____
112
113
    * Argument
             : void
114
    *_____
115
    * Return Value : 0 : Normal completion
116
    *_____
117
    * Note
             : None
    118
119
   int io_cache_writeback(void)
120
    {
121
   volatile unsigned long *arry;
122
    unsigned int i,j;
123
    int mask;
124
125
    /* ==== Interrupt mask setting ==== */
126
   mask = get_imask();
127
    set_imask(15);
                       /* Set to the level 15 */
128
```



3.8 Sample Program Listing "cache.c" (3/3)

```
129
        /* ==== All entries disabled ==== */
       for(i=0u; i <4u; i++){</pre>
130
131
         for(j=0u; j < 128u; j++){
132
            /* ---- Creating an address array address ---- */
133
            arry = (volatile unsigned long *)(0xf0800000 | (i<<11) | (j<<4));
            /* ---- Write U=0 and V=0 in the address array ---- */
134
135
             *arry &= 0xfffffffcul; /* V=0,U=0 */
136
        }
137
       }
138
139
       /* ==== Interrupt mask recovery ==== */
       set_imask(mask);
                                 /* Set to the original level */
140
141
142
       return 0;
143
    }
144
145
146
    /* End of File */
```



4. References

- Software Manual SH-2A/SH-2A-FPU Software Manual Rev. 3.00 (Download the latest version from the Renesas website.)
- Hardware Manual SH7262 Group, SH7264 Group Hardware Manual Rev. 1.00 (Download the latest version from the Renesas website.)



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Revision History

		Descript	ion		
Rev.	Date	Page	Summary		
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