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H8SX Family

Transfer of Longword Data to Odd Addresses—DTC Edition

Introduction

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even. The DTC is capable of operating in the same way.

In the example given in this application note, the DTC is activated by IRQ0 interrupt instruction to transfer longword data, altering the boundaries to odd addresses from even addresses.

Target Device

H8SX/1653F

Contents

1. Specification

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even.

The DTC is used to transfer data allocated to odd addresses. When an H8SX MCU transfers data allocated to odd addresses as the boundary in memory, the user doesn't have to think about the operation since the hardware handles boundary-related control.

1. The DTC is used to transfer data from the on-chip ROM area to the on-chip RAM area.
2. Data in the on-chip ROM are allocated to even addresses as the longword boundaries, and the on-chip RAM area is set to odd addresses.
3. Data access size is set to longword and the transfer mode is set to block transfer, then four longwords (16 bytes) of data are transferred.

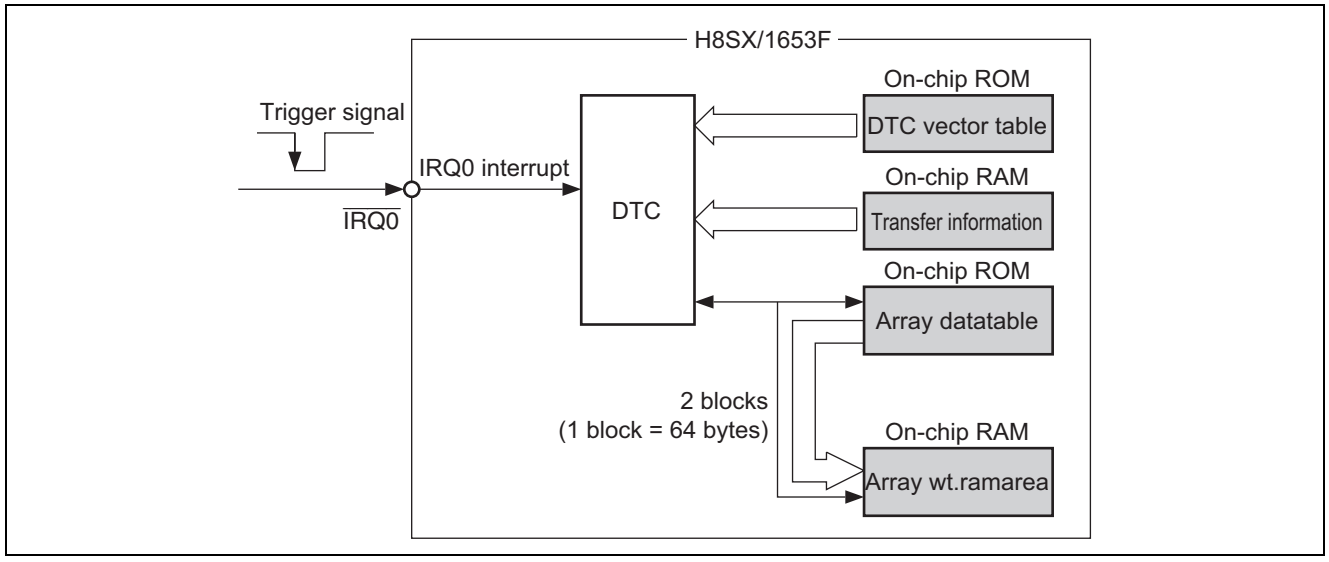


Figure 1 DTC Transfer of Data Allocated to Odd Addresses

2. Applicable Conditions

Table 1 Applicable Condition

Item	Details
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Functions Used

Figure 2 is a block diagram of the DTC. The block diagram is explained below.

The registers shown below cannot be directly accessed by the CPU. The values to be set in the registers must be stored in the data area as transfer information. When a DTC activation source event occurs, the DTC reads out the first address of the transfer information from the vector address assigned to the given activation source, copies the desired transfer information to the registers in the DTC, and transfers the data. After transferring the data, the DTC writes the contents of the registers back to the data area.

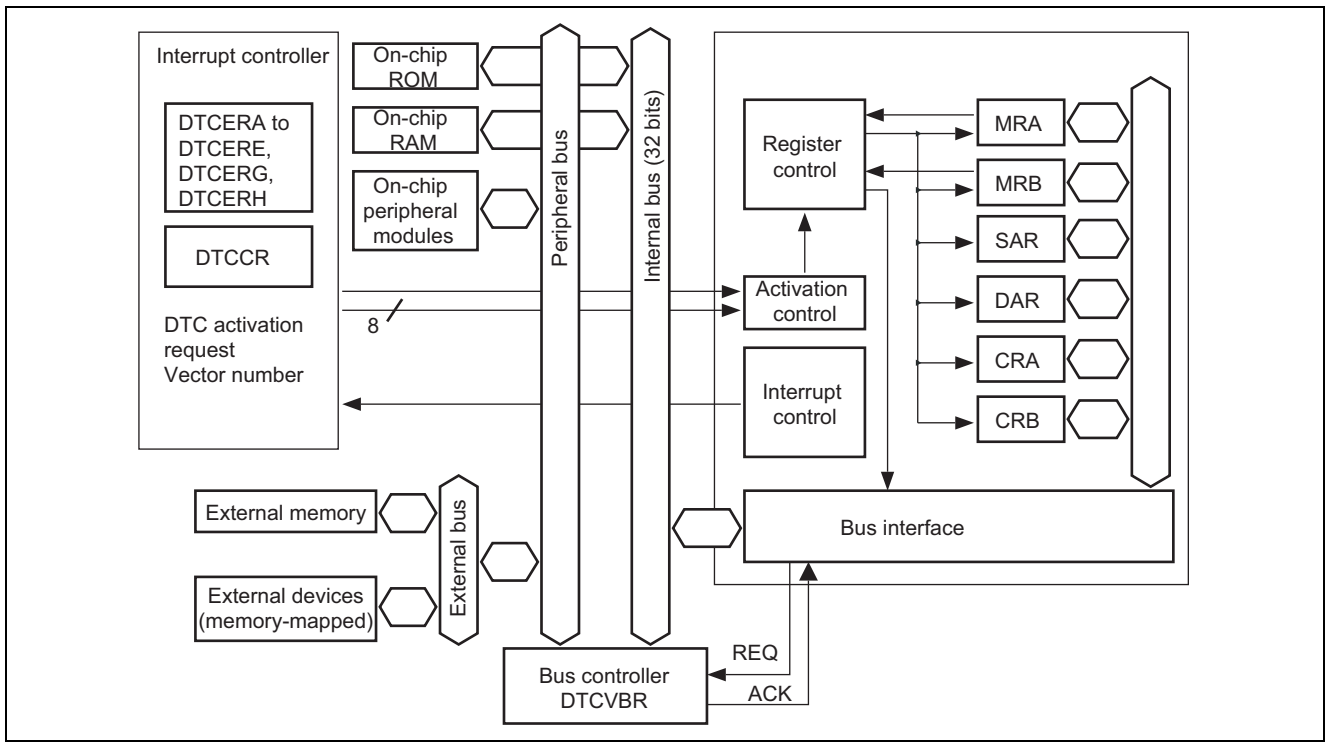


Figure 2 Block Diagram of DTC

- DTC mode register A (MRA)

MRA selects the DTC operating mode. In this sample task, the transfer mode is normal, the transfer data size is set to longword, and incrementation of SAR after each data transfer is selected.

- DTC mode register B (MRB)

MRB selects the DTC operating mode. In this sample task, the destination is specified as a block area, and incrementation of DAR after each data transfer is selected.

- DTC source address register (SAR)

SAR specifies the source address for data transfer.

- DTC destination address register (DAR)

DAR specifies the destination address for data transfer.

- DTC transfer count register A (CRA)

CRA specifies the number of times data is to be transferred by the DTC. In block transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the block size while CRAL functions as an 8-bit block-size counter (1 to 256, indicating bytes, words, or longwords). In this sample task, the block size is specified as 4 longwords (16 bytes) of data.

- DTC transfer count register B (CRB)

CRB specifies the number of times block data is to be transferred by the DTC in block transfer mode.

The registers covered below are in the interrupt controller or bus controller and are directly accessible to the CPU.

- DTC enable registers A to E, G, and H (DTCERA to DTCERE, DTCERG, and DTCERH)

The DTCER registers (DTCERA to DTCERE, DTCERG, and DTCERH) select the DTC activation interrupt sources. Refer to the hardware manual for the correspondence between the interrupt sources and DTCE bits. In this sample task, the IRQ0 interrupt is selected as the activation source.

- DTC control register (DTCCR)

DTCCR specifies DTC activation by the IRQ0 interrupt.

- DTC vector base register (DTCVBR)

DTCVBR specifies the base address to be used in calculating vector table addresses.

4. Principle of Operation

4.1 Example of Data Transfer to Odd Addresses

Figure 3 is a schematic view of the data transfer to odd addresses. Four longwords (16 bytes) of data are transferred from H'003000 to H'FF2001 by longword access in block transfer mode.

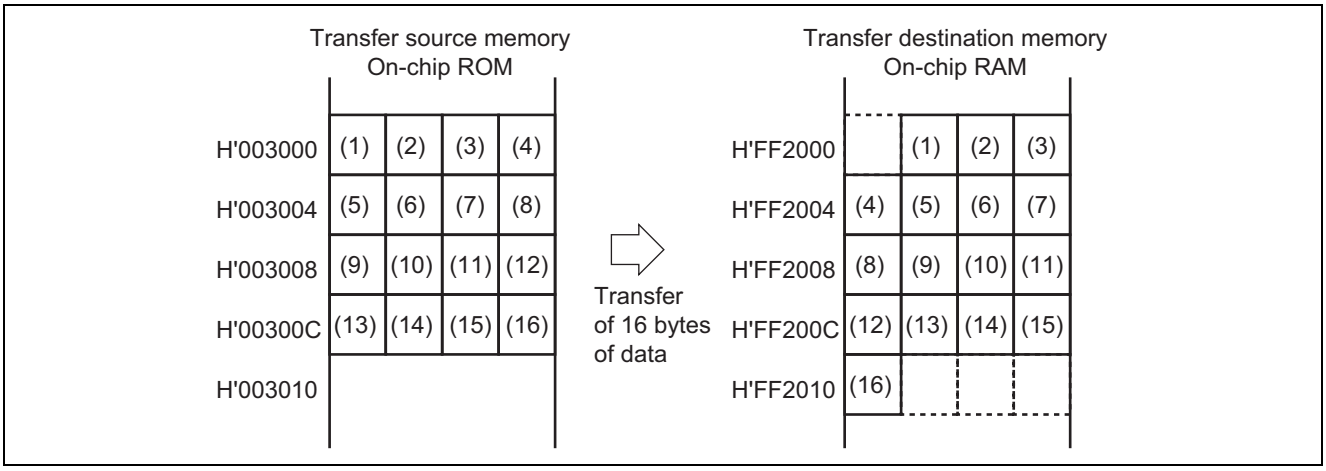


Figure 3 Example of Data Transfer to Odd Addresses

4.2 Timing of Data Transfer to an Odd Address

Figure 4 is a timing chart for data transfer to an odd address. Data in on-chip ROM allocated to an address aligned with a longword boundary are read in one cycle of longword (L) access, and then written to an odd address in on-chip RAM in a total of three cycles, for byte (B), word (W), and byte (B) access.

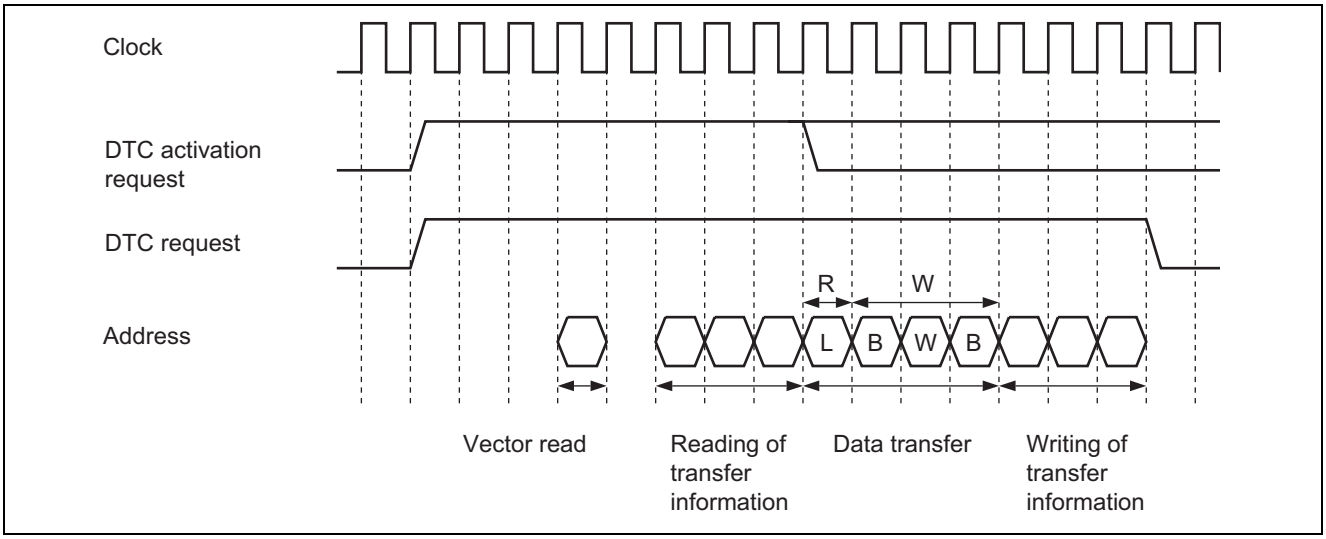


Figure 4 Example of Timing for Data Transfer to an Odd Address

4.3 DTC Transfer Information

4.3.1 Configuration of Transfer Information

Figure 5 shows the configuration of the transfer information in memory when the DTC is in short address mode. In this sample task, the start address of transfer information is set to H'FFB000.

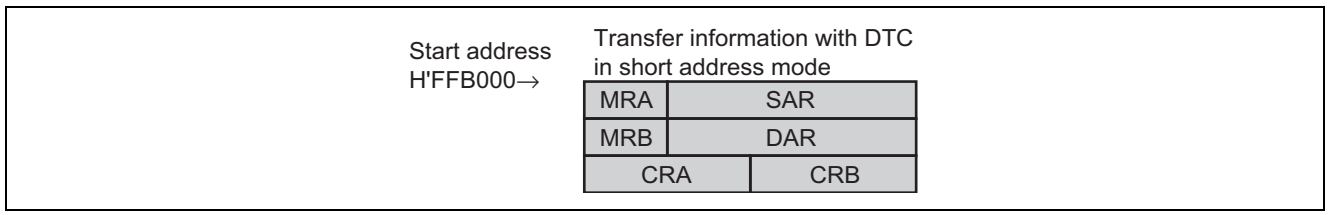


Figure 5 Configuration of Transfer Information

4.3.2 Correspondence between Vector Table and Transfer Information

Figure 6 shows the correspondence between the vector table and transfer information. In this sample task, the vector table address is calculated as H'00002500 based on the contents of DTCVBR. The first address (H'FFB000) of the transfer information is set in this location of the vector table, and the transfer information is read from there into the registers of the DTC.

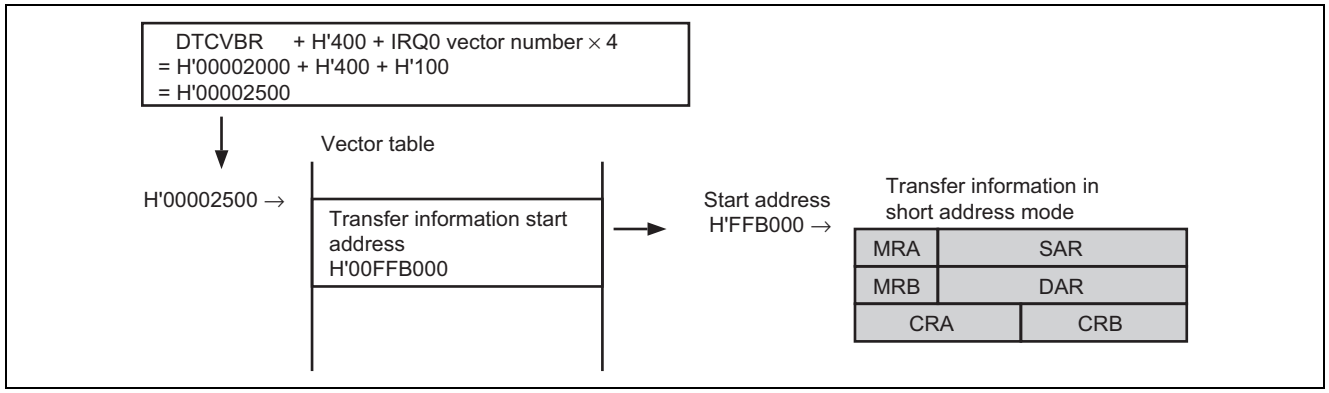


Figure 6 Correspondence between Vector Table and Transfer Information

5. Description of Software

5.1 Operating Environment

Table 2 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.01 (manufactured by Renesas Technology)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 3 Setting of Sections

Address	Section	Description
H'001000	P	Program area
H'002500	CDTCV	DTC vector address storage area
H'003000	C	Data table storage area Array datatable is allocated here.
H'FF2000	B	Non-initialized data area (RAM area) The wt structure is allocated here.

Table 4 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init
IRQ0	64	H'000100	irq0_int

5.2 List of Functions

Table 5 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function.
main	Main routine Makes initial settings for the DTC. These are for block transfer in 4 longwords × 1 block and enabling transfer.
irq0_int	IRQ0 interrupt handling routine

5.3 RAM Usage

Table 6 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	wt.dummy	wt structure This dummy variable is used to set wt.ramarea to an odd address.	main
unsigned char	wt.ramarea[16]	wt structure Transfer destination area in RAM	main
DTC_tag	TRINFO	DTC transfer information (start address: H'FFB000)	main

5.4 Constants

Table 7 Constants

Type	Variable Name	Settings	Description	Used in
unsigned long	datatable[4]	H'00010203, H'04050607, H'08090A0B, H'0C0D0E0F	Holds source data for transfer.	main

5.5 Description of Functions

5.5.1 init Function

1. Functional overview

Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by pins MD3 to MD0.

Table 8 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC.
8	ICK0	0	R/W	000: Input clock×4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock ×2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock ×4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	0	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

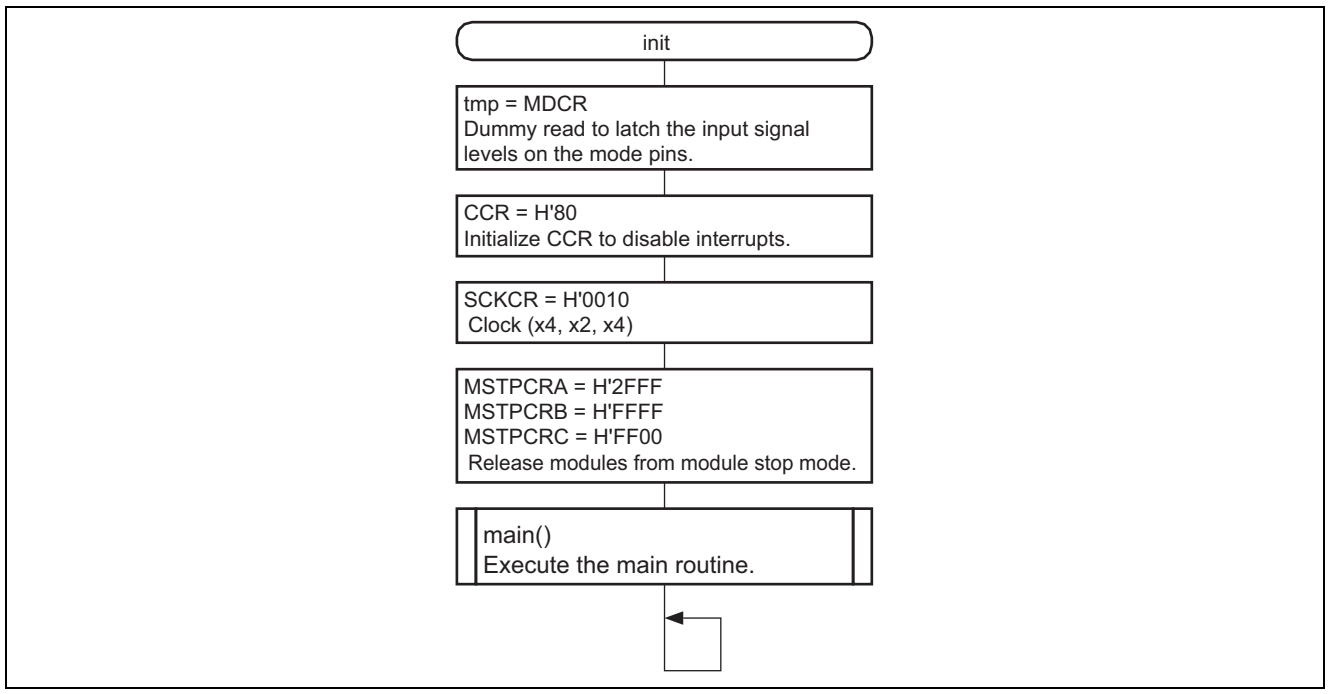
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
Clock (x4, x2, x4)
MSTPCRA = H'2FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
Release modules from module stop mode.
main()
Execute the main routine.

5.5.2 main Function

1. Functional overview

Main routine which sets up the DTC for transfer and performs transfer start processing.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- DTC mode register A (MRA) (Cannot be directly accessed by the CPU.)

Bit	Bit Name	Setting	R/W	Description
7	MD1	1	–	DTC Mode 1, 0
6	MD0	0		10: Block transfer mode
5	Sz1	1	–	DTC Data Transfer Size 1, 0
4	Sz0	0		10: Longword-size transfer
3	SM1	1	–	Source Address Mode 1, 0
2	SM0	0		These bits specify the SAR operation after a data transfer. 10: Increments SAR after a transfer.

- DTC mode register B (MRB) (Cannot be directly accessed by the CPU.)

Bit	Bit Name	Setting	R/W	Description
4	DTS	0	–	DTC Transfer Mode Select 0: Specifies the destination as repeated or a block area. 1: Specifies the source as repeated or a block area.
3	DM1	1	–	Destination Address Mode 1, 0
2	DM0	0		These bits specify the DAR operation after a data transfer. 10: DAR is incremented after a transfer.

- DTC source address register (SAR) (not directly accessible by the CPU.)

Function: Setting the transfer source address

Setting: Start address of array datatable

- DTC destination address register (DAR) (not directly accessible by the CPU.)

Function: Setting the transfer destination address

Setting: Start address of array wt.ramarea

- DTC transfer count register A (CRA) (not directly accessible by the CPU.)

Function: Setting the block size in block transfer mode. When Sz1 and Sz0 in MRA = B’10 (longword-size transfer) and CRA = H’0404, the block size is 4 longwords (4 bytes).

Setting: H'0404

- DTC transfer count register B (CRB) (not directly accessible by the CPU)

Function: Setting the number of times data is to be transferred in block transfer mode. CRB is decremented by 1 every time data is transferred.

Setting: H'0001

- Port 5 input buffer control register (P5ICR) Number of bits: 8 Address: H'FFFB94

Bit	Bit Name	Setting	R/W	Description
0	P50ICR	1	R/W	0: Disables the input buffer of the P50 pin. 1: Enables the input buffer of the P50 pin.

- Port function control register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
0	ITS0	1	R/W	$\overline{\text{IRQ0}}$ Pin Select 0: Selects the P10 pin as the $\overline{\text{IRQ0}}$-A input. 1: Selects the P50 pin as the $\overline{\text{IRQ0}}$-B input.

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
1	IRQ0SR	0	R/W	IRQ Sense Control Rise
0	IRQ0SF	1	R/W	IRQ Sense Control Fall 01: Interrupt requests are generated by the falling edges of the $\overline{\text{IRQ0}}$ input.

- DTC vector base register (DTCVBR) Number of bits: 32 Address: H'FFFD80

Function: DTCVBR is a 32-bit register that specifies the base address used to calculate the vector table address.

Setting: H'00002000

- DTC enable register A (DTCERA) Number of bits: 16 Address: H'FFFF20

Bit	Bit Name	Setting	R/W	Description
15	DTCEA15	1	R/W	0: The IRQ0 interrupt is not selected as the DTC activation source. 1: The IRQ0 interrupt is the DTC activation source.

- DTC control register (DTCCR) Number of bits: 8 Address: H'FFFF30

Bit	Bit Name	Setting	R/W	Description
4	RRS	1	R/W	DTC Transfer Information Read Skip Enable 0: Disables skipping of transfer information read. 1: Reading of transfer information is skipped when the vector numbers match.
0	ERR	0	R/(W)*	Transfer Stop Flag 0: Neither an address error nor an NMI interrupt request has occurred. 1: An address error or an NMI interrupt request has occurred.

Note: * Only 0 can be written here, to clear the flag.

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

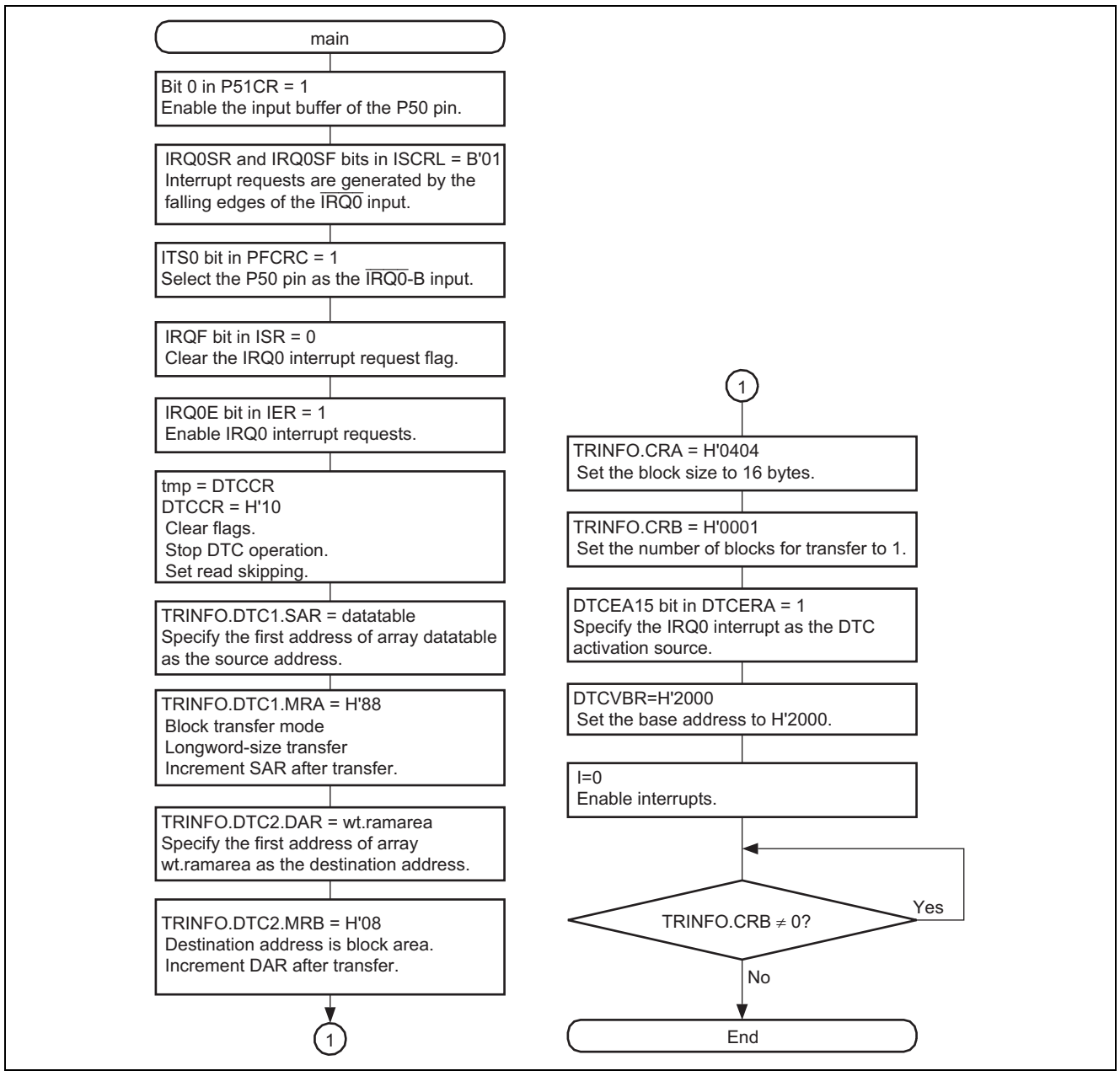
Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	1	R/W	IRQ0 Enable 0: Disables IRQ0 interrupt requests. 1: Enables IRQ0 interrupt requests.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
0	IRQ0F	0	R/(W)*	IRQ0 Status 0: IRQF0 interrupt has not been generated. 1: IRQ0 interrupt has been generated.

Note: * Only 0 can be written here, to clear the flag.

5. Flowchart



5.5.3 irq0_int Function

1. Functional overview

IRQ0 interrupt handling routine

2. Argument

None

3. Return value

None

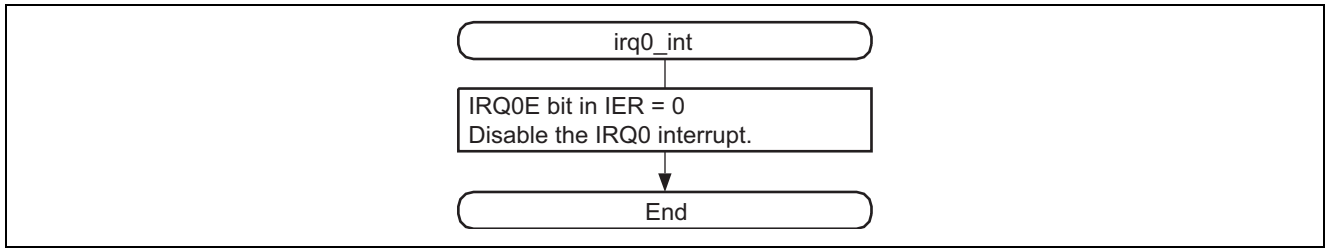
4. Description of internal registers

The internal registers used in this sample task are described below. The setting shown in the table below is the value used in this sample task and differs from the initial value.

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	0	R/W	IRQ0 Enable 0: Disables IRQ0 interrupt requests. 1: Enables IRQ0 interrupt requests.

5. Flowchart



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