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H8/300H Tiny Series

Timer Z Input Capture Operation

Introduction

The timer Z input-capture function is used.

Target Device

H8/3687

Contents

1. Specifications

1. The input-capture function of timer Z is used.
2. The TCNT0 value is transferred to the GRA0 at the rising edge of a pulse input to the input-capture input pin A0 (FTIOA0).

2. Description of Functions

1. In this sample task, the timer Z input-capture function is used. Figure 2.1 is a block diagram of timer Z input-capture function. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) selects TCNT0 input clock. In this sample task, the input clock is specified as ϕ/8 and TCNT0 is incremented at the rising edge of ϕ/8.
- Timer I/O control register A0 (TIORA0) controls GRA0 and GRB0. In this sample task, GRA0 used an input-capture register, and the TCNT0 value is transferred to the GRA0 at the rising edge of the FTIOA0 pin.
- Timer status register 0 (TSR0) indicates the timer Z status. In this sample task, the input-capture/compare-match flag A (IMFA) are set to one when a GRA0 input capture occurs.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by an internal clock or external clock input. In this sample task, the input clock is specified as ϕ/8 and TCNT0 is incremented at the rising edge of ϕ/8.
- General register A0 (GRA0) a 16-bit readable/writable register. In this sample task, the GRA0 is used as an input-capture register and the TCNT0 value is transferred to the GRA0 at the rising edge of the FTIOA0 pin.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 is specified to start counting and TCNT1 is specified to stop counting.
- Timer mode register (TMDR) specifies synchronous or independent operation of TCNT0 and TCNT1. In this sample task, TCNT0 operates independently of TCNT1.
- Timer function control register (TFCR) specifies operation modes and selects the output level. In this sample task, channels 0 and 1 are specified for normal operation.
- The input-capture/output-compare A0 pin (FTIOA0) is specified as an input-capture input pin. The TCNT0 value is transferred to the GRA0 at the rising edge of the FTIOA0 pin.

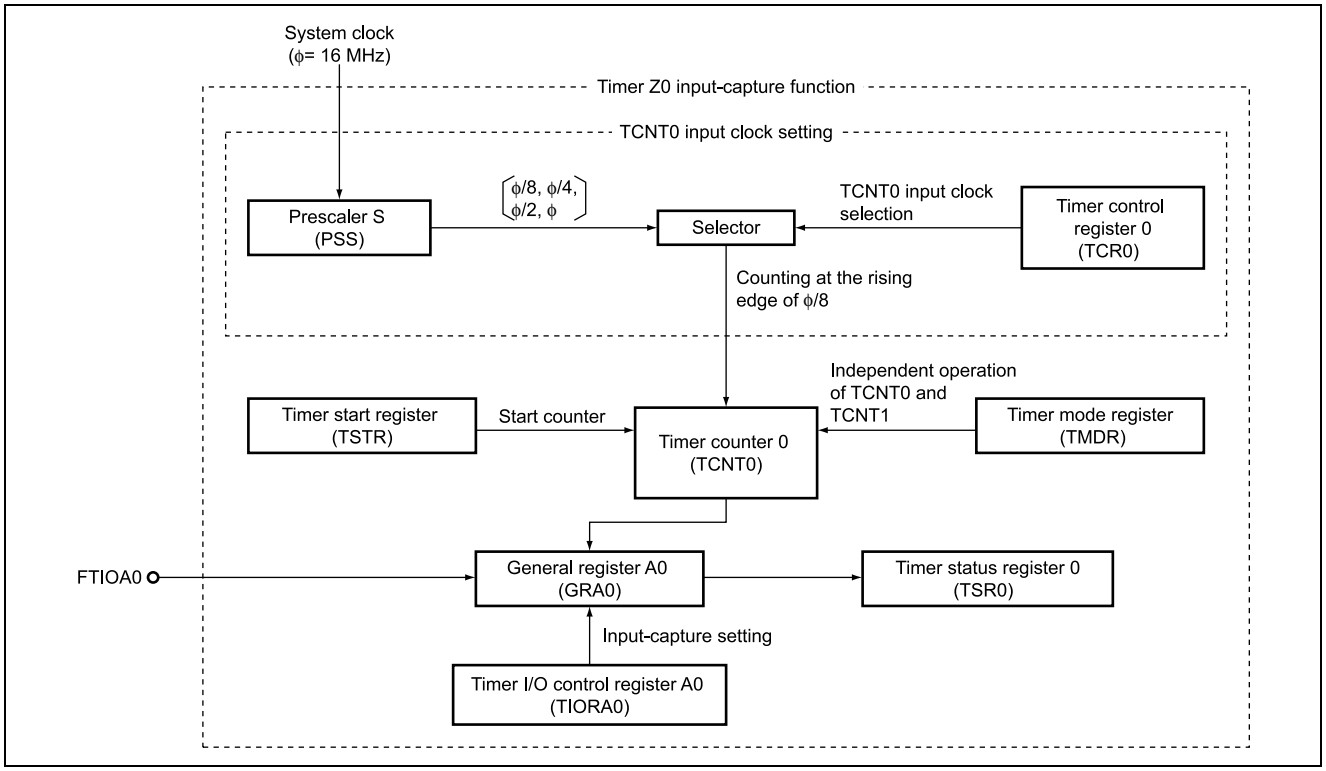


Figure 2.1 Block Diagram of Timer Z0

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so as to cause the input-capture function to operate.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCR0	Specifies the TCNT0 input clock
TIORA0	Specifies the GRA0 as an input-capture register.
TSR0	Controls the flag by GRA0 input capture.
TCNT0	16-bit counter that counts at the rising edge of ϕ/8
GRA0	The contents of TCNT0 is transferred to the GRA0 at the rising edge of the FTIOA0 pin
TSTR	Controls TCNT0 count start and stop.
TMDR	Specifies TCNT0 to operate independently of TCNT1
TFCR	Specifies channels 0 and 1 for normal operation
FTIOA0 pin	Pulse input pin

3. Description of Operation

Figure 3.1 illustrates the operation of this sample task. The hardware and software processing are applied as shown in figure 3.1 to cause the input-capture function to operate.

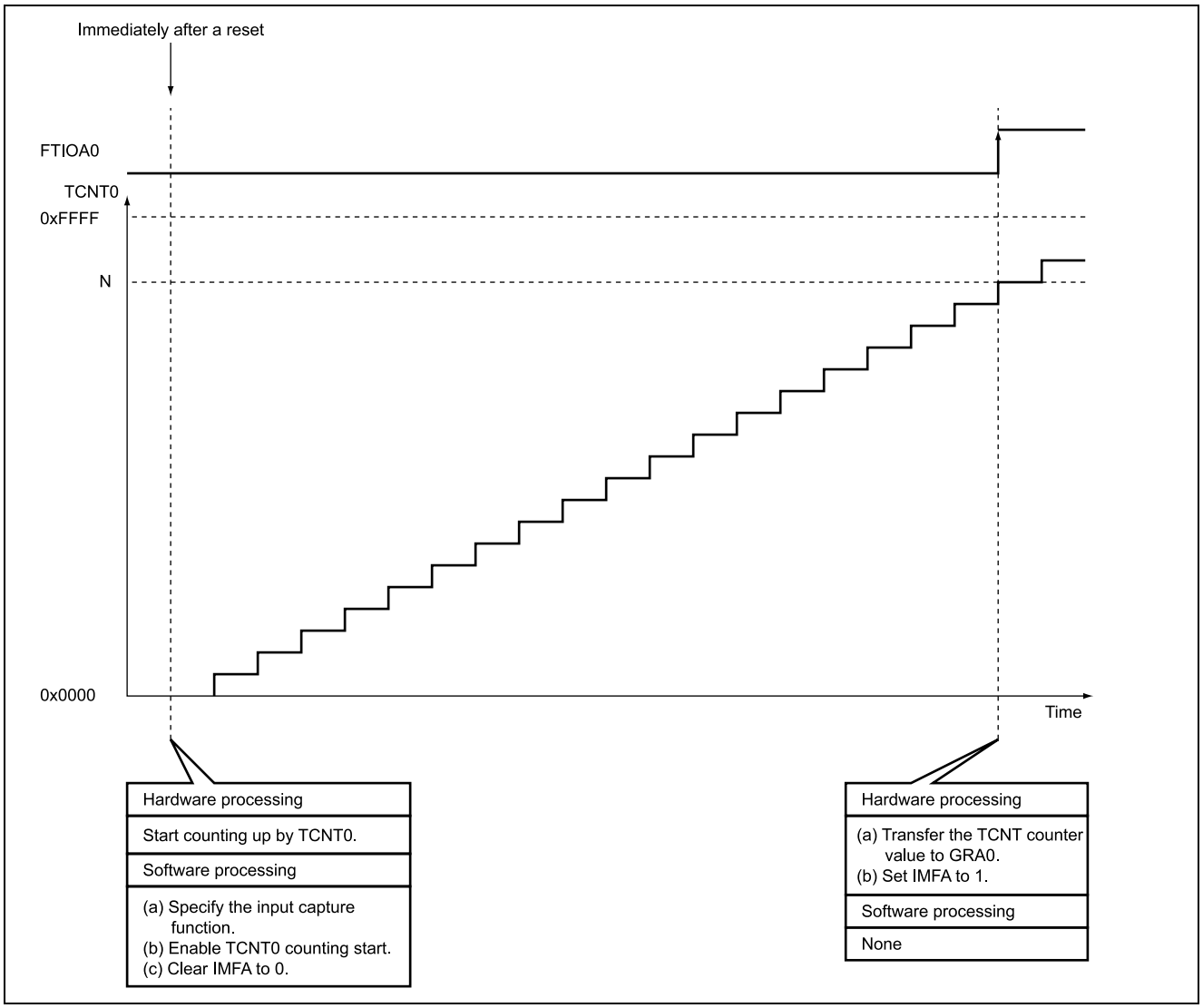


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of the Module

Module Name	Label Name	Function
Main routine	main	Sets the timer Z0 input-capture function.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts at the rising edge of the clock.
2	TPSC2	TPSC2 = 0	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 1	TPSC2 = 0, TPSC1 = 1, TPSC0 = 1: Counts by ϕ/8.
0	TPSC0	TPSC0 = 1	

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
2	IOA2	IOA2 = 1	I/O control A2 to A0
1	IOA1	IOA1 = 0	IOA2 = 1, IOA1 = 0, IOA0 = 0:
0	IOA0	IOA0 = 0	Specifies the GRA0 as an input-capture register and specifies the TCNT0 value to be transferred to the GRA0 at the rising edge of the FTIOA0 pin.

- TSR0 Timer status register 0 Address: 0xF703

Bit	Bit Name	Setting	Function
0	IMFA	0	Input-capture/compare-match flag A When the GRA0 functions as an input-capture register, indicates whether or not the TCNT0 value has been transferred to the GRA0 by the input-capture signal. IMFA = 0: Indicates that the TCNT0 value has not been transferred to the GRA0. IMFA = 1: Indicates that the TCNT0 value has been transferred to the GRA0.

- TCNT0 Timer counter 0 Address: 0xF706
  Function: A 16-bit upward counter that is incremented at the rising edge of ϕ/8.
  Setting: 0x0000

- GRA0 General register A0 Address: 0xF708
  Function: The TCNT0 value is transferred to the GRA0 at the rising edge of the FTIOA0 pin during input capture operation.
  Setting: —

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0.

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TFCR Timer function control register Address: 0xF723

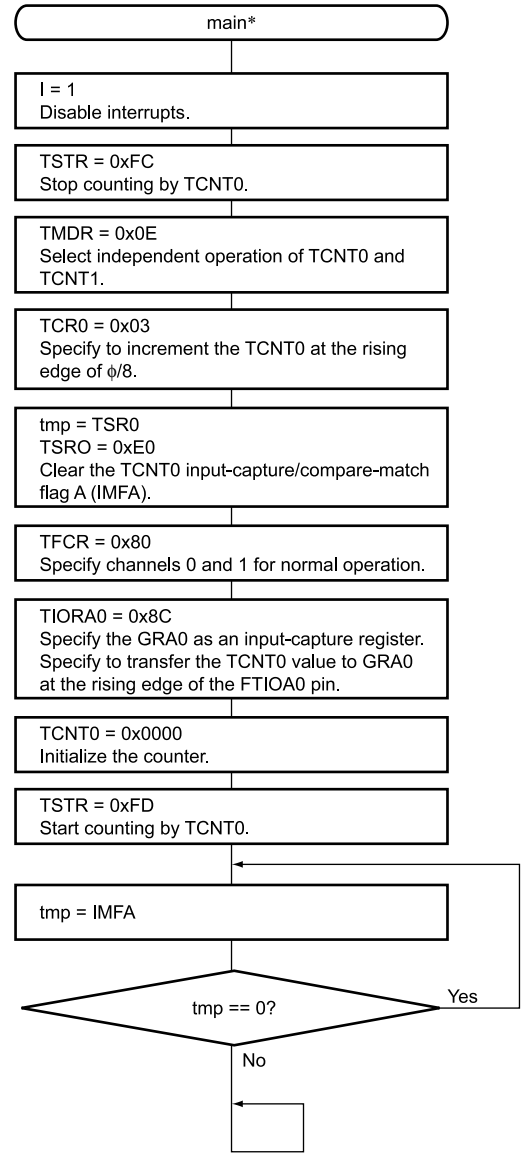
Bit	Bit Name	Setting	Function
1	CMD1	CMD1 = 0	Combination mode 1 to 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMD0 = 0: Channels 0 and 1 operate in normal operation mode.

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Input Caputure Function'                                                                                          */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z Input Caputure                                                                                           */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0               */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0         */
#define        TSR0           *(volatile unsigned char *)0xF703                  /* Timer status register_0                */
#define        TSR0_BIT       (*(struct BIT *)0xF703)                            /* Timer status register_0                */
#define        IMFA           TSR0_BIT.b0                                        /* Input Capture/Compare Match FlagA      */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                        */
#define        GRA0           *(volatile unsigned short *)0xF708                 /* General register A_0                   */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                   */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                    */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register        */

/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                       /* SP Set                                 */
void main ( void );
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                        */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                               */
     INIT                                                               /* 00 Reset                                  */
};

#pragma section                                                         /* P                                         */

/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     volatile unsigned char tmp;

     set_imask_ccr(1);                                                  /* Interrupt Disable                         */

     TSTR = 0xFC;                                                       /* TCNT0 count stop                          */
     TMDR = 0x0E;                                                       /* TCNT0,TCNT1 Single Mode                   */
     TCR0 = 0x03;                                                       /* Rising edge, phi/8 Clock count            */
     tmp = TSR0;
     TSR0 = 0xE0;                                                       /* Interrupt Flag Clear                      */
     TFCR = 0x80;                                                       /* Channel 0,1 operate normally              */
     TIORA0 = 0x8C;                                                     /* Input capture to GRA                      */
                                                                        /* at the rising edge                        */
     TCNT0 = 0x0000;                                                    /* Clear TCNT0                               */
     TSTR = 0xFD;                                                       /* TCNT0 count start                         */

     do{
          tmp = IMFA;
     }while(tmp == 0);

     while(1);
}
```

Link address specifications

Section Name	Address
CV1	0x0000
P	0x0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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